HI-REL DATA SHEET

HM 65797

256 k x 1 HIGH SPEED CMOS SRAM

FEATURES

- **FAST ACCESS TIME : 25*/35/45/55 ns**
- **LOW POWER CONSUMPTION**
  ACTIVE : 550 mW
  STANDBY : 190 mW
- **WIDE TEMPERATURE RANGE :**
  - 55°C TO 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**

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* Preliminary

DESCRIPTION

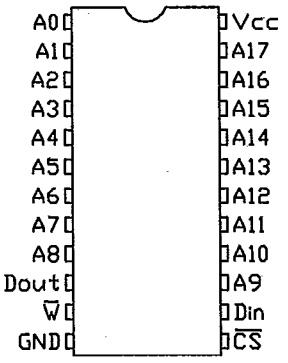
The HM 65797 is a high speed CMOS static RAM organized as 262,144 x 1 bit. It is manufactured using MHS high performance CMOS technology.
Access times as fast as 25 ns are available.
The HM-65797 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 67 % when the circuit is deselected.

Easy memory expansion is provided by active low chip select ($\overline{CS}$) and three state drivers.
All inputs and outputs of the HM 65797 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM 65797 is 100 % processed following the test methods of MIL STD 883C and/or ESA/SCC 9000, making it ideally suitable for military/space applications that demand superior levels of performance and reliability.

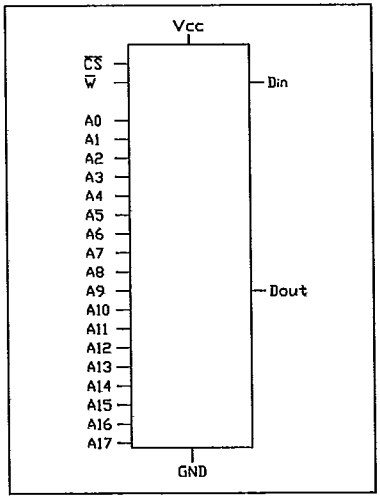
PACKAGES

Ceramic 300 mils, 24 pins, DIL. LCC, 28 pins.

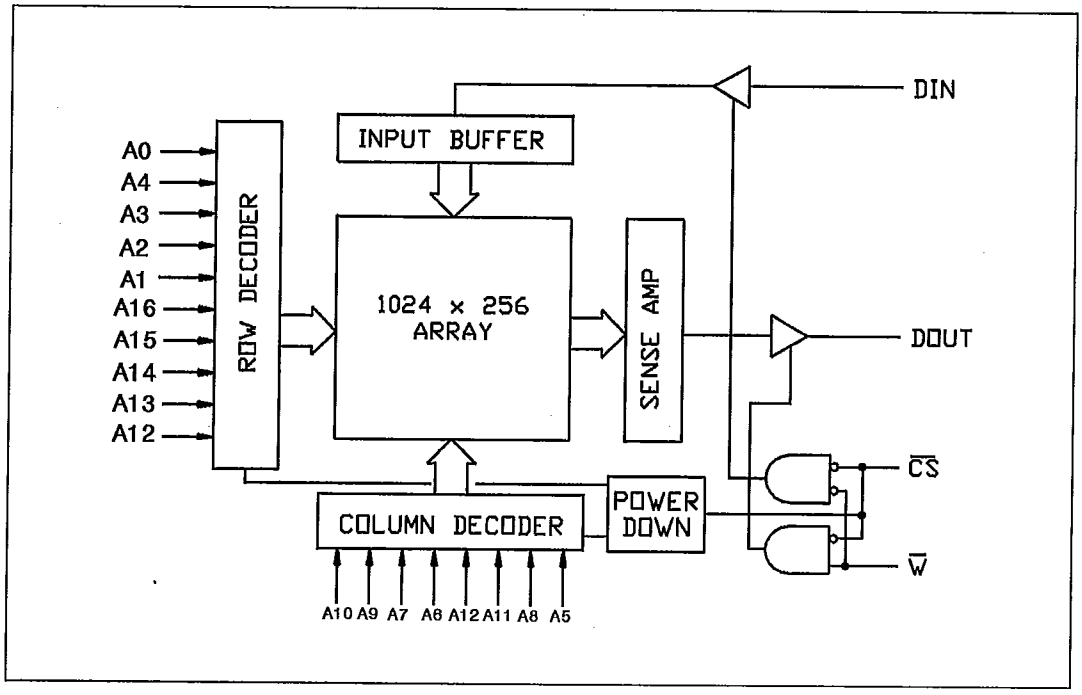
Pinout DIL 24 pins (top view)



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A0-A17 : Address inputs	$\overline{W}$: Write enable
Din : Input	Vcc : Power
Dout : Output	GND : Ground
$\overline{CS}$: Chip Select	

TRUTH TABLE

$\overline{CS}$	$\overline{W}$	INPUT/OUTPUTS	MODE
H	X	High Z	Deselect/Power down
L	H	Data Out	Read
L	L	Data In	Write

L = low, H = high, X = H or L, Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : - 0.5 V to + 7.0 V
DC input voltage : - 3.0 V to 7.0 V
DC output voltage in high Z state : - 0.5 V to + 7.0 V
Storage temperature : - 65°C to + 150°C

Output current into outputs (low) : 20mA
Electro static discharge voltage : >2000 V (MIL STD 883C method 3015)

OPERATING RANGE	OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	5 V ± 10 %	- 55°C to + 125°C
Industrial	5 V ± 10 %	- 40°C to + 85°C

ELECTRICAL CHARACTERISTICS
DC PARAMETERS : MIL STD 883C FOR GROUP A (Subgroups 1, 2, 3, 4)

Parameter	Description	65797 H	65797 K	65797 M	65797 N	Unit	Value	Note 6
ICCSB (1)	Standby supply current	20	20	20	20	mA	Max	M
ICCSB (1a)	Standby supply current	35	35	35	35	mA	Max	M
ICCOP (2)	Operating supply current	120	110	110	110	mA	Max	M
IIX (3)	Input leakage current	+ / - 10	+ / - 10	+ / - 10	+ / - 10	µA	Max	M
IOZ (3)	Output leakage current	+ / - 50	+ / - 50	+ / - 50	+ / - 50	µA	Max	M
VIL (4)	Input low voltage	0.8	0.8	0.8	0.8	V	Max	T
VIH (4)	Input low voltage	2.2	2.2	2.2	2.2	V	Min	T
VOL (5)	Output low voltage	0.4	0.4	0.4	0.4	V	Max	M
VOH (5)	Output high voltage	2.4	2.4	2.4	2.4	V	Min	M
C IN	Input capacitance	5	5	5	5	pF	Max	G
C OUT	Output capacitance	7	7	7	7	pF	Max	G

Notes : 1. $\overline{CS} \geq Vcc - 0.3$ V
1a. $CS \geq VIH$
2. Vcc max, Output current = 0 mA
3. Vcc max, Vin = Gnd to Vcc
4. VIL min = - 3.0V VIH max = Vcc
5. Vcc min, IOL = 8 mA, IOH = - 4 mA
6. Including open/short test or inputs clamp voltage.
G - Guaranted - Not tested : Parameter measured at design validation and at any design change.
M - Measured : Parameter measured and data-log capability.
T - Tested : Parameter verification during testing.

AC TEST LOADS WAVEFORMS

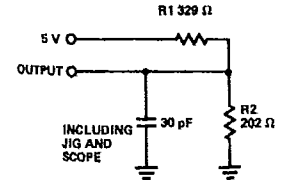


Figure 1a

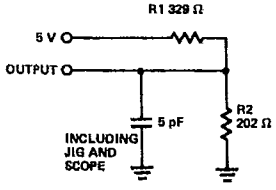


Figure 1b

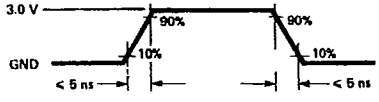
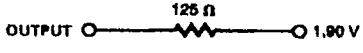
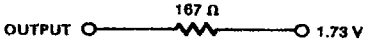


Figure 2

Equivalent to : THEVENIN EQUIVALENT



Commercial



Military

AC PARAMETERS : MIL STD 883C FOR GROUP A (SUBGROUPS 7, 8, 9, 10, 11)

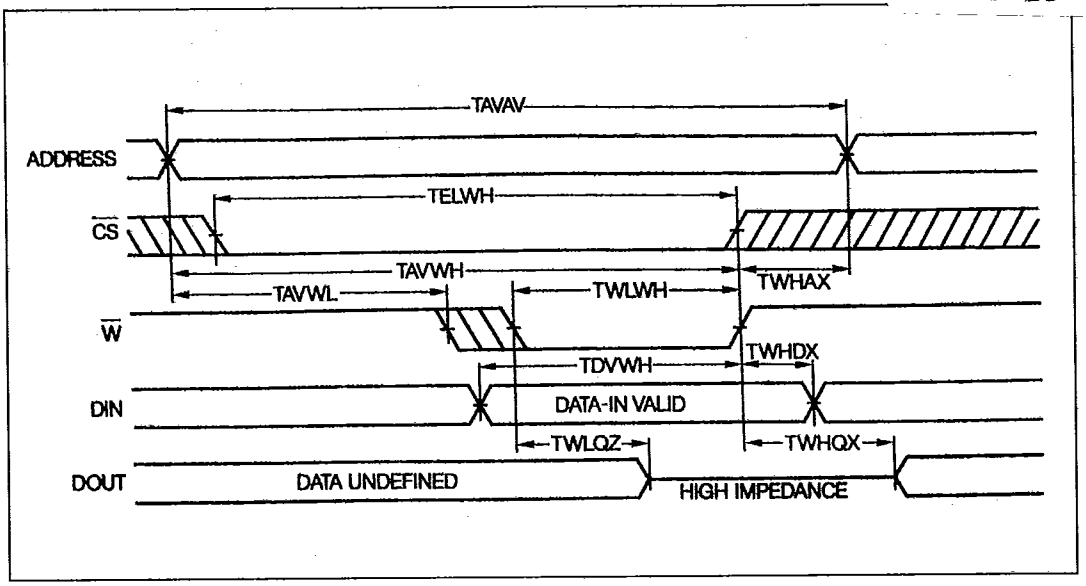
Conditions
- VCC 5V ± 10 %
- Input pulse levels Gnd to 3.ov
- Input rise 5 ns
- Input timing reference levels 1.5V
- Output loading IOL / IOH + 30 pF
- Operating temperature - 55°C to + 125°C

WRITE CYCLE :

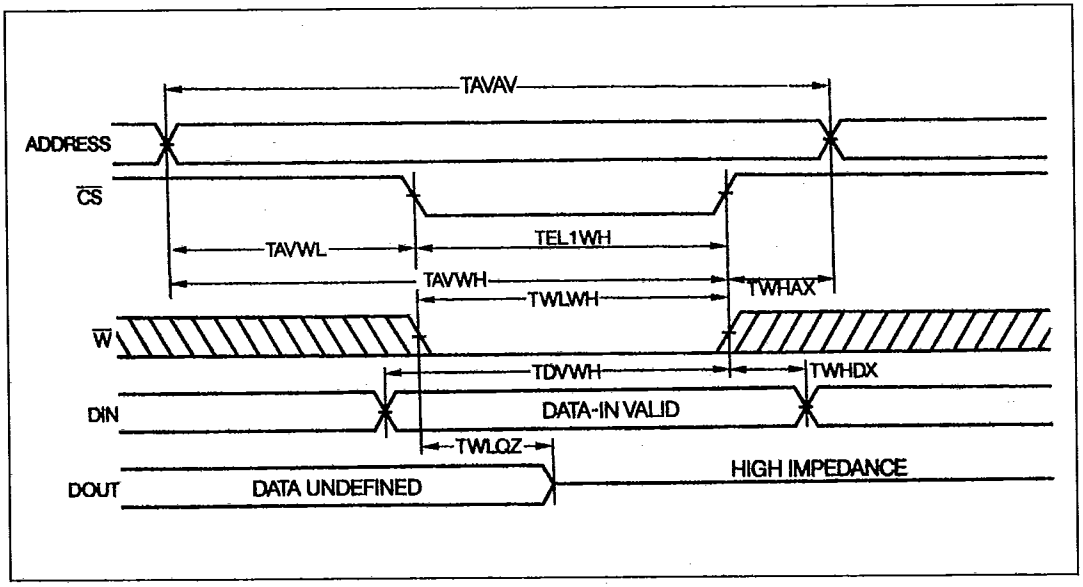
SYMBOL	PARAMETER (8)	65797 H	65797 K	65797 M	65797 N	UNIT	VALUE
TAVAV	Write cycle time	25	35	45	55	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	20	30	40	50	ns	min
TDVWH	Data set-up time	15	17	20	25	ns	min
TELWH	$\overline{CS}$ low to write end	20	30	40	50	ns	min
TWLQZ (7)	Write low to high Z	13	15	20	25	ns	max
TWLWH	Write pulse width	20	25	30	35	ns	min
TWHAX	Address hold to Write end	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (7)	Write high to low Z	3	3	3	3	ns	min

Notes : 7. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. All parameters tested only.
All parameters are screened during full speed functional test.
For subgroups 7 and 8 (functional test).
Tested at 1 MHz with VIL = OV and VIH = 3V.
HM 65797 is verified with differents patterns unit for basic function, latch-up, maximum rating, data-retention.

WRITE CYCLE 1 : $\overline{W}$ Controlled (note 9)



WRITE CYCLE 2 : $\overline{CS}$ Controlled (note 9)



Note : 9. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to rising edge of the signal that terminates the write.

READ CYCLE :

SYMBOL	PARAMETER (8)	65797 H	65797 K	65797 M	65797 N	UNIT	VALUE
TAVAV	Read cycle time	25	35	45	55	ns	min
TAVQV	Address access time	25	35	45	55	ns	max
TAVQX	Address valid to low Z	3	3	3	3	ns	min
TELQV	Chip-select access time	25	35	45	55	ns	max
TELQX	CS low to low Z	3	3	3	3	ns	min
TEHQZ	$\overline{CS}$ high to high Z	13	15	20	20	ns	max
TELIC	CS low to power up	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	20	25	30	35	ns	max

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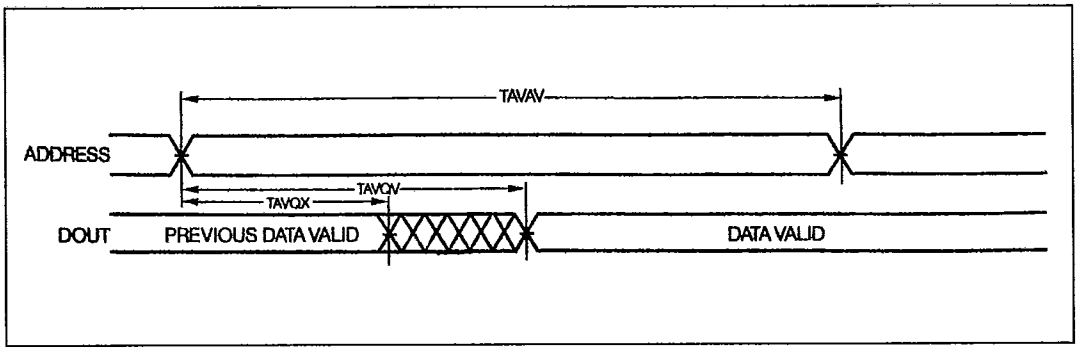
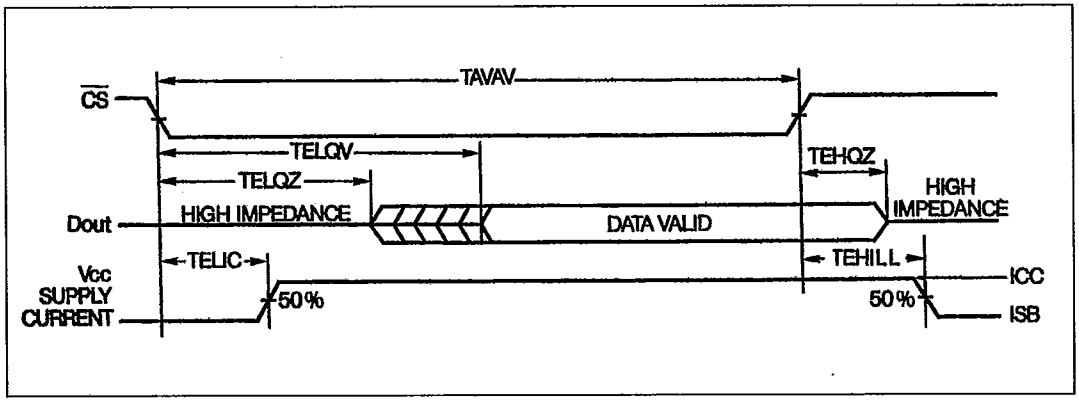
READ CYCLE 1 (note 10, 11, 12)

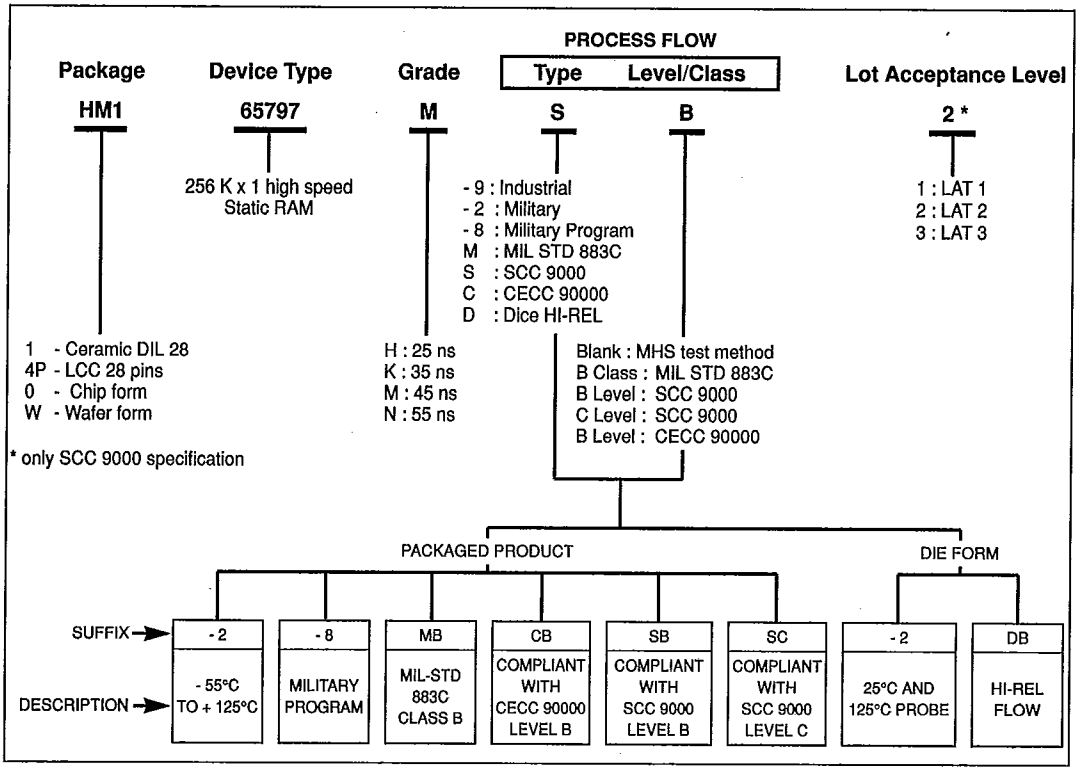


READ CYCLE nb 2 (note 10, 12)



Notes : 10. $\overline{W}$ is HIGH for read cycle.
11. Device is continuously selected $\overline{CS}$ = VIL.
12. Address valid prior to or coincident with $\overline{CS}$ transition low.

ORDERING INFORMATION



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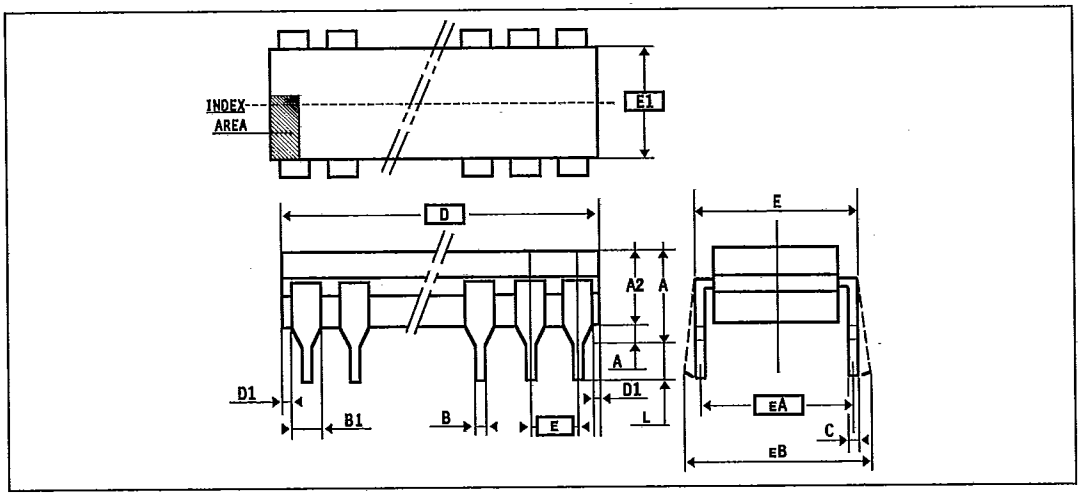
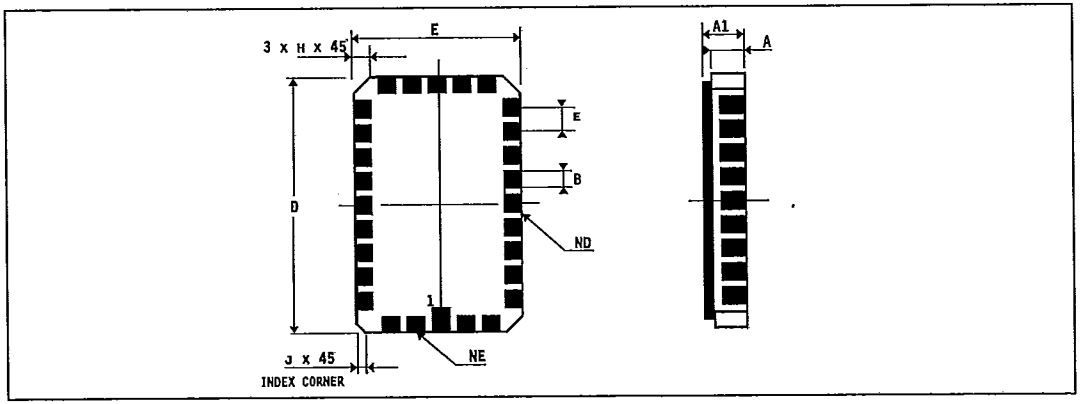
PACKAGE OUTLINES



24 PINS CERDIP .300

		A	A1	A2	B	B1	C	D	D1	E	E1	e	eA	eB	D1
MM	MIN	—	0.50	3.81	0.36	0.76	0.20	31.50	0.76	7.90	7.24	2.54	7.62	—	3.17
	MAX	5.71	—	4.95	—	1.78	0.38	32.26	—	8.38	7.87	BSC	BSC	10.92	5.08
INCHES	MIN	—	.020	.150	.014	.030	.008	1.240	.030	.311	.285	.100	.300	—	.125
	MAX	.225	—	.195	—	.070	.015	1.270	—	.330	.310	BSC	BSC	.430	.200



28 LDS .050 CENTER LEADLESS RECTANGULAR CHIP CARRIER

		A	A1	B	D	E	e	h	j	ND	NE
MM	MIN	1.37	1.62	0.56	13.81	8.74	1.27	0.64	0.38	9	5
	MAX	1.65	2.00	0.71	14.22	9.14	BSC	Ref	Ref		
INCHES	MIN	.054	.064	.022	.544	.344	.050	0.25	.015	9	5
	MAX	.065	.079	.028	.560	.360	BSC	Ref	Ref		