Precision, Very Low Noise, Low Input Bias Current, Wide Bandwidth JFET Operational Amplifier

AD8610/AD8620

FEATURES
Low Noise 6 nV/√Hz
Low Offset Voltage: 100 μV Max
Low Input Bias Current 10 pA Max
Fast Settling: 600 ns to 0.01%
Low Distortion
Unity Gain Stable
No Phase Reversal
Dual-Supply Operation: ±5 V to ±13 V

APPLICATIONS
Photodiode Amplifier
ATE
Instrumentation
Sensors and Controls
High Performance Filters
Fast Precision Integrators
High Performance Audio

FUNCTIONAL BLOCK DIAGRAMS

8-Lead MSOP and SOIC
(RM-8 and R-8 Suffixes)

NC = NO CONNECT

8-Lead SOIC
(R-8 Suffix)

GENERAL DESCRIPTION

The AD8610/AD8620 is a very high precision JFET input amplifier featuring ultralow offset voltage and drift, very low input voltage and current noise, very low input bias current, and wide bandwidth. Unlike many JFET amplifiers, the AD8610/AD8620 input bias current is low over the entire operating temperature range. The AD8610/AD8620 is stable with capacitive loads of over 1000 pF in noninverting unity gain; much larger capacitive loads can be driven easily at higher noise gains. The AD8610/AD8620 swings to within 1.2 V of the supplies even with a 1 kΩ load, maximizing dynamic range even with limited supply voltages. Outputs slew at 50 V/μs in either inverting or noninverting gain configurations, and settle to 0.01% accuracy in less than 600 ns. Combined with the high input impedance, great precision, and very high output drive, the AD8610/AD8620 is an ideal amplifier for driving high performance A/D inputs and buffering D/A converter outputs.

Applications for the AD8610/AD8620 include electronic instruments; ATE amplification, buffering, and integrator circuits; CAT/MRI/ultrasound medical instrumentation; instrumentation quality photodiode amplification; fast precision filters (including PLL filters); and high quality audio.

The AD8610/AD8620 is fully specified over the extended industrial (–40°C to +125°C) temperature range. The AD8610 is available in the narrow 8-lead SOIC and the tiny MSOP8 surface-mount packages. The AD8620 is available in the narrow 8-lead SOIC package. MSOP8 packaged devices are available only in tape and reel.

REV. D

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703

AD8610/AD8620–SPECIFICATIONS (@ V_S = ±5.0 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage (AD8610B)	V_{OS}			45	100	µV
		–40°C < T_A < +125°C		80	200	µV
Offset Voltage (AD8620B)	V_{OS}			45	150	µV
		–40°C < T_A < +125°C		80	300	µV
Offset Voltage (AD8610A/AD8620A)	V_{OS}			85	250	µV
		+25°C < T_A < 125°C		90	350	µV
		–40°C < T_A < +125°C		150	850	µV
Input Bias Current	I_B		–10	+2	+10	pA
		–40°C < T_A < +85°C	–250	+130	+250	pA
		–40°C < T_A < +125°C	–2.5	+1.5	+2.5	nA
Input Offset Current	I_{OS}		–10	+1	+10	pA
		–40°C < T_A < +85°C	–75	+20	+75	pA
		–40°C < T_A < +125°C	–150	+40	+150	pA
Input Voltage Range			–2		+3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = –2.5 V to +1.5 V	90	95		dB
Large Signal Voltage Gain	A_{VO}	R_L = 1 kΩ, V_O = –3 V to +3 V	100	180		V/mV
Offset Voltage Drift (AD8610B)	$\Delta V_{OS}/\Delta T$	–40°C < T_A < +125°C		0.5	1	µV/°C
Offset Voltage Drift (AD8620B)	$\Delta V_{OS}/\Delta T$	–40°C < T_A < +125°C		0.5	1.5	µV/°C
Offset Voltage Drift (AD8610A/AD8620A)	$\Delta V_{OS}/\Delta T$	–40°C < T_A < +125°C		0.8	3.5	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 1 kΩ, –40°C < T_A < +125°C	3.8	4		V
Output Voltage Low	V_{OL}	R_L = 1 kΩ, –40°C < T_A < +125°C		–4	–3.8	V
Output Current	I_{OUT}	V_{OUT} > ±2 V		±30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±5 V to ±13 V	100	110		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		2.5	3.0	mA
		–40°C < T_A < +125°C		3.0	3.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	40	50		V/µs
Gain Bandwidth Product	GBP			25		MHz
Settling Time	t_S	A_V = +1, 4 V Step, to 0.01%		350		ns
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		1.8		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		6		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		5		fA/√Hz
Input Capacitance	C_{IN}					
Differential				8		pF
Common-Mode				15		pF
Channel Separation	C_S					
f = 10 kHz				137		dB
f = 300 kHz				120		dB

Specifications subject to change without notice.

ELECTRICAL SPECIFICATIONS (@ V_S = ±13 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage (AD8610B)	V_{OS}			45	100	µV
		–40°C < T_A < +125°C		80	200	µV
Offset Voltage (AD8620B)	V_{OS}			45	150	µV
		–40°C < T_A < +125°C		80	300	µV
Offset Voltage (AD8610A/AD8620A)	V_{OS}			85	250	µV
		+25°C < T_A < 125°C		90	350	µV
		–40°C < T_A < +125°C		150	850	µV
Input Bias Current	I_B		–10	+3	+10	pA
		–40°C < T_A < +85°C	–250	+130	+250	pA
		–40°C < T_A < +125°C	–3.5		+3.5	nA
Input Offset Current	I_{OS}		–10	+1.5	+10	pA
		–40°C < T_A < +85°C	–75	+20	+75	pA
		–40°C < T_A < +125°C	–150	+40	+150	pA
Input Voltage Range			–10.5		+10.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = –10 V to +10 V	90	110		dB
Large Signal Voltage Gain	A_{VO}	R_L = 1 kΩ, V_O = –10 V to +10 V	100	200		V/mV
Offset Voltage Drift (AD8610B)	$\Delta V_{OS}/\Delta T$	–40°C < T_A < +125°C		0.5	1	µV/°C
Offset Voltage Drift (AD8620B)	$\Delta V_{OS}/\Delta T$	–40°C < T_A < +125°C		0.5	1.5	µV/°C
Offset Voltage Drift (AD8610A/AD8620A)	$\Delta V_{OS}/\Delta T$	–40°C < T_A < +125°C		0.8	3.5	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 1 kΩ, –40°C < T_A < +125°C	+11.75	+11.84		V
Output Voltage Low	V_{OL}	R_L = 1 kΩ, –40°C < T_A < +125°C		–11.84	–11.75	V
Output Current	I_{OUT}	V_{OUT} > 10 V		±45		mA
Short Circuit Current	I_{SC}			±65		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±5 V to ±13 V	100	110		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		3.0	3.5	mA
		–40°C < T_A < +125°C		3.5	4.0	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	40	60		V/µs
Gain Bandwidth Product	GBP			25		MHz
Settling Time	t_S	A_V = 1, 10 V Step, to 0.01%		600		ns
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		1.8		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		6		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		5		fA/√Hz
Input Capacitance	C_{IN}					
Differential				8		pF
Common-Mode				15		pF
Channel Separation	C_S					
f = 10 kHz				137		dB
f = 300 kHz				120		dB

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . 27.3 V
Input Voltage . . . . . V_{S-} to V_{S+}
Differential Input Voltage . . . . . ± Supply Voltage
Output Short-Circuit Duration to GND . . . . . Indefinite
Storage Temperature Range
R, RM Packages . . . . . –65°C to +150°C
Operating Temperature Range
AD8610/AD8620 . . . . . –40°C to +125°C
Junction Temperature Range
R, RM Packages . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 10 sec) . . . . . 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Type	θ_{JA}*	θ_{JC}	Unit
8-Lead MSOP (RM)	190	44	°C/W
8-Lead SOIC (RN)	158	43	°C/W

*θ_{JA} is specified for worst-case conditions; i.e., θ_{JA} is specified for a device soldered in circuit board for surface-mount packages.

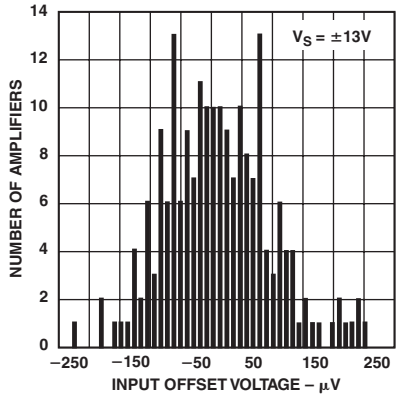
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8610AR	–40°C to +125°C	8-Lead SOIC	RN-8	
AD8610AR-REEL	–40°C to +125°C	8-Lead SOIC	RN-8	
AD8610AR-REEL7	–40°C to +125°C	8-Lead SOIC	RN-8	
AD8610ARM-REEL	–40°C to +125°C	8-Lead MSOP	RM-8	B0A
AD8610ARM-R2	–40°C to +125°C	8-Lead MSOP	RM-8	B0A
AD8610ARZ*	–40°C to +125°C	8-Lead SOIC	RN-8	
AD8610ARZ-REEL*	–40°C to +125°C	8-Lead SOIC	RN-8	
AD8610ARZ-REEL7*	–40°C to +125°C	8-Lead SOIC	RN-8	
AD8610BR	–40°C to +125°C	8-Lead SOIC	RN-8	
AD8610BR-REEL	–40°C to +125°C	8-Lead SOIC	RN-8	
AD8610BR-REEL7	–40°C to +125°C	8-Lead SOIC	RN-8	
AD8610BRZ*	–40°C to +125°C	8-Lead SOIC	RN-8	
AD8610BRZ-REEL*	–40°C to +125°C	8-Lead SOIC	RN-8	
AD8610BRZ-REEL7*	–40°C to +125°C	8-Lead SOIC	RN-8	
AD8620AR	–40°C to +125°C	8-Lead SOIC	RN-8	
AD8620AR-REEL	–40°C to +125°C	8-Lead SOIC	RN-8	
AD8620AR-REEL7	–40°C to +125°C	8-Lead SOIC	RN-8	
AD8620BR	–40°C to +125°C	8-Lead SOIC	RN-8	
AD8620BR-REEL	–40°C to +125°C	8-Lead SOIC	RN-8	
AD8620BR-REEL7	–40°C to +125°C	8-Lead SOIC	RN-8	

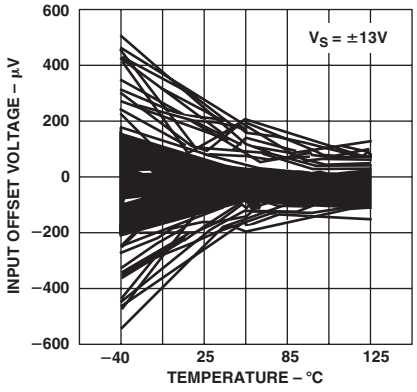
*Pb-free part

CAUTION

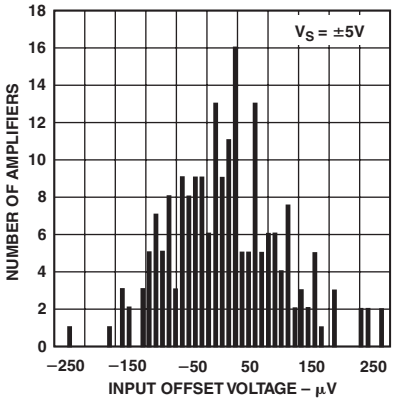
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8610/AD8620 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



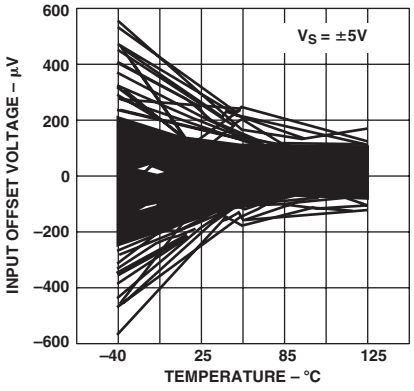
TPC 1. Input Offset Voltage at ±13 V



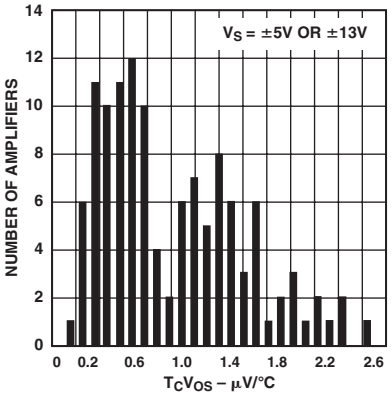
TPC 2. Input Offset Voltage vs. Temperature at ±13 V (300 Amplifiers)



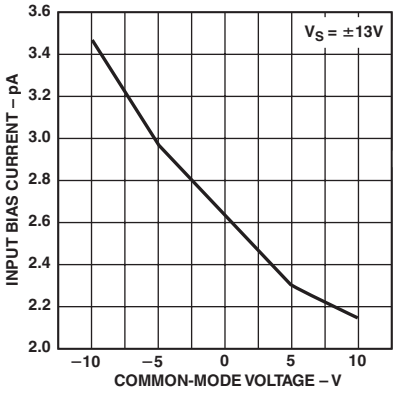
TPC 3. Input Offset Voltage at ±5 V



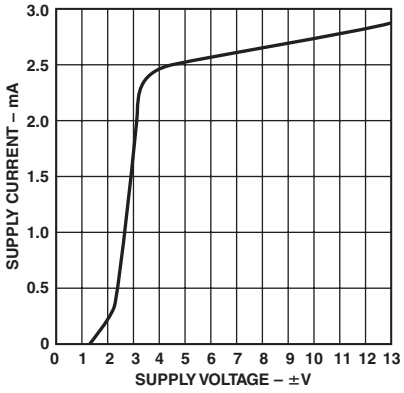
TPC 4. Input Offset Voltage vs. Temperature at ±5 V (300 Amplifiers)



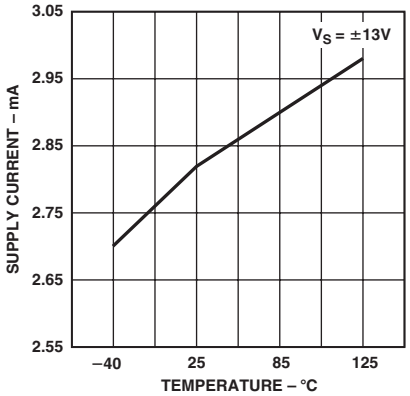
TPC 5. Input Offset Voltage Drift



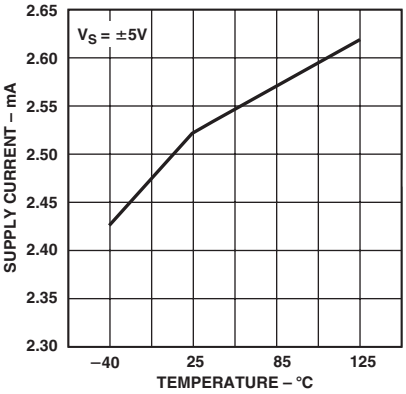
TPC 6. Input Bias Current vs. Common-Mode Voltage



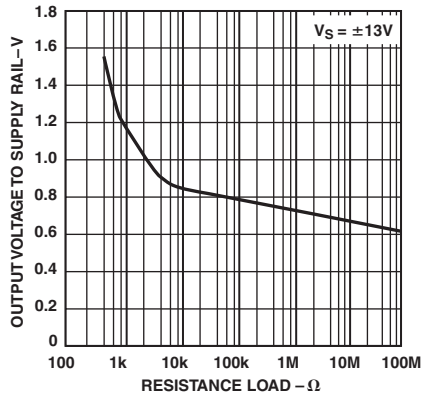
TPC 7. Supply Current vs. Supply Voltage



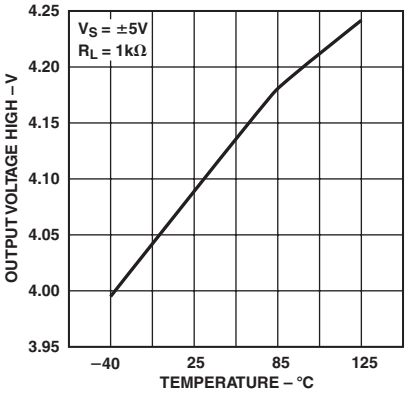
TPC 8. Supply Current vs. Temperature at ±13 V



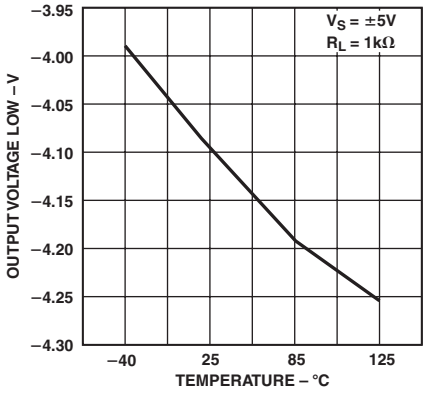
TPC 9. Supply Current vs. Temperature at ±5 V



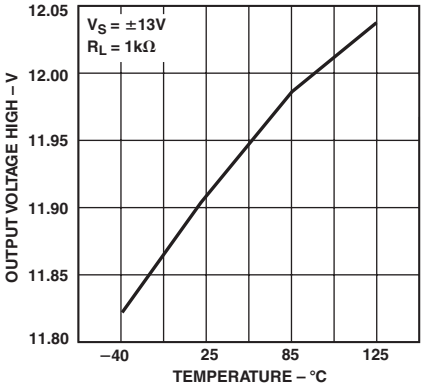
TPC 10. Output Voltage to Supply Rail vs. Load



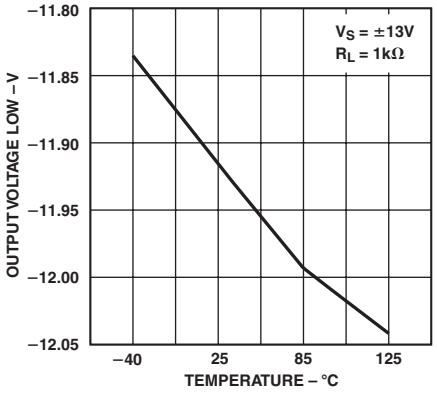
TPC 11. Output Voltage High vs. Temperature at ±5 V



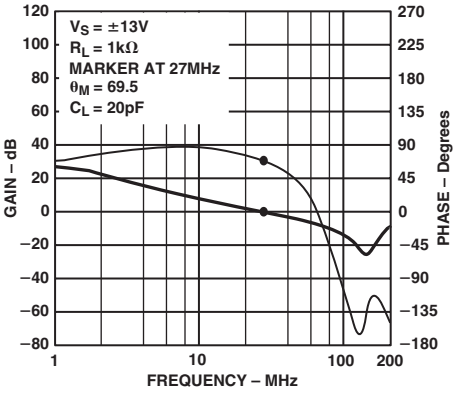
TPC 12. Output Voltage Low vs. Temperature at ±5 V



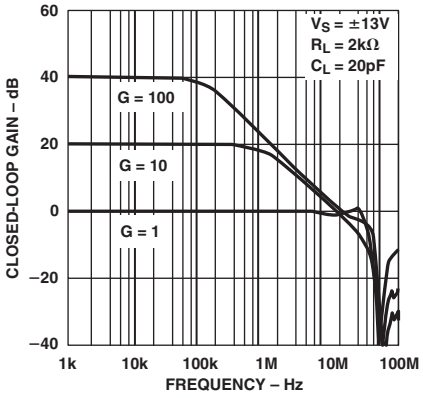
TPC 13. Output Voltage High vs. Temperature at ±13 V



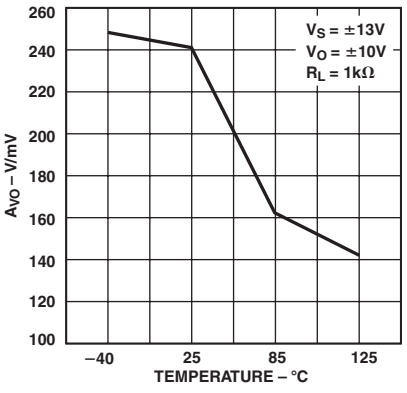
TPC 14. Output Voltage Low vs. Temperature at ±13 V



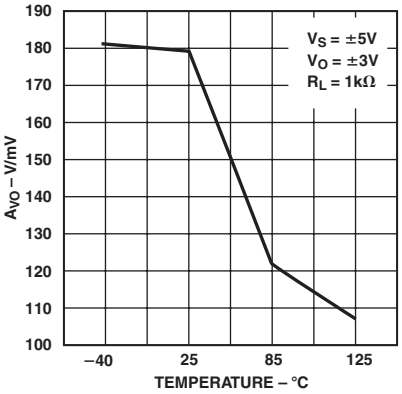
TPC 15. Open-Loop Gain and Phase vs. Frequency



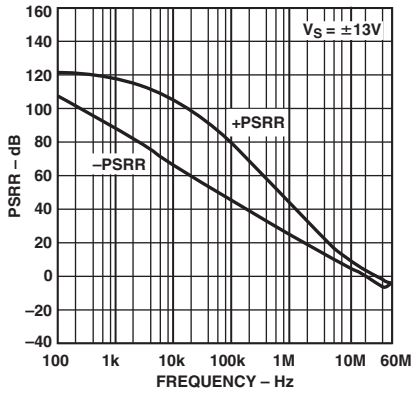
TPC 16. Closed-Loop Gain vs. Frequency



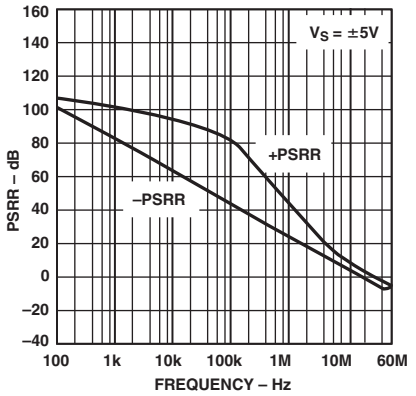
TPC 17. A_{VO} vs. Temperature at ±13 V



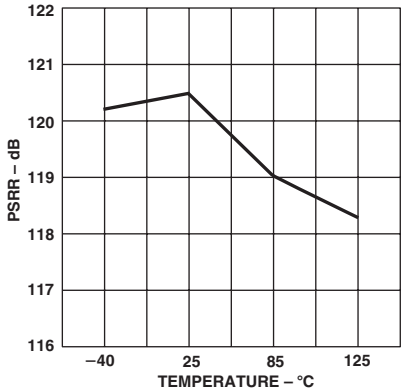
TPC 18. A_{VO} vs. Temperature at ±5 V



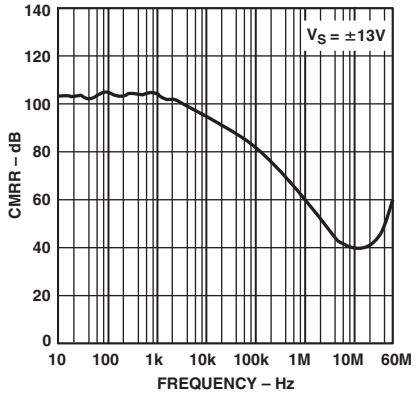
TPC 19. PSRR vs. Frequency at ±13 V



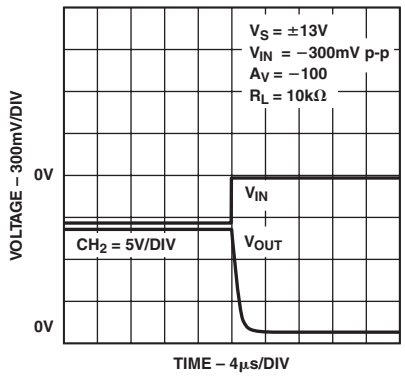
TPC 20. PSRR vs. Frequency at ±5 V



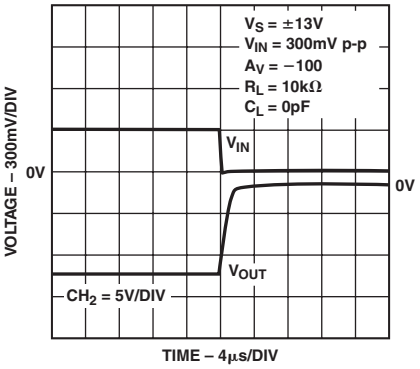
TPC 21. PSRR vs. Temperature



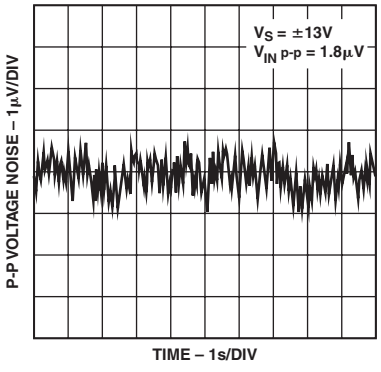
TPC 22. CMRR vs. Frequency



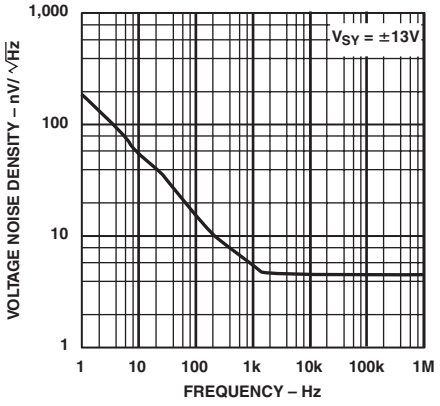
TPC 23. Positive Overvoltage Recovery



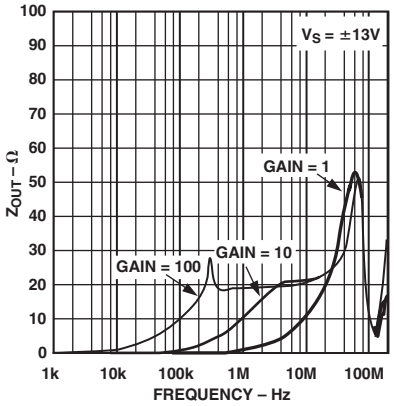
TPC 24. Negative Overvoltage Recovery



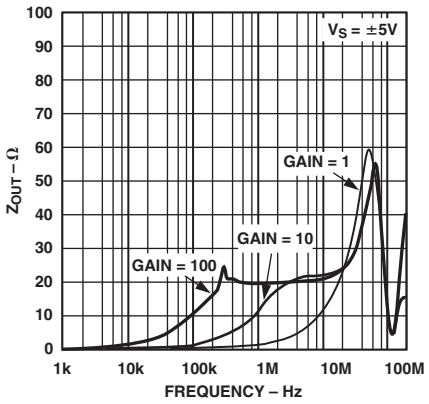
TPC 25. 0.1 Hz to 10 Hz Input Voltage Noise



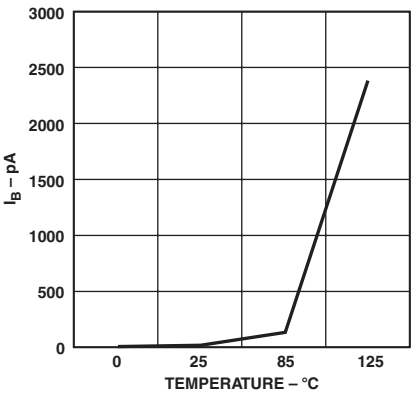
TPC 26. Input Voltage Noise vs. Frequency



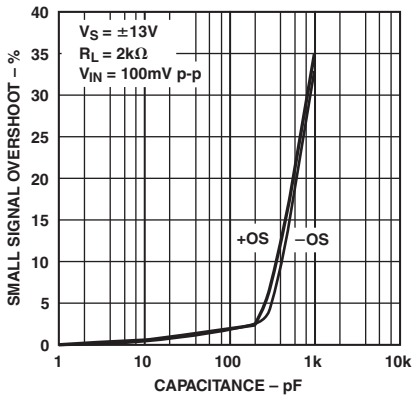
TPC 27. Z_{OUT} vs. Frequency



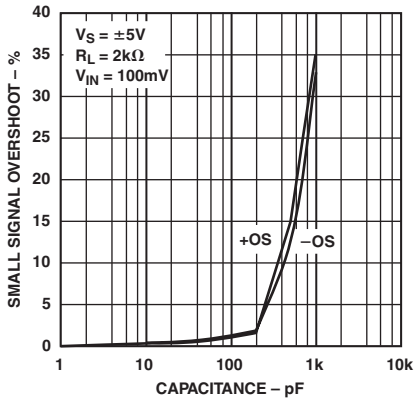
TPC 28. Z_{OUT} vs. Frequency



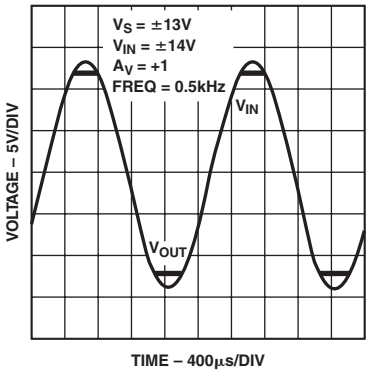
TPC 29. Input Bias Current vs. Temperature



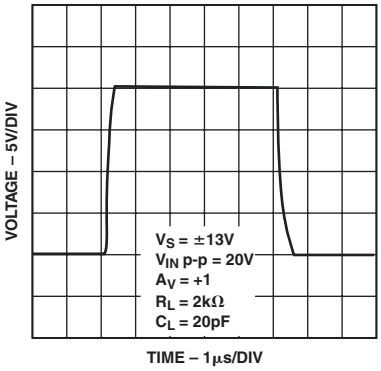
TPC 30. Small Signal Overshoot vs. Load Capacitance



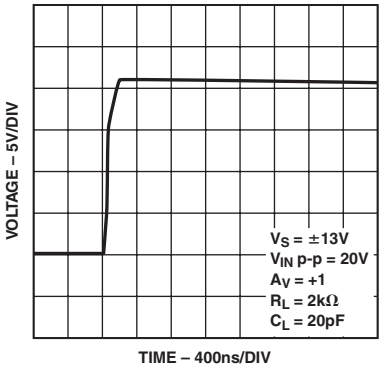
TPC 31. Small Signal Overshoot vs. Load Capacitance



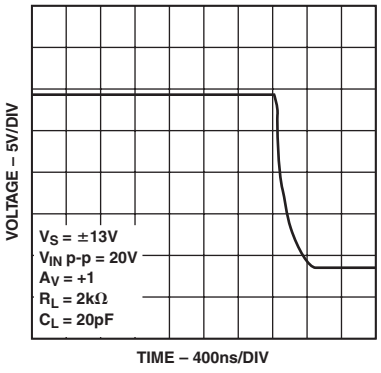
TPC 32. No Phase Reversal



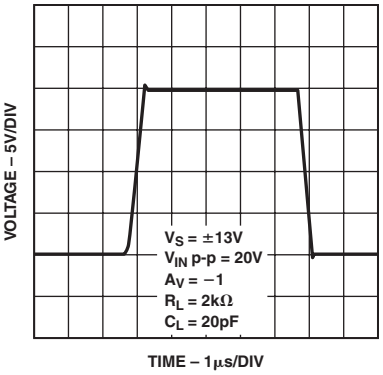
TPC 33. Large Signal Response at G = +1



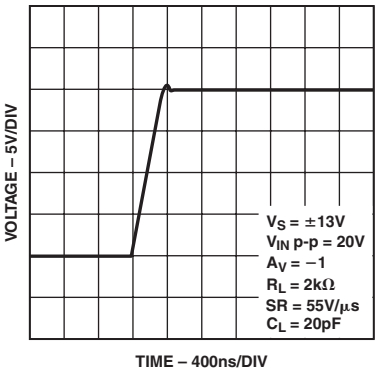
TPC 34. +SR at G = +1



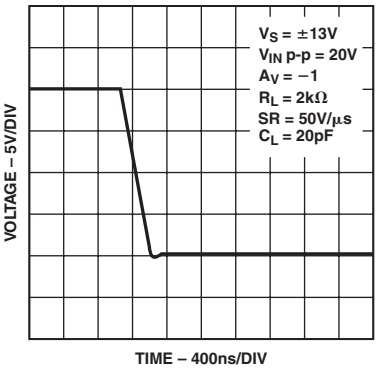
TPC 35. –SR at G = +1



TPC 36. Large Signal Response at G = –1



TPC 37. +SR at G = –1



TPC 38. –SR at G = –1

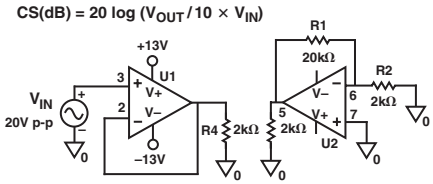


Figure 1. Channel Separation Test Circuit

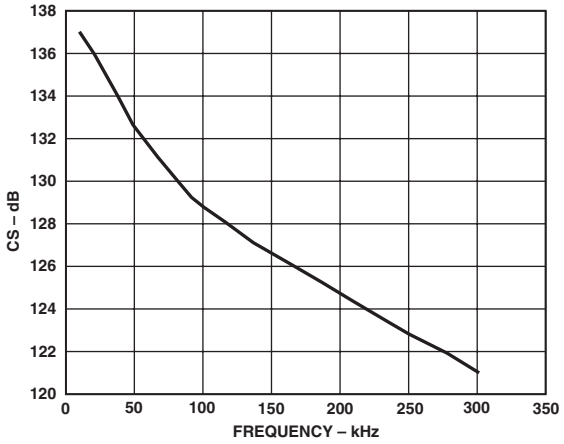


Figure 2. AD8620 Channel Separation Graph

FUNCTIONAL DESCRIPTION

The AD8610/AD8620 is manufactured on Analog Devices, Inc.'s proprietary XFCB (eXtra Fast Complementary Bipolar) process. XFCB is fully dielectrically isolated (DI) and used in conjunction with N-channel JFET technology and trimmable thin-film resistors to create the world's most precise JFET input amplifier. Dielectrically isolated NPN and PNP transistors fabricated on XFCB have F_T greater than 3 GHz. Low T_C thin film resistors enable very accurate offset voltage and offset voltage tempco trimming. These process breakthroughs allowed Analog Devices' world class IC designers to create an amplifier with faster slew rate and more than 50% higher bandwidth at half of the current consumed by its closest competition. The AD8610 is unconditionally stable in all gains, even with capacitive loads well in excess of 1 nF. The AD8610B achieves less than 100 µV of offset and 1 µV/°C of offset drift, numbers usually associated with very high precision bipolar input amplifiers. The AD8610 is offered in the tiny 8-lead MSOP as well as narrow 8-lead SOIC surface-mount packages and is fully specified with supply voltages from ±5 V to ±13 V. The very wide specified temperature range, up to 125°C, guarantees superior operation in systems with little or no active cooling.

The unique input architecture of the AD8610 features extremely low input bias currents and very low input offset voltage. Low power consumption minimizes the die temperature and maintains the very low input bias current. Unlike many competitive JFET amplifiers, the AD8610/AD8620 input bias currents are low even at elevated temperatures. Typical bias currents are less than 200 pA at 85°C. The gate current of a JFET doubles every 10°C resulting in a similar increase in input bias current over temperature. Special care should be given to the PC board layout to minimize leakage currents between PCB traces. Improper layout and board handling generates leakage current that exceeds the bias current of the AD8610/AD8620.

Power Consumption

A major advantage of the AD8610/AD8620 in new designs is the saving of power. Lower power consumption of the AD8610 makes it much more attractive for portable instrumentation and for high-density systems, simplifying thermal management, and reducing power supply performance requirements. Compare the power consumption of the AD8610/AD8620 versus the OPA627 in Figure 3.

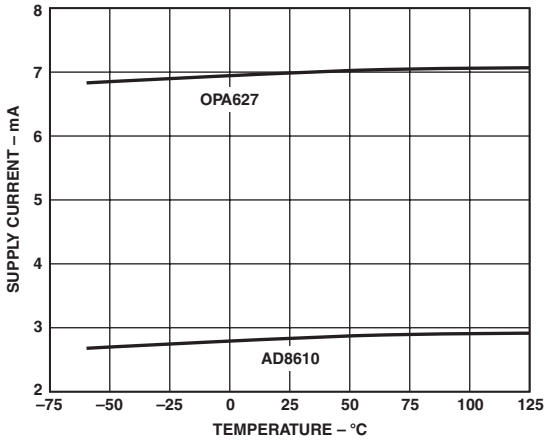


Figure 3. Supply Current vs. Temperature

Driving Large Capacitive Loads

The AD8610 has excellent capacitive load driving capability and can safely drive up to 10 nF when operating with ±5 V supply. Figures 4 and 5 compare the AD8610/AD8620 against the OPA627 in the noninverting gain configuration driving a 10 kΩ resistor and 10,000 pF capacitor placed in parallel on its output, with a square wave input set to a frequency of 200 kHz. The AD8610 has much less ringing than the OPA627 with heavy capacitive loads.

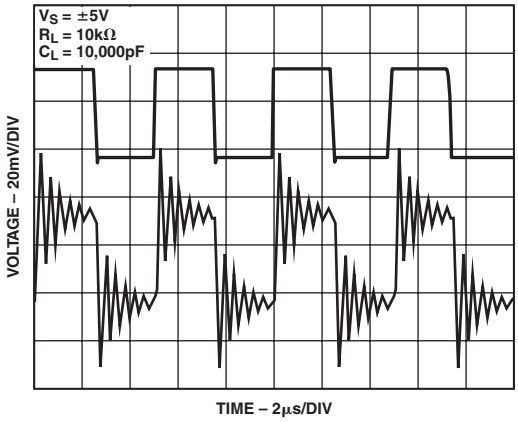


Figure 4. OPA627 Driving C_L = 10,000 pF

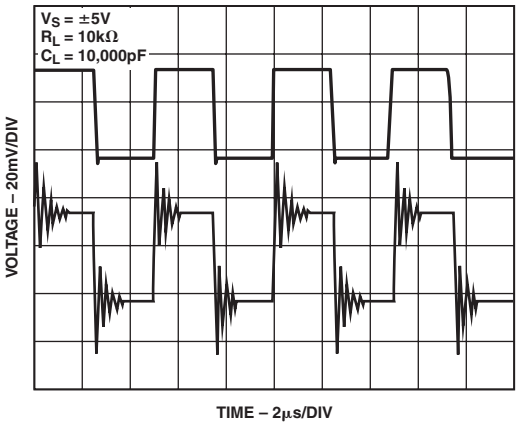


Figure 5. AD8610/AD8620 Driving C_L = 10,000 pF

The AD8610/AD8620 can drive much larger capacitances without any external compensation. Although the AD8610/AD8620 is stable with very large capacitive loads, remember that this capacitive loading will limit the bandwidth of the amplifier. Heavy capacitive loads will also increase the amount of overshoot and ringing at the output. Figures 7 and 8 show the AD8610/AD8620 and the OPA627 in a noninverting gain of +2 driving 2 μF of capacitance load. The ringing on the OPA627 is much larger in magnitude and continues more than 10 times longer than the AD8610.

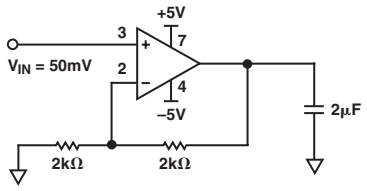


Figure 6. Capacitive Load Drive Test Circuit

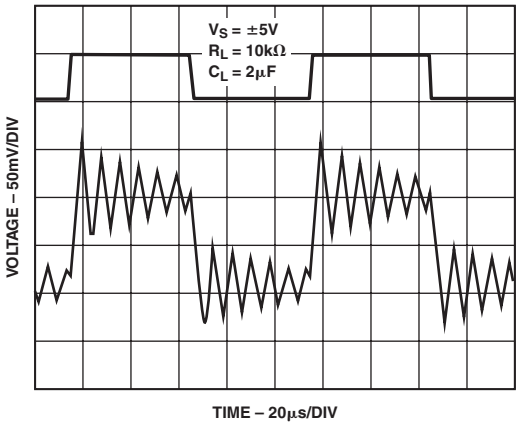


Figure 7. OPA627 Capacitive Load Drive, A_V = +2

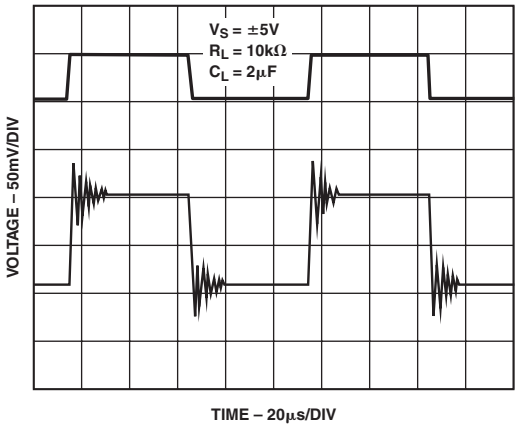


Figure 8. AD8610/AD8620 Capacitive Load Drive, A_V = +2

Slew Rate (Unity Gain Inverting vs. Noninverting)

Amplifiers generally have a faster slew rate in an inverting unity gain configuration due to the absence of the differential input capacitance. Figures 9 through 12 show the performance of the AD8610 configured in a gain of –1 compared to the OPA627. The AD8610 slew rate is more symmetrical, and both the positive and negative transitions are much cleaner than in the OPA627.

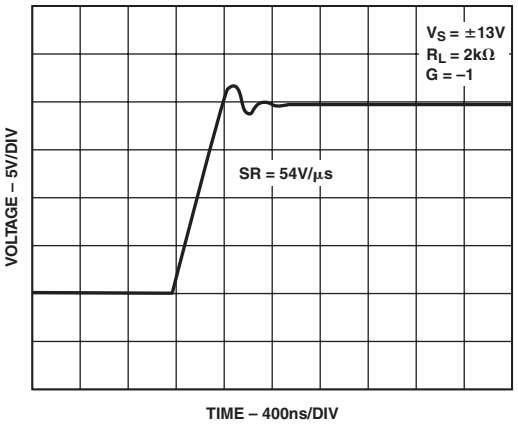


Figure 9. (+SR) of AD8610/AD8620 in Unity Gain of –1

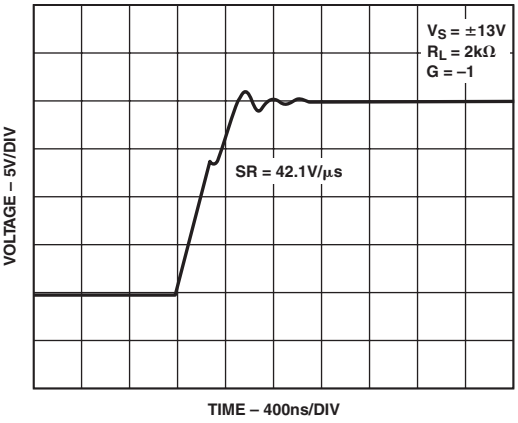


Figure 10. (+SR) of OPA627 in Unity Gain of –1

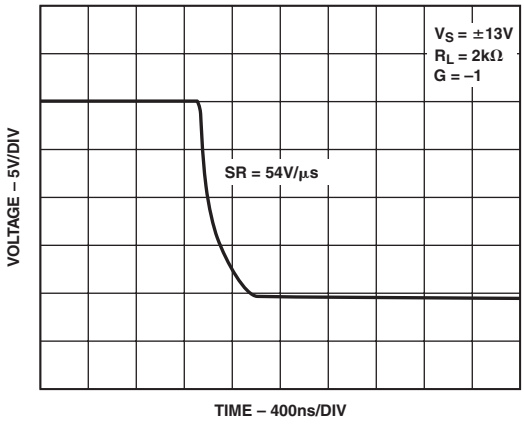


Figure 11. (–SR) of AD8610/AD8620 in Unity Gain of –1

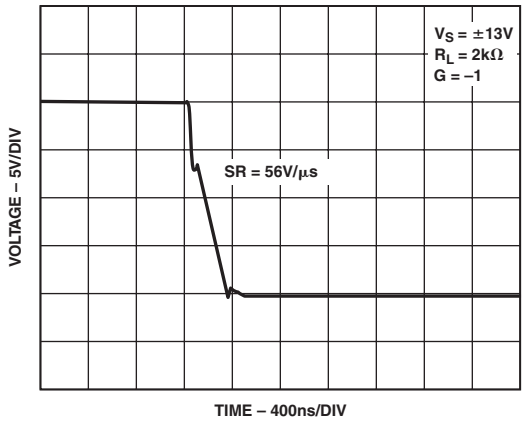


Figure 12. (–SR) of OPA627 in Unity Gain of –1

The AD8610 has a very fast slew rate of 60 V/μs even when configured in a noninverting gain of +1. This is the toughest condition to impose on any amplifier since the input common-mode capacitance of the amplifier generally makes its SR appear worse. The slew rate of an amplifier varies according to the voltage difference between its two inputs. To observe the maximum SR as specified in the AD8610 data sheet, a difference voltage of about 2 V between the inputs must be ensured. This will be required for virtually any JFET op amp so that one side of the op amp input circuit is completely off, maximizing the current available to charge and discharge the internal compensation capacitance. Lower differential drive voltages will produce lower slew rate readings. A JFET-input op amp with a slew rate of 60 V/μs at unity gain with V_{IN} = 10 V might slew at 20 V/μs if it is operated at a gain of +100 with V_{IN} = 100 mV.

The slew rate of the AD8610/AD8620 is double that of the OPA627 when configured in a unity gain of +1 (see Figures 13 and 14).

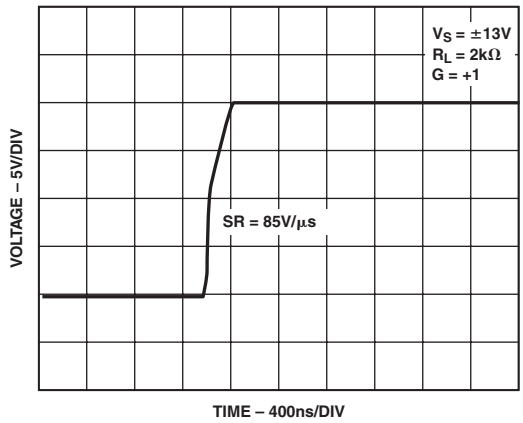


Figure 13. (+SR) of AD8610/AD8620 in Unity Gain of +1

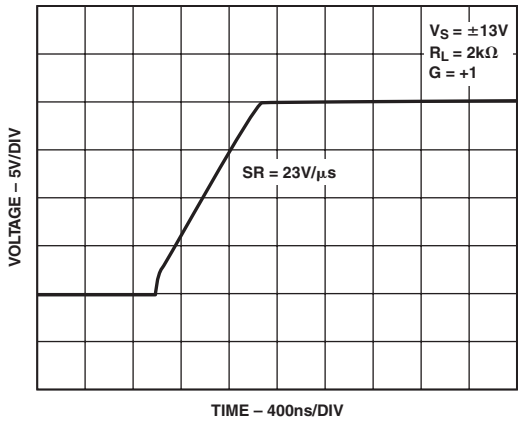


Figure 14. (+SR) of OPA627 in Unity Gain of +1

The slew rate of an amplifier determines the maximum frequency at which it can respond to a large signal input. This frequency (known as full-power bandwidth, or FPBW) can be calculated from the equation:

$$FPBW = \frac{SR}{\left(2\pi \times V_{PEAK}\right)}$$

for a given distortion (e.g., 1%).

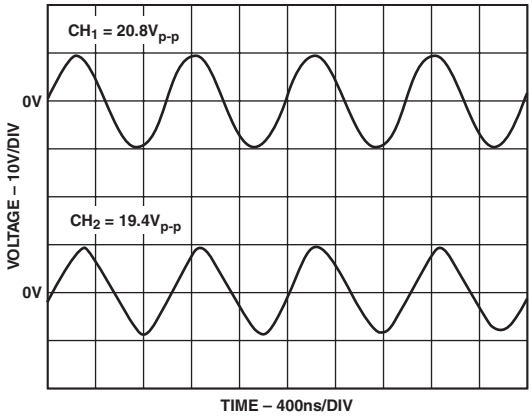


Figure 15. AD8610 FPBW

Input Overvoltage Protection

When the input of an amplifier is driven below V_{EE} or above V_{CC} by more than one V_{BE}, large currents will flow from the substrate through the negative supply (V–) or the positive supply (V+), respectively, to the input pins, which can destroy the device. If the input source can deliver larger currents than the maximum forward current of the diode (>5 mA), a series resistor can be added to protect the inputs. With its very low input bias and offset current, a large series resistor can be placed in front of the AD8610 inputs to limit current to below damaging levels. Series resistance of 10 kΩ will generate less than 25 μV of offset. This 10 kΩ will allow input voltages more than 5 V beyond either power supply. Thermal noise generated by the resistor will add 7.5 nV/√Hz to the noise of the AD8610. For the AD8610/AD8620, differential voltages equal to the supply voltage will not cause any problem (see Figure 15). In this context, it should also be noted that the high breakdown voltage of the input FETs eliminates the need to include clamp diodes between the inputs of the amplifier, a practice that is mandatory on many precision op amps. Unfortunately, clamp diodes greatly interfere with many application circuits such as precision rectifiers and comparators. The AD8610 is free from these limitations.

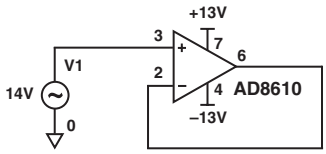


Figure 16. Unity Gain Follower

No Phase Reversal

Many amplifiers misbehave when one or both of the inputs are forced beyond the input common-mode voltage range. Phase reversal is typified by the transfer function of the amplifier, effectively reversing its transfer polarity. In some cases, this can cause lockup and even equipment damage in servo systems, and may cause permanent damage or nonrecoverable parameter shifts to the amplifier itself. Many amplifiers feature compensation circuitry to combat these effects, but some are only effective for the inverting input. The AD8610/AD8620 is designed to prevent phase reversal when one or both inputs are forced beyond their input common-mode voltage range.

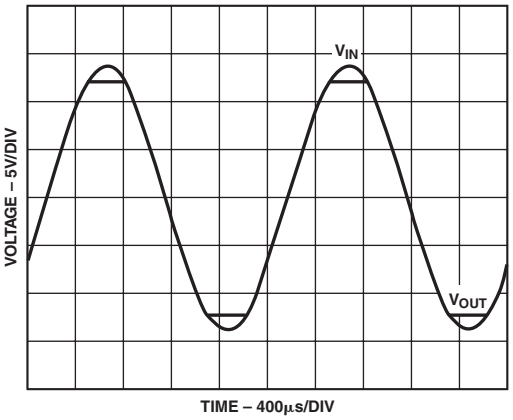


Figure 17. No Phase Reversal

THD Readings vs. Common-Mode Voltage

Total harmonic distortion of the AD8610/AD8620 is well below 0.0006% with any load down to 600 Ω. The AD8610/AD8620 outperforms the OPA627 for distortion, especially at frequencies above 20 kHz.

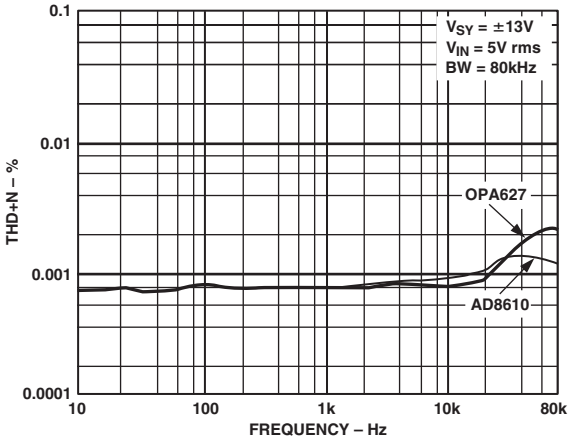


Figure 18. AD8610 vs. OPA627 THD + Noise @ V_{CM} = 0 V

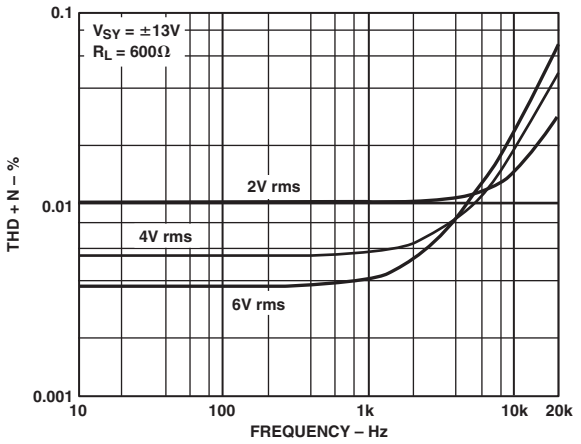


Figure 19. THD + Noise vs. Frequency

Noise vs. Common-Mode Voltage
AD8610 noise density varies only 10% over the input range as shown in Table I.

Table I. Noise vs. Common-Mode Voltage

V_{CM} at F = 1 kHz (V)	Noise Reading (nV/√Hz)
–10	7.21
–5	6.89
0	6.73
+5	6.41
+10	7.21

Settling Time
The AD8610 has a very fast settling time, even to a very tight error band, as can be seen from Figure 20. The AD8610 is configured in an inverting gain of +1 with 2 kΩ input and feedback resistors. The output is monitored with a 10×, 10 M, 11.2 pF scope probe.

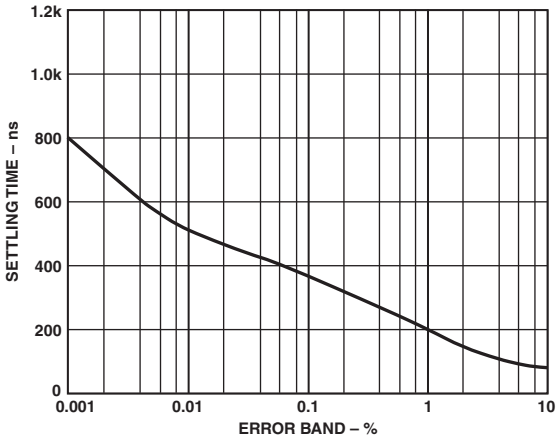


Figure 20. AD8610 Settling Time vs. Error Band

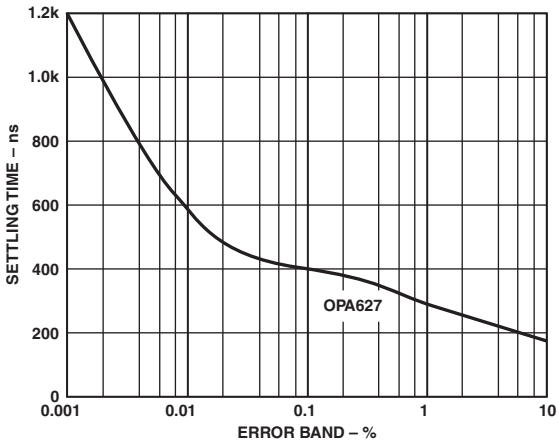


Figure 21. OPA627 Settling Time vs. Error Band

The AD8610/AD8620 maintains this fast settling when loaded with large capacitive loads as shown in Figure 22.

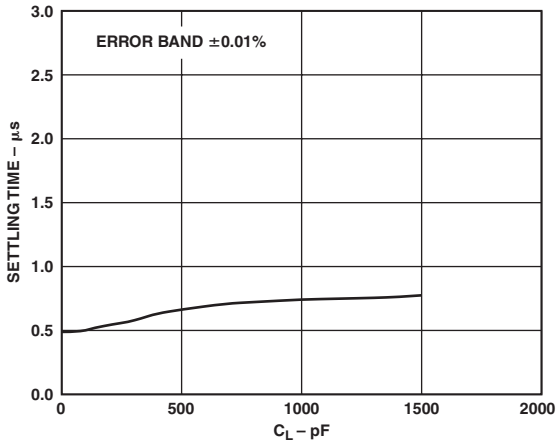


Figure 22. AD8610 Settling Time vs. Load Capacitance

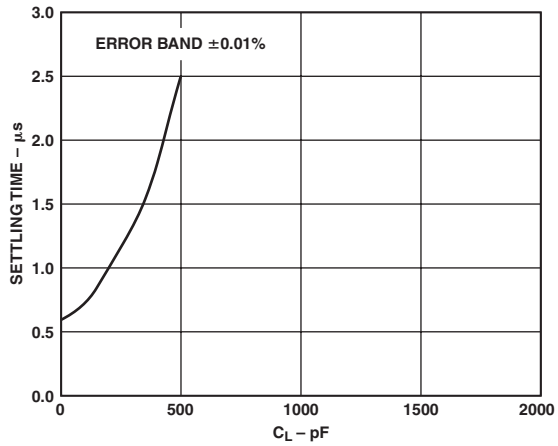


Figure 23. OPA627 Settling Time vs. Load Capacitance

Output Current Capability
The AD8610 can drive very heavy loads due to its high output current. It is capable of sourcing or sinking 45 mA at ±10 V output. The short circuit current is quite high and the part is capable of sinking about 95 mA and sourcing over 60 mA while operating with

supplies of ±5 V. Figures 24 and 25 compare the load current versus output voltage of AD8610/AD8620 and OPA627.

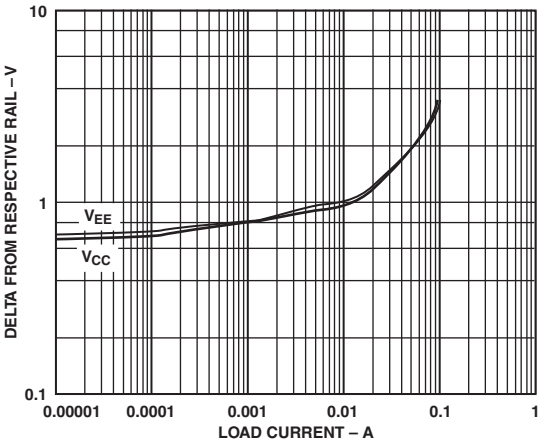


Figure 24. AD8610 Dropout from ±13 V vs. Load Current

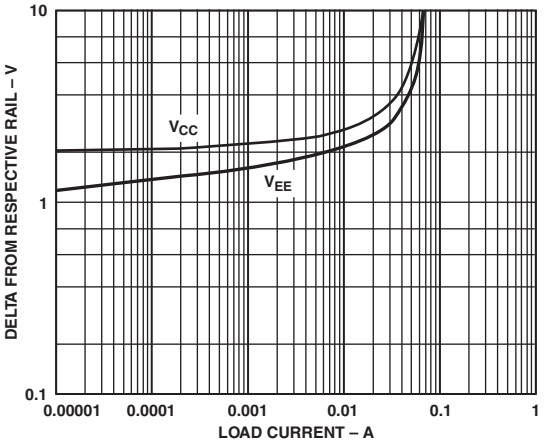


Figure 25. OPA627 Dropout from ±15 V vs. Load Current

Although operating conditions imposed on the AD8610 (±13 V) are less favorable than the OPA627 (±15 V), it can be seen that the AD8610 has much better drive capability (lower headroom to the supply) for a given load current.

Operating with Supplies Greater than ±13 V

The AD8610 maximum operating voltage is specified at ±13 V. When ±13 V is not readily available, an inexpensive LDO can provide ±12 V from a nominal ±15 V supply.

Input Offset Voltage Adjustment

Offset of AD8610 is very small and normally does not require additional offset adjustment. However, the offset adjust pins can be used as shown in Figure 26 to further reduce the dc offset. By using resistors in the range of 50 kΩ, offset trim range is ±3.3 mV.

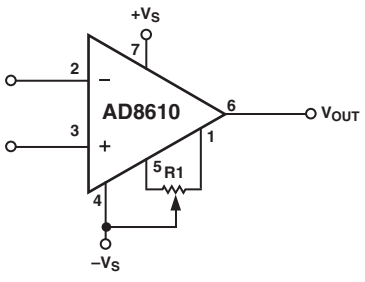


Figure 26. Offset Voltage Nulling Circuit

Programmable Gain Amplifier (PGA)

The combination of low noise, low input bias current, low input offset voltage, and low temperature drift make the AD8610 a perfect solution for programmable gain amplifiers. PGAs are often used immediately after sensors to increase the dynamic range of the measurement circuit. Historically, the large ON resistance of switches, combined with the large I_B currents of amplifiers, created a large dc offset in PGAs. Recent and improved monolithic switches and amplifiers completely remove these problems. A PGA discrete circuit is shown in Figure 27. In Figure 27, when the 10 pA bias current of the AD8610 is dropped across the (<5 Ω) R_{ON} of the switch, it results in a negligible offset error.

When high precision resistors are used, as in the circuit of Figure 27, the error introduced by the PGA is within the 1/2 LSB requirement for a 16-bit system.

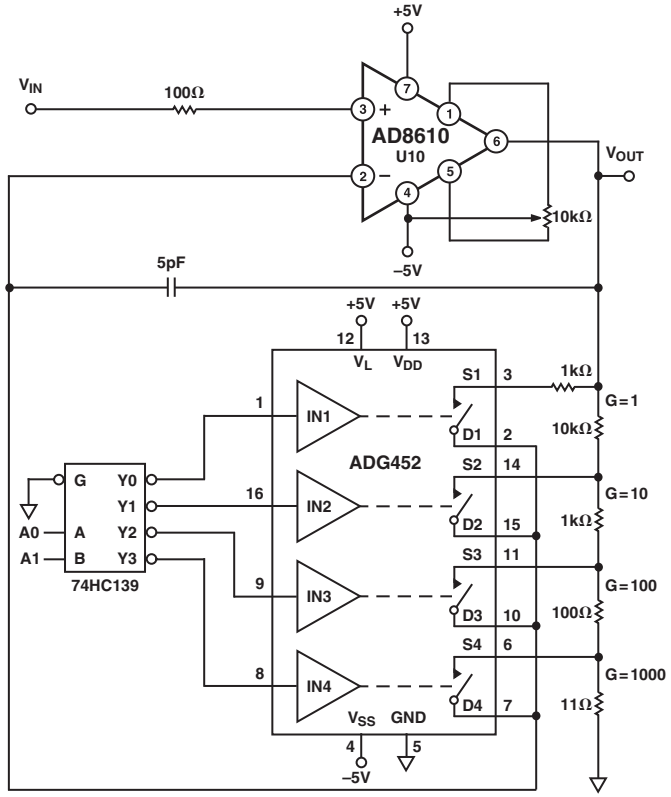


Figure 27. High Precision PGA

1. Room temperature error calculation due to R_{ON} and I_B:

$$\Delta V_{OS} = I_B \times R_{ON} = 2\,\text{pA} \times 5\ \Omega = 10\,\text{pV}$$
$$Total\ \ Offset = AD8610(Offset) + \Delta V_{OS}$$
$$Total\ \ Offset = AD8610(Offset\_Trimmed) + \Delta V_{OS}$$
$$Total\ \ Offset = 5\ \mu\text{V} + 10\,\text{pV} \cong 5\ \mu\text{V}$$

2. Full temperature error calculation due to R_{ON} and I_B:

$$\Delta V_{OS}(@85°\text{C}) = I_B(@85°\text{C}) \times R_{ON}(@85°\text{C}) =$$
$$250\ \text{pA} \times 15\ \Omega = 3.75\ \text{nV}$$

3. Temperature coefficient of switch and AD8610/AD8620 combined is essentially the same as the $T_C V_{OS}$ of the AD8610:

$$\Delta V_{OS}/\Delta T(total) = \Delta V_{OS}/\Delta T(AD8610) + \Delta V_{OS}/\Delta T(I_B \times R_{ON})$$
$$\Delta V_{OS}/\Delta T(total) = 0.5\ \mu\text{V}/°\text{C} + 0.06\ \text{nV}/°\text{C} \cong 0.5\ \mu\text{V}/°\text{C}$$

High Speed Instrumentation Amplifier (IN AMP)

The three op amp instrumentation amplifiers shown in Figure 28 can provide a range of gains from unity up to 1,000 or higher. The instrumentation amplifier configuration features high common-mode rejection, balanced differential inputs, and stable, accurately defined gain. Low input bias currents and fast settling are achieved with the JFET input AD8610/AD8620. Most instrumentation amplifiers cannot match the high frequency performance of this circuit. The circuit bandwidth is 25 MHz at a gain of 1, and close to 5 MHz at a gain of 10. Settling time for the entire circuit is 550 ns to 0.01% for a 10 V step (gain = 10). Note that the resistors around the input pins need to be small enough in value so that the RC time constant they form in combination with stray circuit capacitance does not reduce circuit bandwidth.

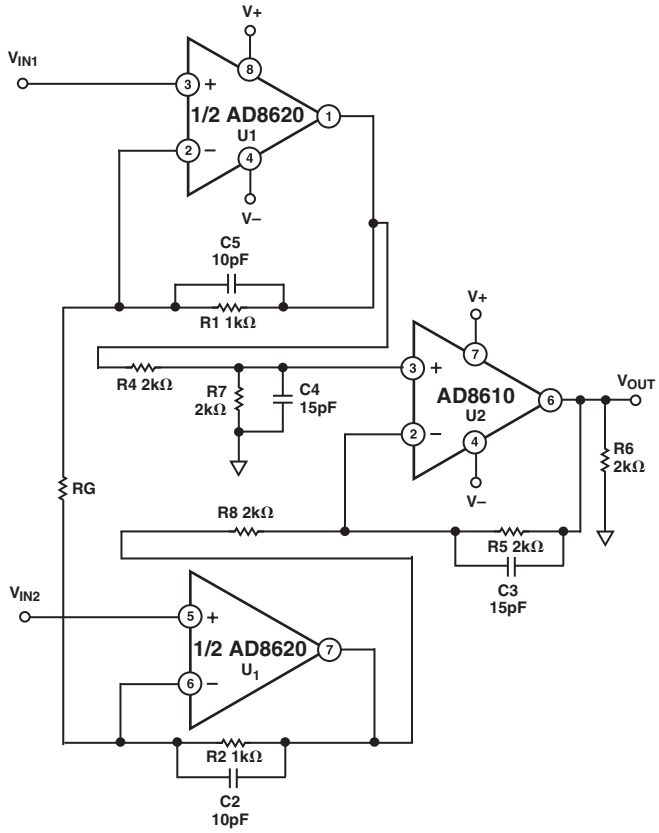


Figure 28. High Speed Instrumentation Amplifier

High Speed Filters

The four most popular configurations are Butterworth, Elliptical, Bessel, and Chebyshev. Each type has a response that is optimized for a given characteristic as shown in Table II.

In active filter applications using operational amplifiers, the dc accuracy of the amplifier is critical to optimal filter performance. The amplifier's offset voltage and bias current contribute to output error. Input offset voltage is passed by the filter, and may be amplified to produce excessive output offset. For low frequency applications requiring large value input resistors, bias and offset currents flowing through these resistors will also generate an offset voltage.

At higher frequencies, an amplifier's dynamic response must be carefully considered. In this case, slew rate, bandwidth, and open-loop gain play a major role in amplifier selection. The slew rate must be both fast and symmetrical to minimize distortion. The amplifier's bandwidth, in conjunction with the filter's gain, will dictate the frequency response of the filter. The use of a high performance amplifier such as the AD8610/AD8620 will minimize both dc and ac errors in all active filter applications.

Second-Order Low-Pass Filter

Figure 29 shows the AD8610 configured as a second-order Butterworth low-pass filter. With the values as shown, the corner frequency of the filter will be 1 MHz. The wide bandwidth of the AD8610/AD8620 allows a corner frequency up to tens of megaHertz. The following equations can be used for component selection:

$$R1 = R2 = User\ Selected\left(Typical\ Values: 10\,k\Omega - 100\,k\Omega\right)$$

$$C1 = \frac{1.414}{(2\pi)(f_{CUTOFF})(R1)}$$

$$C2 = \frac{0.707}{(2\pi)(f_{CUTOFF})(R1)}$$

where *C1* and *C2* are in farads.

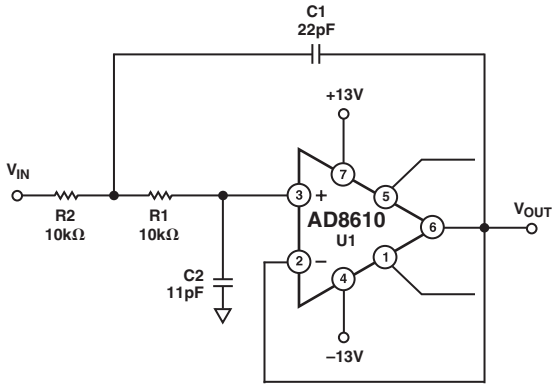


Figure 29. Second-Order Low-Pass Filter

Table II. Filter Types

Type	Sensitivity	Overshoot	Phase	Amplitude (Pass Band)
Butterworth	Moderate	Good		Max Flat
Chebyshev	Good	Moderate	Nonlinear	Equal Ripple
Elliptical	Best	Poor		Equal Ripple
Bessel (Thompson)	Poor	Best	Linear	

High Speed, Low Noise Differential Driver

The AD8620 is a perfect candidate as a low noise differential driver for many popular ADCs. There are also other applications, such as balanced lines, that require differential drivers. The circuit of Figure 30 is a unique line driver widely used in industrial applications. With ±13 V supplies, the line driver can deliver a differential signal of 23 V p-p into a 1 kΩ load. The high slew rate and wide bandwidth of the AD8620 combine to yield a full power bandwidth of 145 kHz while the low noise front end produces a referred-to-input noise voltage spectral density of 6 nV/$\sqrt{\text{Hz}}$. The design is a transformerless, balanced transmission system where output common-mode rejection of noise is of paramount importance. Like the transformer-based design, either output can be shorted to ground for unbalanced line driver applications without changing the circuit gain of 1. This allows the design to be easily set to noninverting, inverting, or differential operation.

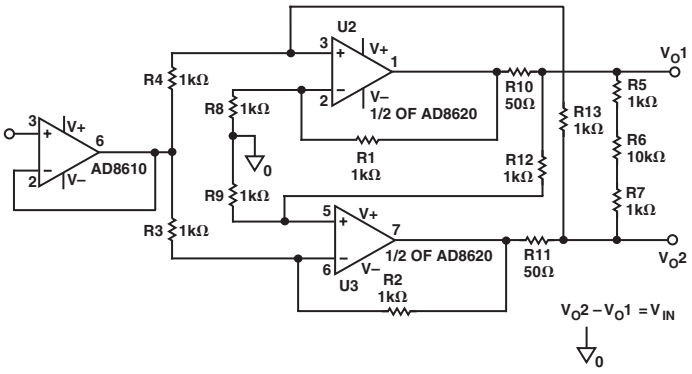
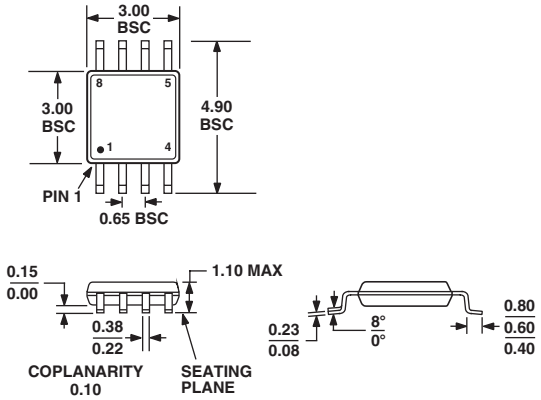


Figure 30. Differential Driver

OUTLINE DIMENSIONS

8-Lead Mini Small Outline Package [MSOP]
(RM-8)

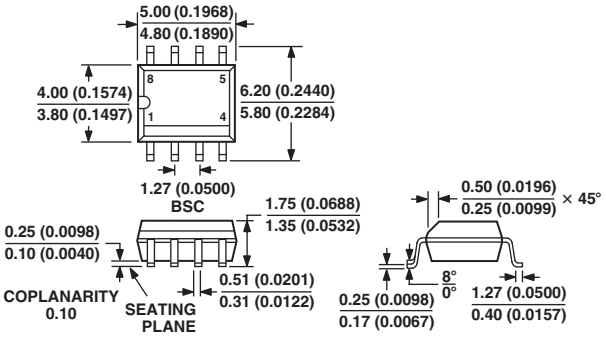
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187AA

8-Lead Standard Small Outline Package [SOIC]
Narrow Body
(R-8)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Revision History

Location	Page
2/04—Data Sheet changed from REV. C to REV. D.	
Changes to SPECIFICATIONS	2
Changes to ORDERING GUIDE	4
Updated OUTLINE DIMENSIONS	17
10/02—Data Sheet changed from REV. B to REV. C.	
Updated ORDERING GUIDE	4
Edits to Figure 15	12
Updated OUTLINE DIMENSIONS	16
5/02—Data Sheet changed from REV. A to REV. B.	
Addition of part number AD8620	Universal
Addition of 8-Lead SOIC (R-8 Suffix) Drawing	1
Changes to GENERAL DESCRIPTION	1
Additions to SPECIFICATIONS	2
Change to ELECTRICAL SPECIFICATIONS	3
Additions to ORDERING GUIDE	4
Replace TPC 29	8
Add Channel Separation Test Circuit Figure	9
Add Channel Separation Graph	9
Changes to Figure 26	15
Addition of High-Speed, Low Noise Differential Driver section	16
Addition of Figure 30	16