1 PRODUCT OVERVIEW

SAM88 RC PRODUCT FAMILY

Samsung's new SAM88RC family of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes. Timer/counters with selectable operating modes are included to support real-time operations. Many SAM88RC microcontrollers have an external interface that provides access to external memory and other peripheral devices. The sophisticated interrupt structure recognizes up to eight interrupt levels. Each level can have one or more interrupt sources and vectors. Fast interrupt processing (within a minimum six CPU clocks) can be assigned to specific interrupt levels.

S3C84A4X MICROCONTROLLER

The S3C84A4 single-chip microcontroller is fabricated using a highly advanced CMOS process. Its design is based on the powerful SAM88RC CPU core. Stop and Idle power-down modes were implemented to reduce power consumption. The size of the internal register file is logically expanded, increasing the addressable on-chip register space to 784 bytes. A flexible yet sophisticated external interface is used to access up to 64-Kbytes of program and data memory. The S3C84A4 is a versatile microcontroller that is ideal for use in a wide range of general-purpose applications such as CD-ROM/DVD-ROM drives.

Using the SAM88RC modular design approach, the following peripherals were integrated with the SAM88RC CPU core:

— Three configurable 8-bit general I/O ports
— One 5-bit general I/O ports
— Two 8-bit timers with interval timer
— Two 16-bit timers/counters with PWM operating modes 8-bit or capture modes
— Voltage level detector circuit embedded.
— Two embedded chip selection pins (CS0–CS1) or normal I/O ports
— Two programmable 8-bit PWM modules with corresponding output pins
— A/D converter with 4 selectable input pins

OTP

The S3C84A4 microcontroller is also avaiable in OTP(One Time Programmable) version, S3P84A4.
The S3P84A4 microcontroller has an on-chip 4K-byte one-time-programmable EPROM instead of masked ROM.
The S3P84A4 is comparable to S3C84A4, both in function and in pin configuration.

FEATURES

CPU

- SAM88RC CPU core

Memory

- 784-byte internal register file
- 4-Kbyte internal program memory

External Interface

- 64K-byte external data memory
- 64K-byte external program memory area (ROMless)
- 60K-byte external program memory and 4K-byte internal program memory
- Automatic wait control function by software.

ADC

- Can be used as a general input/output port
- 8-bit resolution four channels

8-bit Timers

- Two 8-bit timers with interval timer mode (Timer A and B)

16-bit Timer/Counters

- Two programmable 16-bit timer/counters
- Interval, or event counter mode operation
- 16-bit capture and 8-bit PWM mode
- Internal or external clock source

Basic Timer (Watchdog Timer)

- Overflow signal makes a system reset
- 8-bit timer with interval timer mode

General I/O Ports

- Three 8-bit general I/O ports (port 0, 1, 2)
- One 5-bit general I/O port (port 3)
- Port 2 can drive LED directly

Interrupts

- Two edge-driven external interrupts
- Two level-driven external interrupts
- Fast interrupt mode processing

PWM

- Four output channels (PWM0, PWM1, TCPWM, TDPWM)
- 8-bit resolution with a 4-bit prescaler (PWM0, PWM1)
- From 8-bit counter (Timer C/D) (TCPWM, TDPWM)

Embedded chip selection

- To reduce interface glue logic, chip selection logic is embedded (256 byte address unit)

Voltage level detector

- To prevent MCU from malfunctioning in an unstable power level, a voltage level detector circuit is inserted

Operating Voltage Range

- 4.5 V to 5.5 volts (@ 30 MHz)

Operating Temperature Range

- – 40 °C to + 85 °C

Package Types

- 64-pin QFP

Operating frequency

- 30 MHz (4.5 V to 5.5 V)

BLOCK DIAGRAM

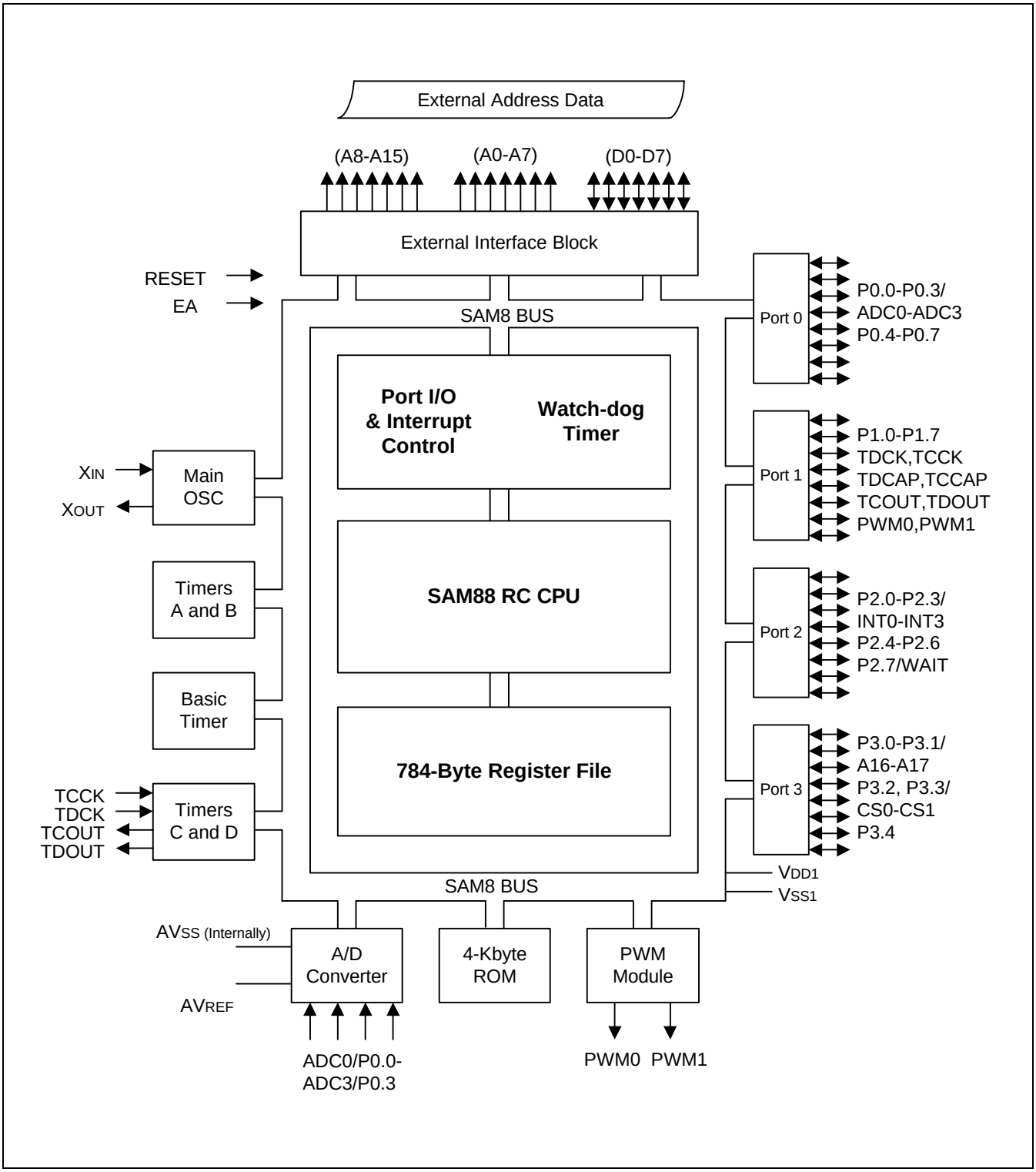


Figure 1-1. S3C84A4 Block Diagram

PIN ASSIGNMENT

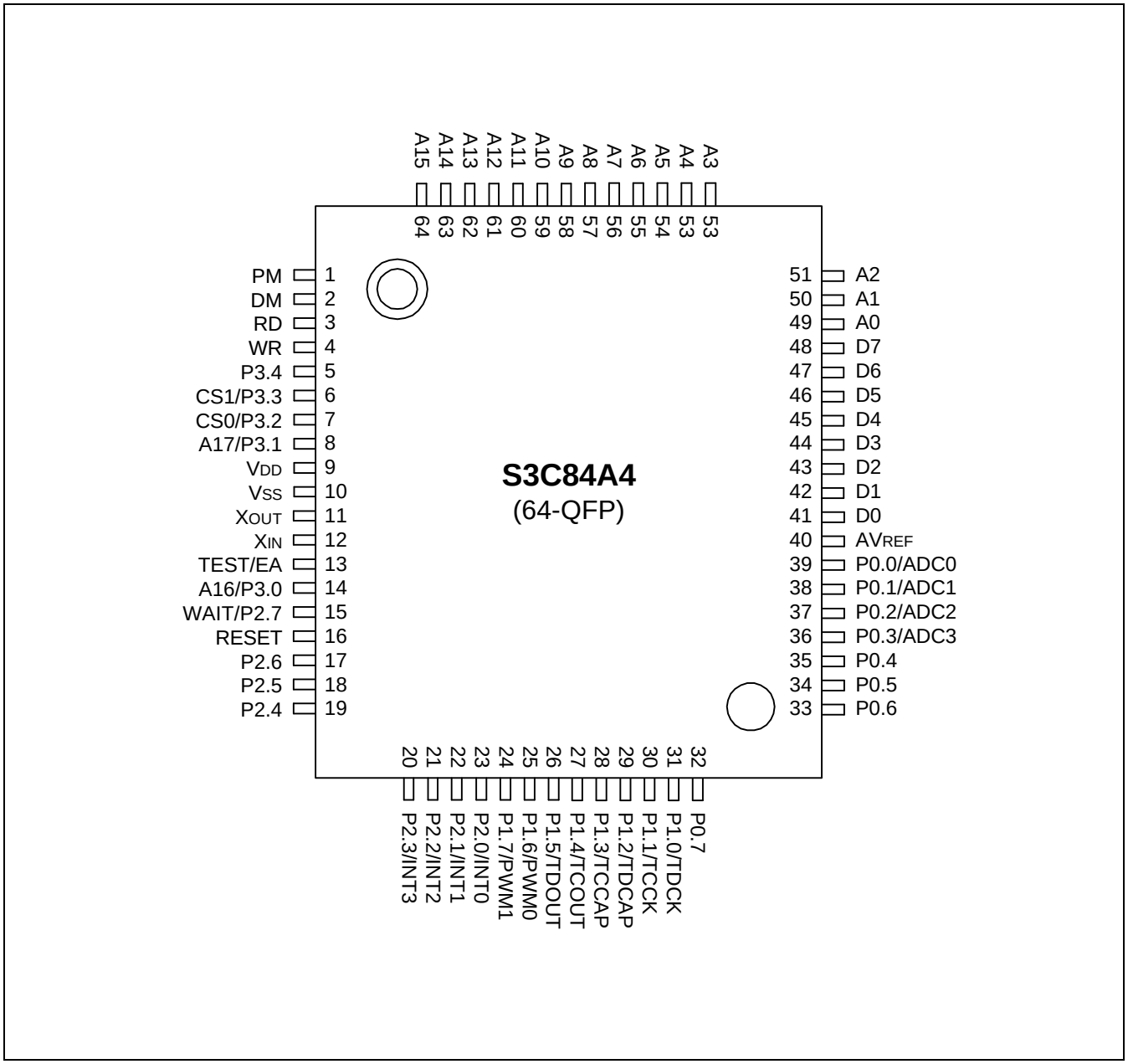


Figure 1-2. S3C84A4 Pin Assignments

PIN DESCRIPTIONS

Table 1-1. S3C84A4/P84A4 Pin Descriptions

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Number	Share Pins
P0.0–P0.7	I/O	Bit programmable port; input or output mode selected by software; normal input or push-pull Software assignable pull-up. Alternately, P0.0–P0.3 can be use as a ADC input port with 8-bit resolution.	2,3	39–32	ADC0–ADC3
P1.0–P1.7	I/O	Bit programmable port; input or output mode selected by software ; normal input or push-pull. Software assignable pull-up. Respectively, each pin can serve as: P1.0 / timer D clock input (TDCK) P1.1 / timer C clock input (TCCK) P1.2 / timer D capture input (TDCAP) P1.3 / timer C capture input (TCCAP) P1.4 / timer C out (TCOUT) / PWM out (TCPWM) P1.5 / timer D out (TDOUT) / PWM out (TDPWM) P1.6 / PWM0 output port P1.7 / PWM1 output port	3,5	31–24	TDCK TCCK TDCAP TCCAP TCOUT/ TCPWM TDOUT/ TDPWM PWM0 PWM1
P2.0–P2.7	I/O	General I/O port with normal input or push-pull output. Software assignable pull-up. Bit programmable; Alternately, P2.0– P2.3 can be used as inputs for external interrupts,INT0– INT3(with noise filter and interrupt control). INT0/INT1 are level interrupts	3,4,5	23–17 15	INT0–INT3
P3.0–P3.4	I/O	General I/O port with bit programmable pins. Normal input or push-pull output with software assignable pull-up. Input or output mode is selectable by software. P3.0-P3.1 can alternately be used as outputs of high address (A16,A17). P3.2–P3.3 can alternately be used as outputs for embedded chip selection output. P3.0 / A16 P3.1 / A17 P3.2 / CS0 P3.3 / CS1	3,5	14, 8–5	A16, A17 CS0,CS1

Table 1-1. S3C84A4/P84A4 Pin Descriptions (Continued)

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Number	Share Pins
ADC0-ADC3	I	Analog input pins for A/D converter module. Alternatively, used as general-purpose I/O	2	39–36	P0.0-P0.3
AV_{REF}	–	A/D converter reference voltage AV_{SS} is connected to ground internally	–	40	–
PWM0, PWM1	O	Pulse width modulation output pins	5	25,24	P1.6, P1.7
INT0-INT3	I	External interrupt input pins	4	23-20	P2.0–P2.3
TCCK, TDCK	I	External clock input for timer C and timer D	3	30,31	P1.1/P1.0
TCCAP, TDCAP	I	Timer C/ Timer D capture input	3	28,29	P1.3/P1.2
TCOUT, TDOUT	O	Timer C/D 8-bit PWM mode output or counter match toggle output	5	27,26	P1.4, P1.5
WAIT	I	Input pin for the slow memory timing signal from the external interface	5	15	P2.7
RESET	I	System reset pin (pull-up resistor: 50 kΩ)	1	16	–
EA	I	5V: ROMless operating 0V: internal 4K and external 60K addressing mode	–	13	–
V_{DD}, V_{SS}	–	Power input pins	–	9,10	–
X_{IN}, X_{OUT}	–	Main oscillator pins	–	12,11	–
A0–A15	O	Address output for external device	6	49–64	–
D0–D7	I/O	Data I/O for external device	7	41–48	–
PM, DM	O	External memory selection output	–	1,2	–
RD,WR	O	External memory read/write output	–	3, 4	–
A16, A17	O	Extended memory high address output	5	14, 8	P3.0, P3.1
CS0–CS1	O	Embedded chip selection output	5	7, 6	P3.2, P3.3

PIN CIRCUITS

Table 1-2. Pin Circuit Assignments for the S3C84A4/P84A4

Circuit Number	Circuit Type	S3C8414X Assignments
1	Input	RESET pin
2	I/O	A/D converter input pins, ADC0–ADC3, P0.0–P0.3
3	I/O	Port 0, 2, and 3
4	I/O	P2 (INT0–INT3)
5	I/O	P1 (TDCK, TCCK, TDCAP, TCCAP, TCOUT, TDOUT, TCPWM, TDPWM, PWM0, PWM1)
6	Output	A0–A15, PM, DM, RD, WR
7	I/O	D0–D7

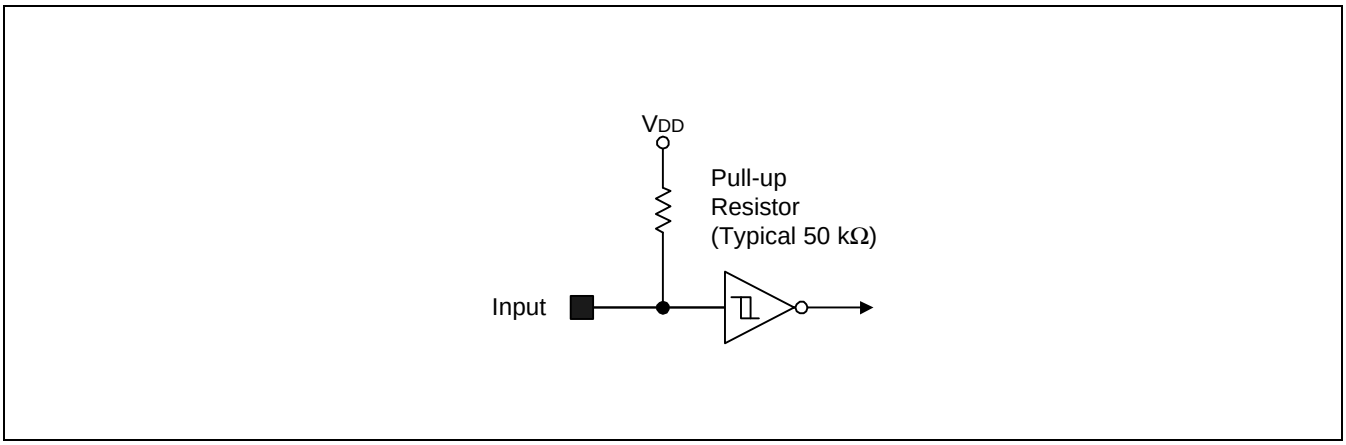


Figure 1-4. Pin Circuit Type 1 (RESET)

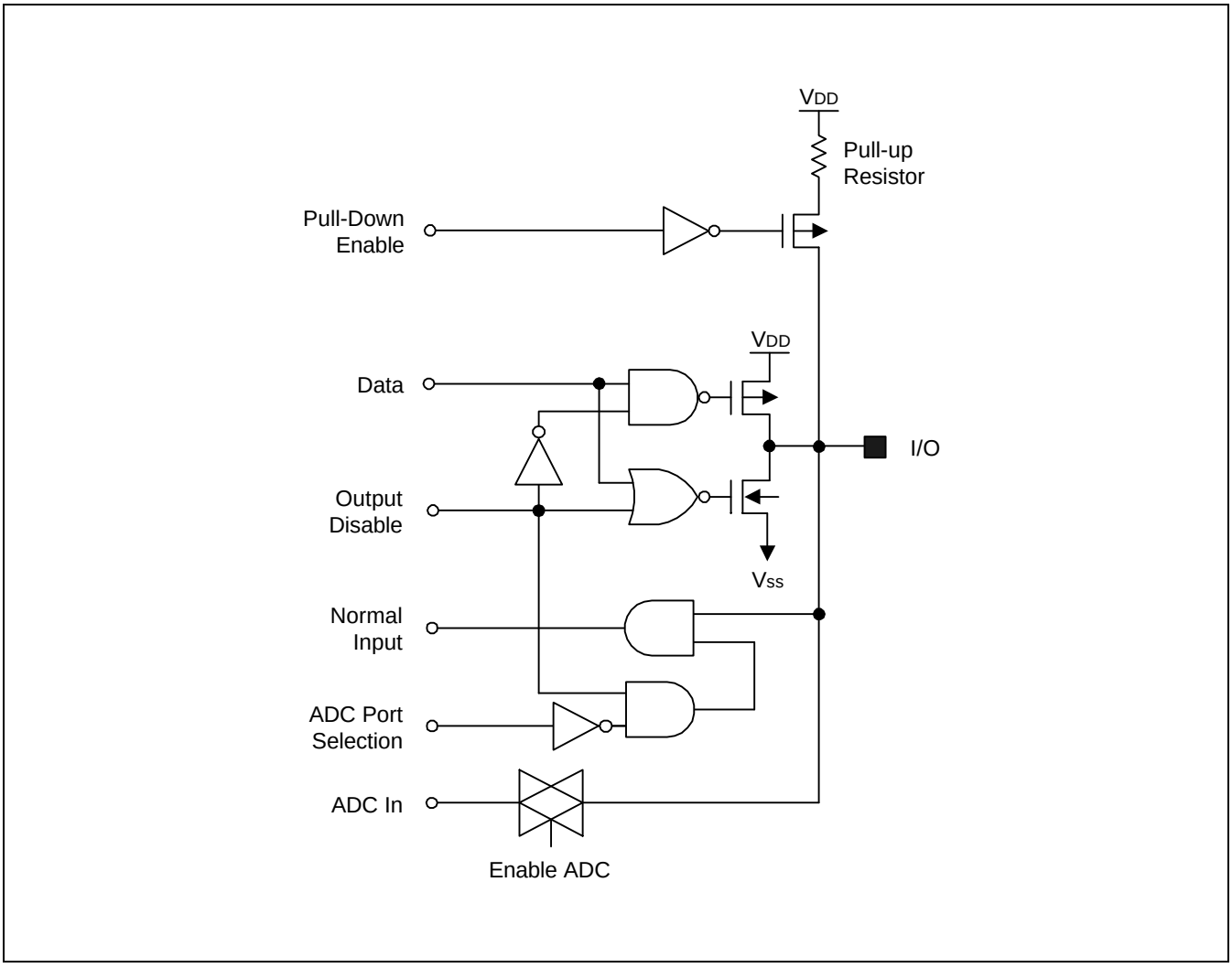


Figure 1-5. Pin Circuit Type 2 (ADC0–ADC3)

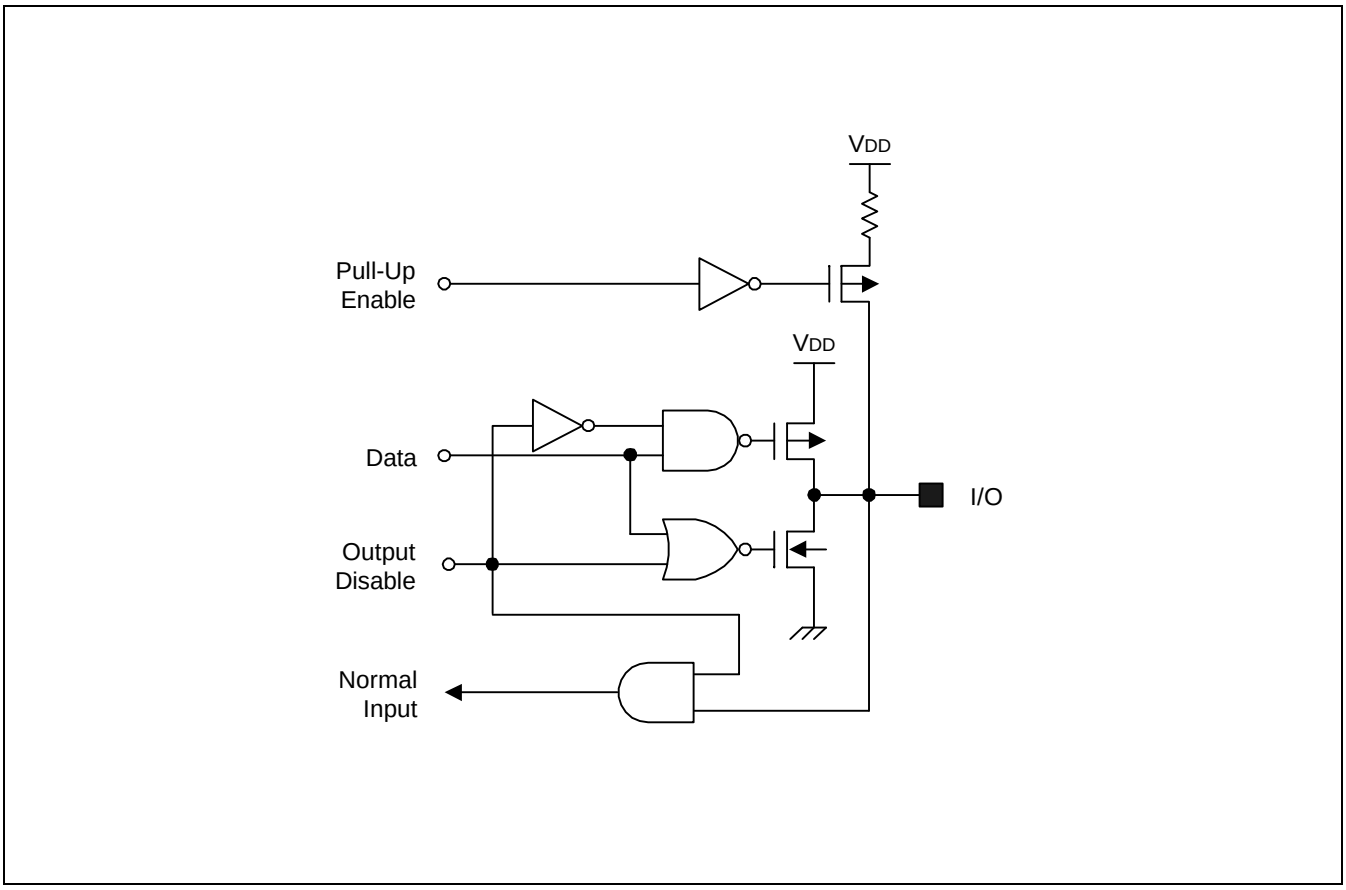


Figure 1-6. Pin Circuit Type 3

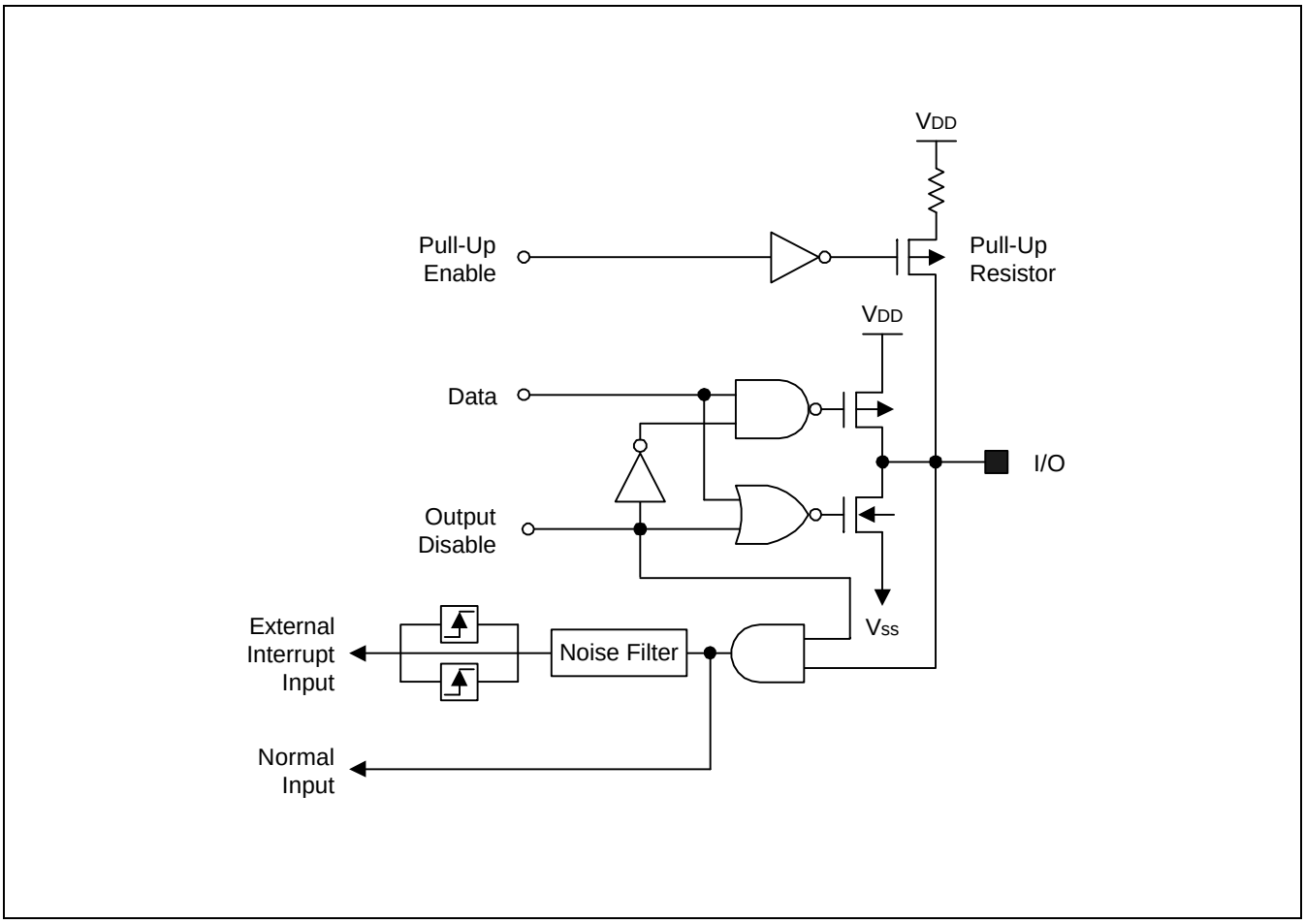


Figure 1-7. Pin Circuit Type 4

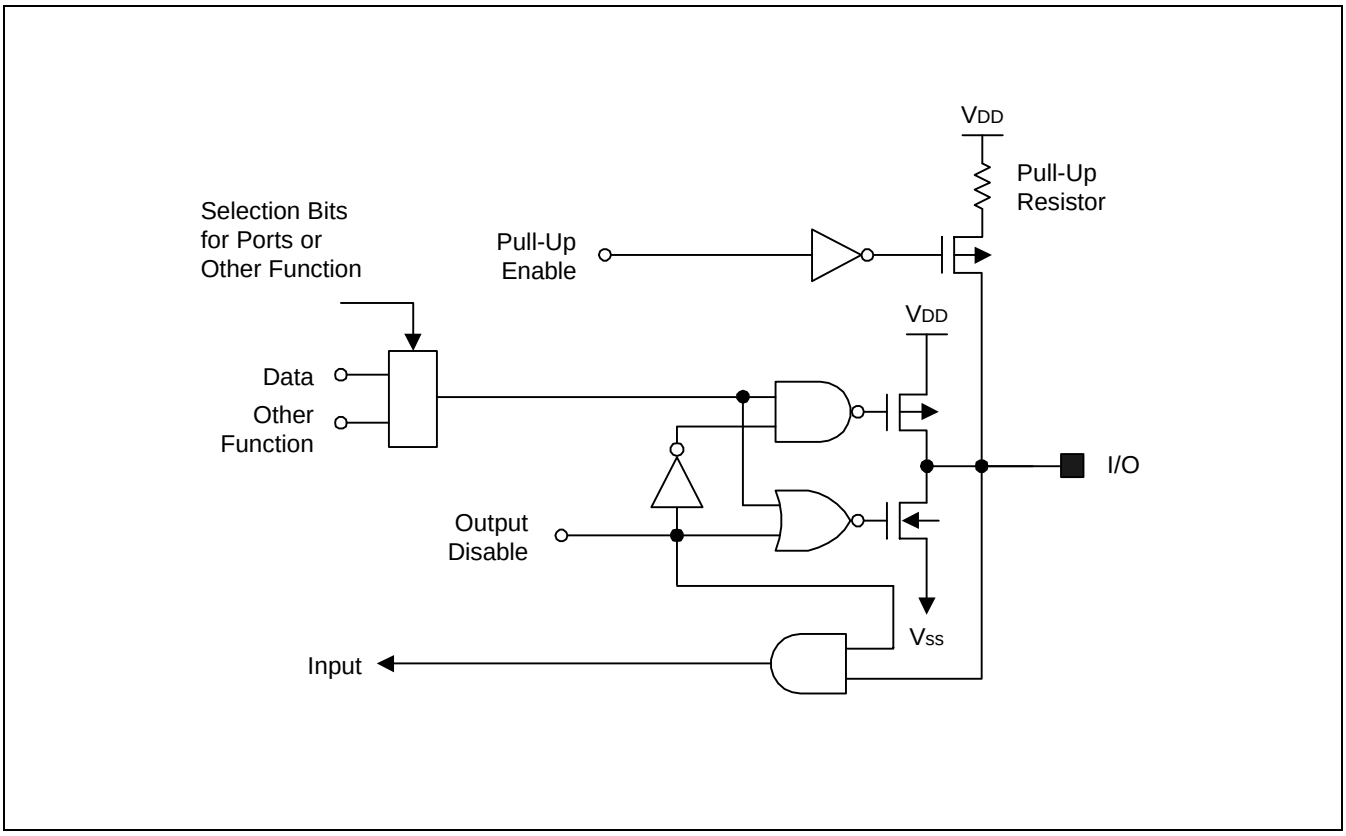


Figure 1-8. Pin Circuit Type 5

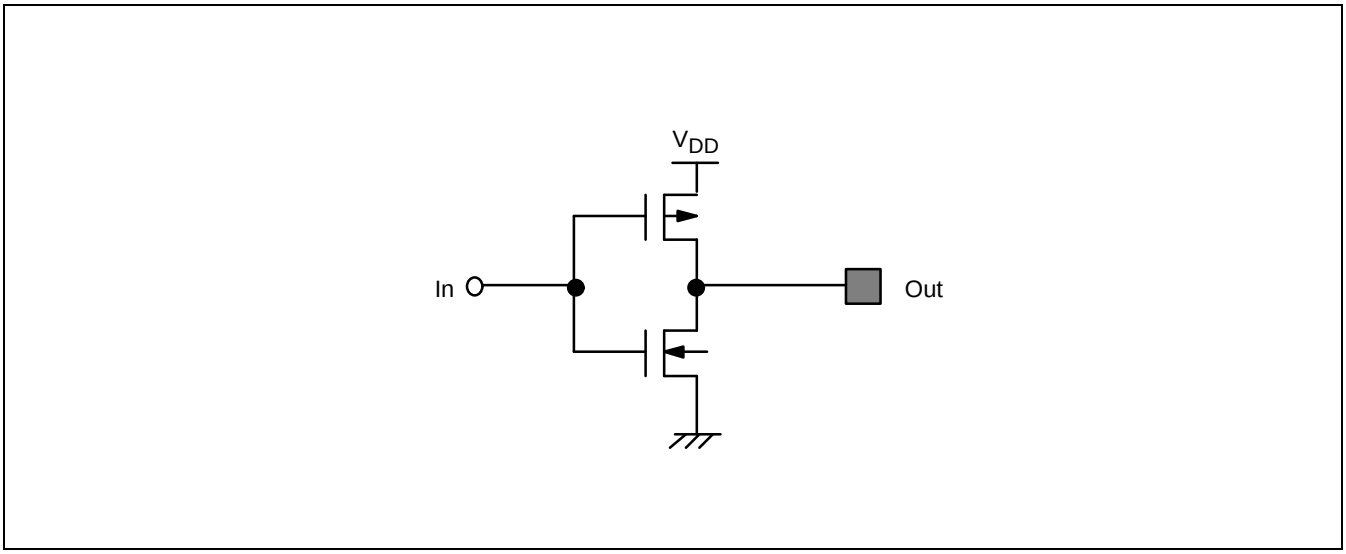


Figure 1-9. Pin Circuit Type 6

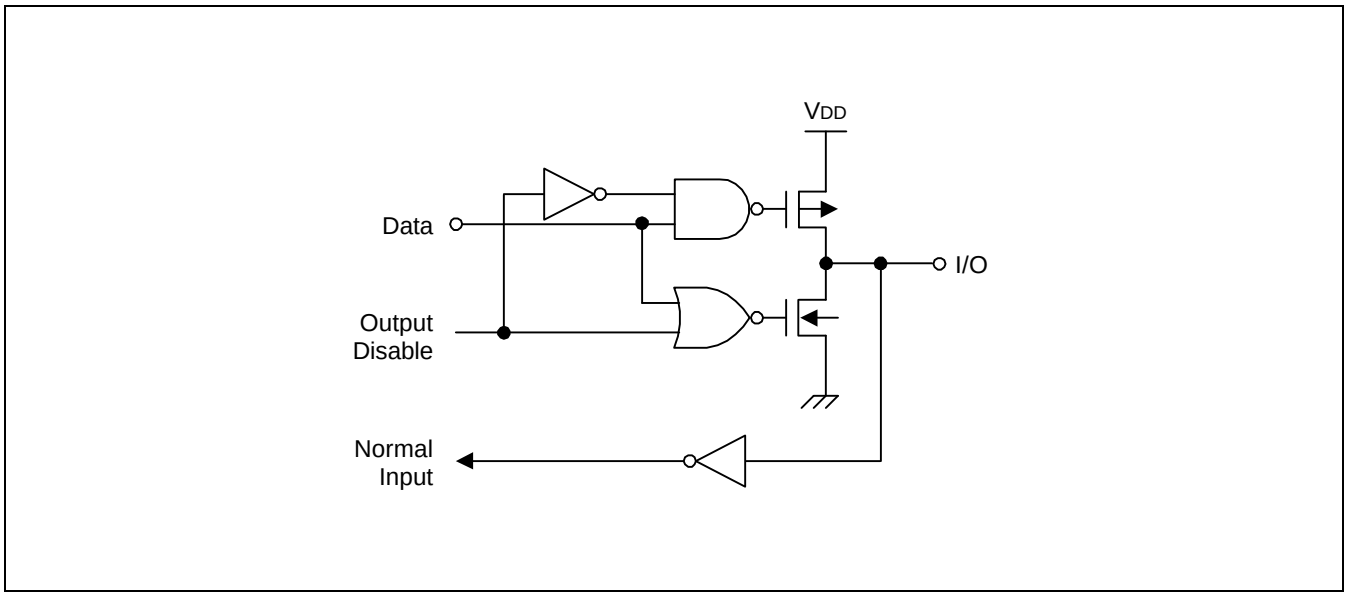


Figure 1-10. Pin Circuit Type 7

17 ELECTRICAL DATA

OVERVIEW

In this section, S3C84A4 electrical characteristics are presented in tables and graphs. The information is arranged in the following order:

— Absolute maximum ratings
— D.C. electrical characteristics
— A.C. electrical characteristics
— I/O capacitance
— Oscillation characteristics
— Oscillation stabilization time

Table 17-1. Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}		– 0.3 to + 6.5	V
Input voltage	V_I		– 0.3 to V_{DD} + 0.3	
Output voltage	V_O		– 0.3 to V_{DD} + 0.3	V
Output current high	I_{OH}	One I/O pin active	– 18	mA
		All I/O pins active	– 60	
Output current low	I_{OL}	One I/O pin active	+ 30	mA
		Total pin current for port	+ 100	
Operating temperature	T_A		– 40 to + 85	°C
Storage temperature	T_{STG}		– 65 to + 150	°C

Table 17-2. D.C. Electrical Characteristics

(T_A = – 40°C to + 85°C, V_{DD} = 2.7 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating voltage	V_{DD}	F_{OSC} = 30 MHz (instruction clock = 7.5 MHz)	4.5	–	5.5	V
Input high voltage	V_{IH1}	All input pins except V_{IH2}, V_{IH3}	0.51 V_{DD}	–	V_{DD}	V
	V_{IH2}	RESET	0.8 V_{DD}			
	V_{IH3}	X_{IN}	V_{DD} – 0.5			
Input low voltage	V_{IL1}	All input pins except V_{IL2}	–	–	0.2 V_{DD}	V
	V_{IL2}	X_{IN}			0.4	
Output high voltage	V_{OH}	V_{DD}= 5 V, I_{OH} = – 1 mA	V_{DD} – 1.0	–	–	V
		I_{OH} = – 100 uA	V_{DD} – 0.5	–	–	
Output low voltage	V_{OL1}	V_{DD} = 5 V, I_{OL} = 2 mA All output pins except port 2	–	–	0.4	V
	V_{OL2}	V_{DD} = 5 V I_{OL} = 15 mA, port 2	–	0.5	1.0	
Input high leakage current	I_{LIH1}	V_{IN} = V_{DD} All input pins except X_{IN}	–	–	3	µA
	I_{LIH2}	V_{IN} = V_{DD} X_{IN}			20	
Input low leakage current	I_{LIL1}	V_{IN} = 0 V All input pins except X_{IN}	–	–	– 3	
	I_{LIL2}	V_{IN} = 0 V, X_{IN}			– 20	
Output high leakage current	I_{LOH}	V_{OUT} = V_{DD} All I/O pins and output pins	–	–	5	
Output low leakage current	I_{LOL}	V_{OUT} = 0 V All I/O pins and output pins	–	– 0	– 5	
Pull-up and pull-down resistor	R_{L1}	V_{IN} = 0 V; V_{DD} = 5 V Ports 0–3, T_A = 25 °C	30	46	80	kΩ
	R_{L2}	V_{IN} = 0 V; V_{DD} = 5 V T_A = 25 °C, RESET only	30	50	80	

Table 17-2. D.C. Electrical Characteristics (Continued)

(T_A = – 40°C to + 85°C, V_{DD} = 2.7 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current (note)	I_{DD1}	V_{DD} = 5 V ± 10% 30 MHz oscillation	–	30	60	mA
	I_{DD2}	Idle mode; V_{DD} = 5 V ± 10% 30 MHz oscillation		10	20	
	I_{DD3}	Stop mode; V_{DD} = 5 V ± 10% LVD enable, T_A = 25°C		100	200	µA

NOTE: Supply current does not include current drawn through internal pull-up resistors or external output current loads.

Table 17-3. A.C. Electrical Characteristics

(T_A = -40°C to + 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interrupt input high, low width (P2.0-P2.7)	t_{INTH}, t_{INTL}	V_{DD} = 5V	180	–	–	nS
RESET input low width	t_{RSL}	V_{DD} = 5V	1000	–	–	nS

NOTES:
1. The unit t_{CPU} means one CPU clock period.
2. The oscillator frequency is the same as the CPU clock frequency.

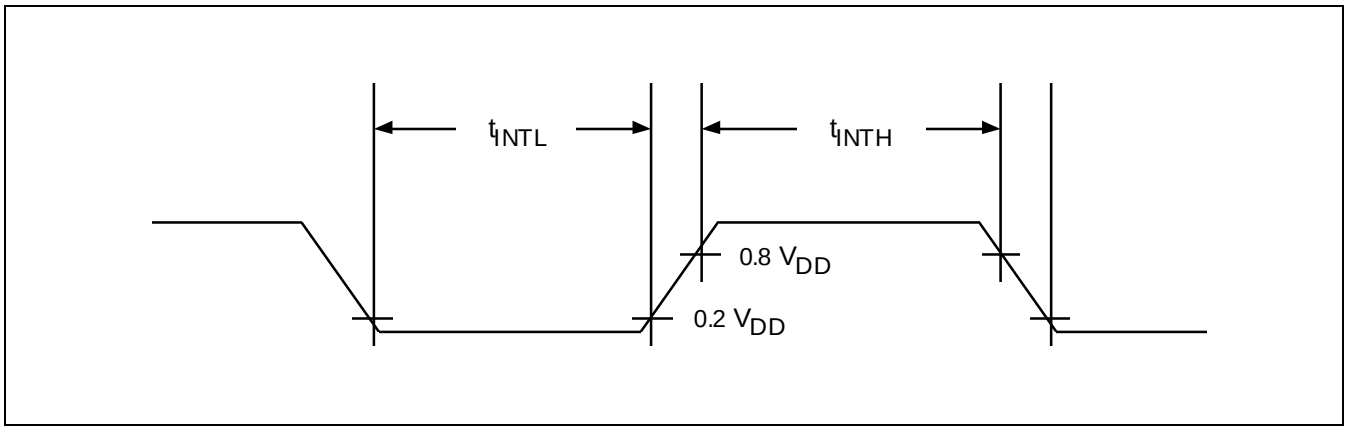


Figure 17-1. Input Timing for External Interrupts (Ports 2)

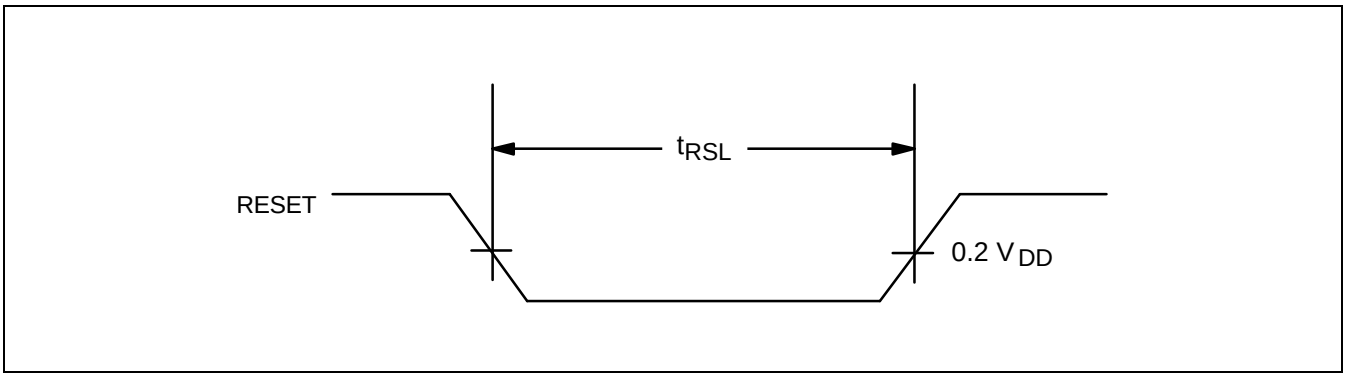


Figure 17-2. Input Timing for RESET

Table 17-4. Input/Output Capacitance

(T_A = – 40°C to + 85°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_{IN}	f = 1 MHz; unmeasured pins are connected to V_{SS}	–	–	10	pF
Output capacitance	C_{OUT}					
I/O capacitance	C_{IO}					

Table 17-5. Data Retention Supply Voltage in Stop Mode

(T_A = – 40°C to + 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}		2	–	5.5	V
Data retention supply current	I_{DDDR}	Stop mode, V_{DDDR} = 2.0 V	–	–	50	µA

NOTES:
1. During the oscillator stabilization wait time (t_{WAIT}), all CPU operations must be stopped.
2. Supply current does not include drawn through internal pull-up resistors and external output current loads.

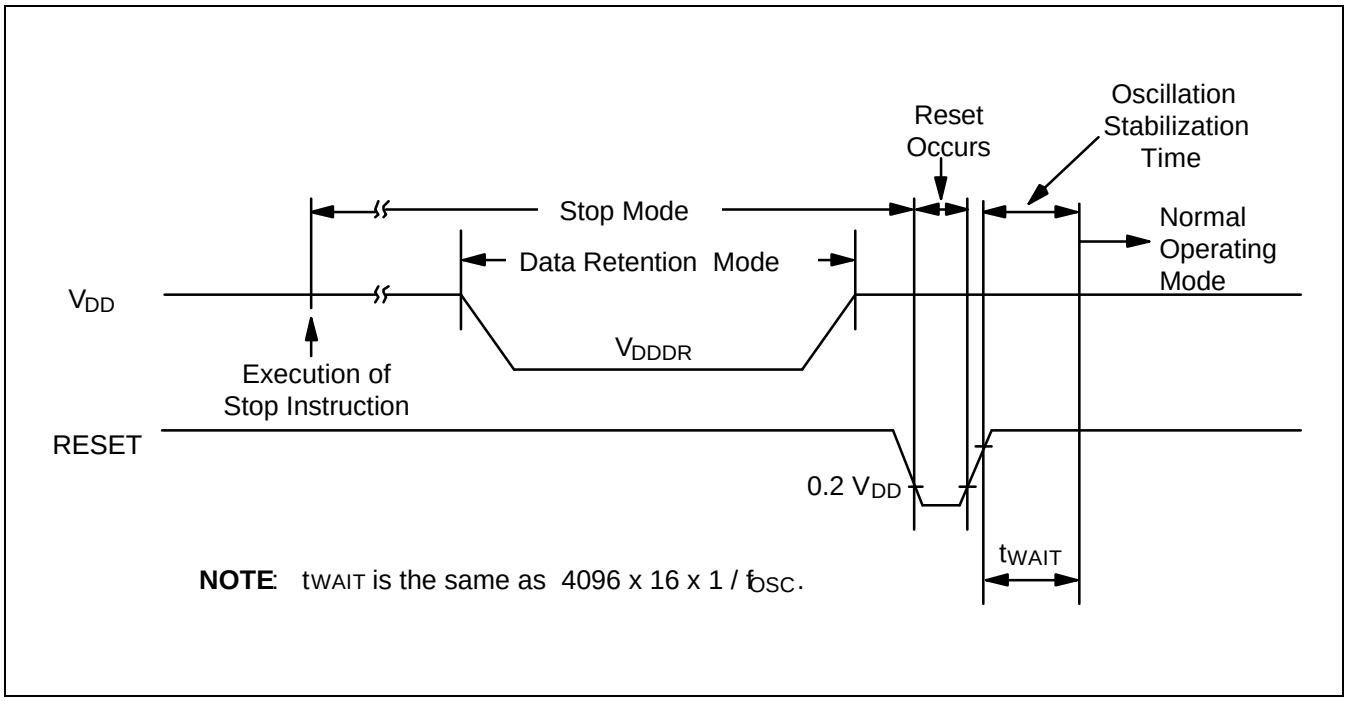


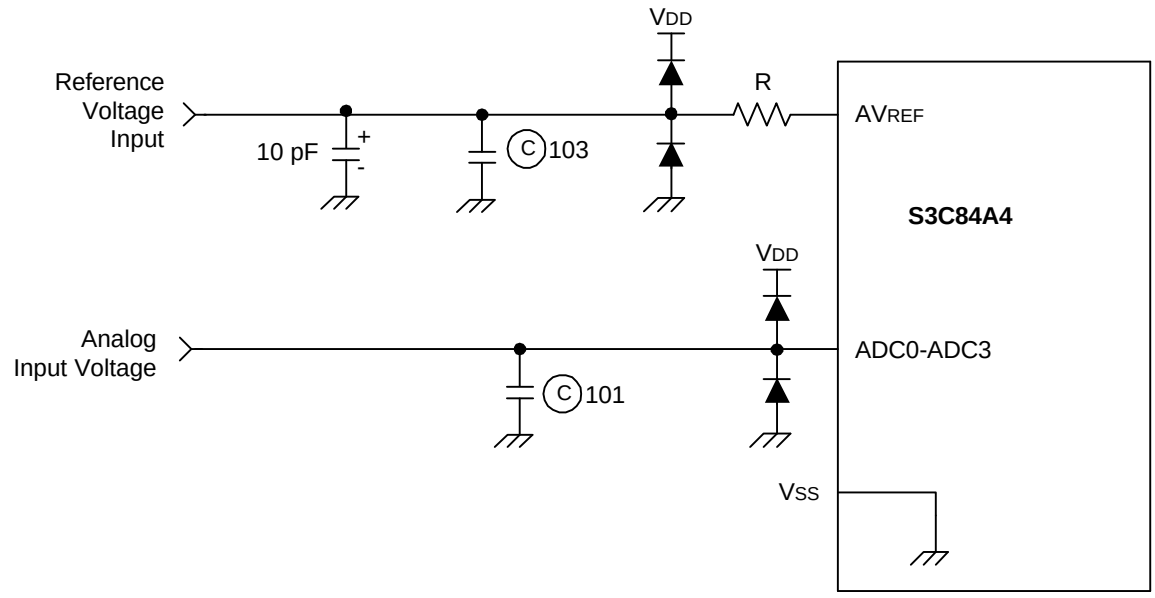
Figure 17-3. Stop Mode Release Timing Initiated by RESET

Table 17-6. A/D Converter Electrical Characteristics

(T_A = – 40°C to + 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Resolution			–	8	–	bit
Total accuracy		V_{DD} = 5 V	–	–	± 3	LSB
Integral linearity error	ILE	Conversion time = 5 us		–	± 2	
Integral linearity error	DLE	AV_{REF} = 5 V		–	± 1	
Offset error of top	EOT	AV_{SS} = 0 V		± 1	± 3	
Offset error of bottom	EOB			± 0.5	± 2	
Conversion time (1)	t_{CON}		17	30	250	µs
Analog input voltage	V_{IAN}		AVss	–	AVref	V
Analog input impedance	R_{AN}	–	2	1000	–	MΩ
Analog reference voltage	AV_{REF}	–	3.0	–	V_{DD}	V
Analog input current	I_{ADIN}	AV_{REF} = V_{DD} = 5V	–	–	10	uA
Analog block current(2)	I_{ADC}	AV_{REF} = V_{DD} = 5V		1	3	mA
		AV_{REF} = V_{DD} = 3V		0.5	1.5	mA
		AV_{REF} = V_{DD} = 5V When Power Down mode		100	500	nA

NOTES:
1. 'Conversion time' is the time required from the moment a conversion operation starts until it ends.
2. I_{ADC} is an operating current during A/D conversion.



NOTE: The symbol "R" signifies an offset resistor with a value of from 50 to 100. If this resistor is omitted, the absolute accuracy will be maximum of 3 LSBs.

Figure 17-4. Recommended A/D Converter Circuit for Highest Absolute Accuracy

Table 17-7. Main Oscillator Frequency (f_{OSC1})

(T_A = – 40°C + 85°C, V_{DD} = 4.5 V to 5.5 V)

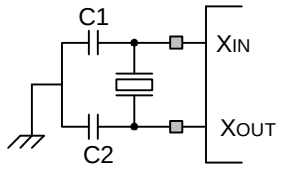
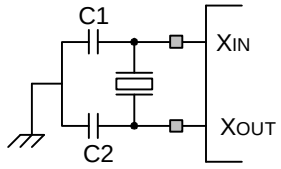
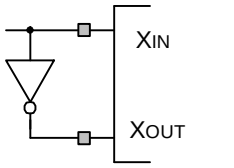
Oscillator	Clock Circuit	Test Condition	Min	Typ	Max	Unit
Crystal		CPU clock oscillation frequency	4	–	25	MHz
Ceramic		CPU clock oscillation frequency	4	–	30	MHz
External clock		X_{IN} input frequency	4	–	30	MHz

Table 17-8. Main Oscillator Clock Stabilization Time (t_{ST1})

(T_A = -40°C + 85°C, V_{DD} = 4.5 V to 5.5 V)

Oscillator	Test Condition	Min	Typ	Max	Unit
Crystal	V_{DD} = 4.5 V to 5.5 V	–	–	10	ms
Ceramic	Stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	–	–	4	ms
External clock	X_{IN} input high and low level width (t_{XH}, t_{XL})	50	–	–	ns

NOTE: Oscillation stabilization time (t_{ST1}) is the time required for the CPU clock to return to its normal oscillation frequency after a power-on occurs, or when Stop mode is ended by a RESET signal. The RESET should therefore be held at low level until the t_{ST1} time has elapsed.

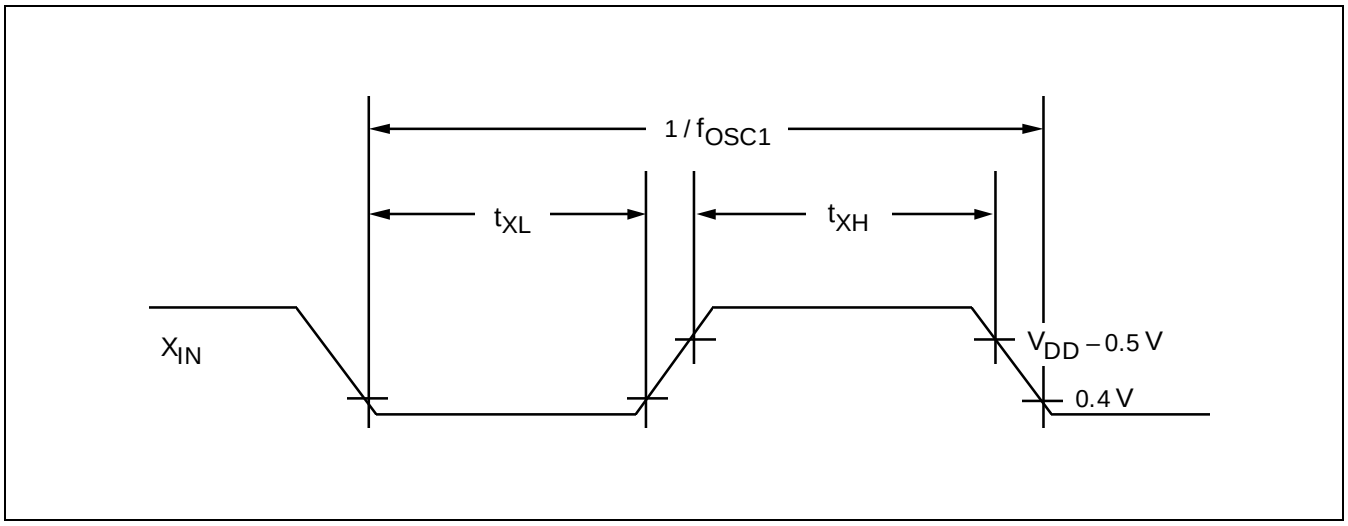


Figure 17-6. Clock Timing Measurement at X_{IN}

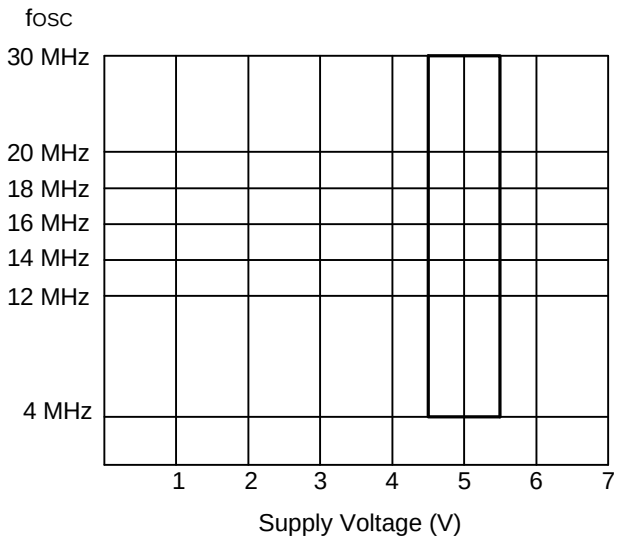
Table 17-9. Characteristics of Voltage Level Detect circuit

(T_A = – 40°C + 85°C) When Power off

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage of VLD	V_{DD}	–	4.5	–	5.5	V
Detect Voltage	V_{DET}	–	3.1	3.7	4.1	V
Current consumption	I_{VLD}	V_{DD} = 5.5 V	–	100	200	uA

(T_A = – 40°C + 85°C) When Power on

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage of VLD	V_{DD}	–	4.5	–	5.5	V
Detect Voltage	V_{DET}	–	3.4	4.0	4.4	V
Current consumption	I_{VLD}	V_{DD} = 5.5 V	–	100	200	uA



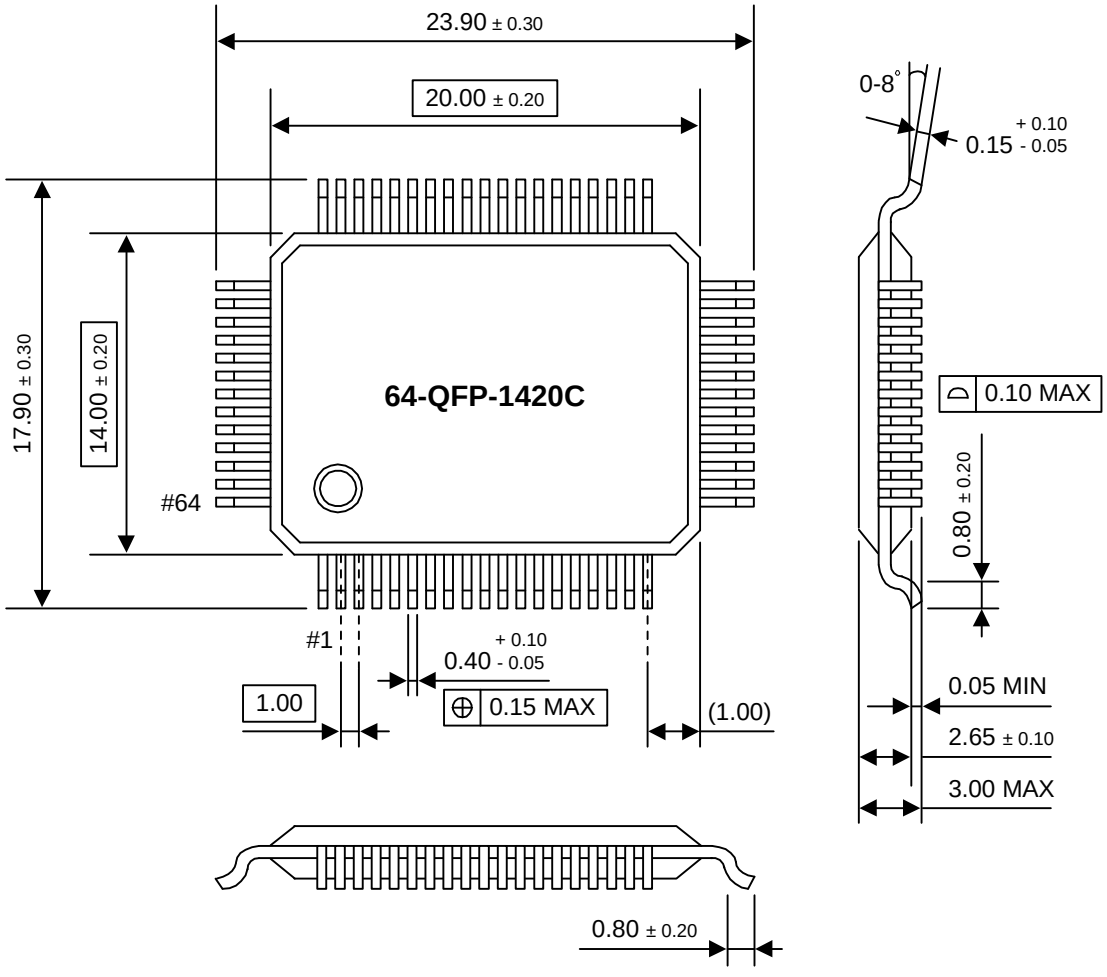
Minimum Instruction Clock = 1/4 x oscillator frequency

Figure 17-7. Operating Voltage Range (LVD Enable)

18 MECHANICAL DATA

OVERVIEW

The S3C84A4 microcontroller is available in a 64-pin QFP package (64-QFP-1420C) .



NOTE: Dimensions are in millimeters.

Figure 18-1. 64-QFP-1420C Package Dimensions

19 S3P84A4 OTP

OVERVIEW

The S3P84A4 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C84A4 microcontrollers. It has an on-chip EPROM instead of masked ROM. The EPROM is accessed by serial data format.

S3C84A4 is fully compatible with S3C84A4, both in function and in pin configuration. As it has simple programming requirements, S3P84A4 is ideal for use as an evaluation chip for the S3C84A4.

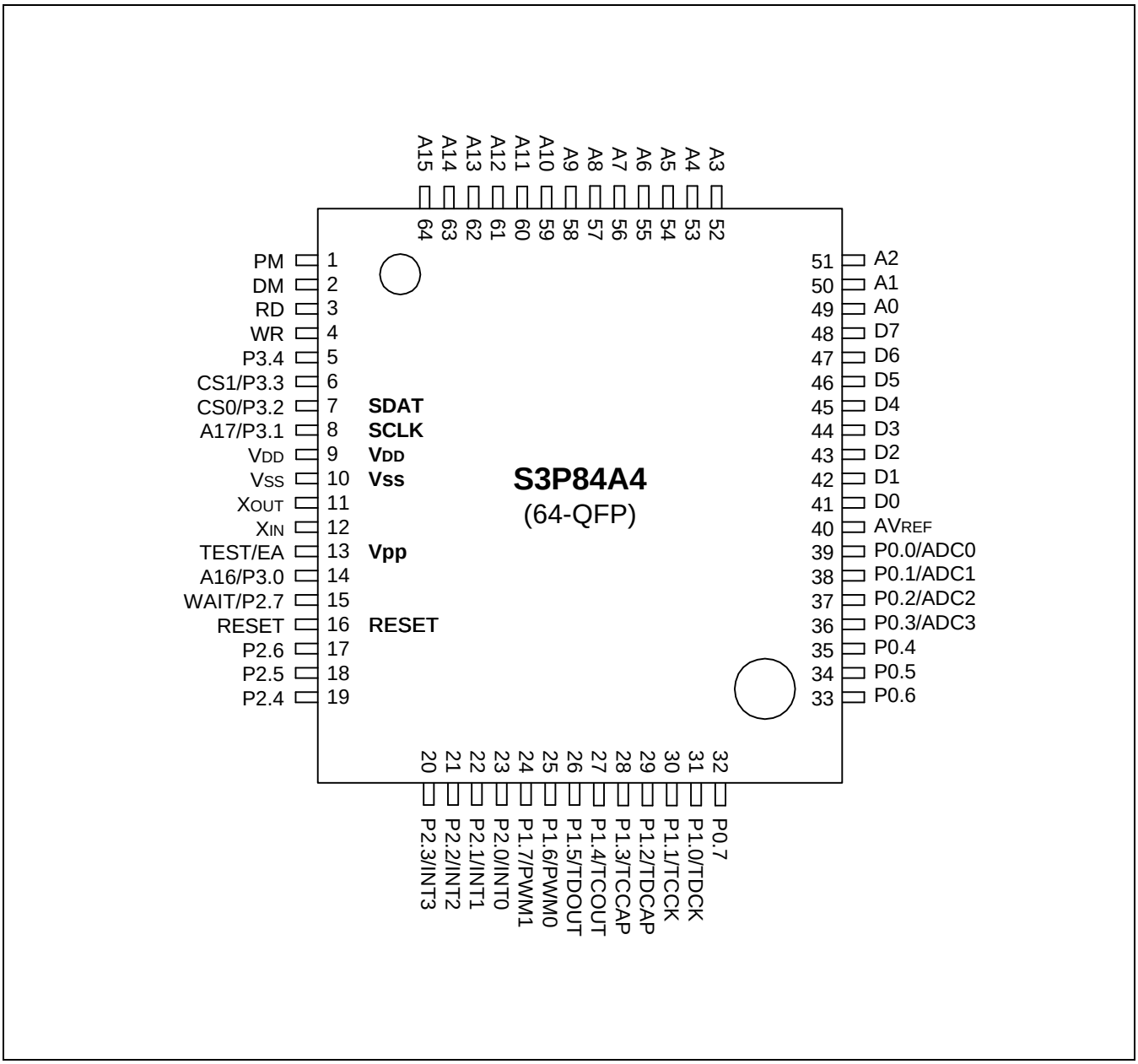


Figure 19-1. S3P84A4 Pin Assignments (64-QFP Package)

Table 19-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip Pin Name	During Programming			
	Pin Name	Pin No.	I/O	Function
P3.2	SDAT	7	I/O	Serial Data Pin (Output when reading, Input when writing) Input and Push-pull Output Port can be assigned.
P3.1	SCLK	8	I	Serial Clock Pin (Input Only Pin)
EA	V_{PP}	13	I	EPROM Cell Writing Power Supply Pin (Indicates OTP Mode Entering) When writing 12.5V is applied and when reading 5 V is applied (Option).
RESET	RESET	16	I	Chip Initialization
V_{DD1}/V_{SS1}	V_{DD}/V_{SS}	9/10	I	Logic Power Supply Pin. V_{DD} should be tied to 5V during programming.

Table 19-2. Comparison of S3P84A4 and S3C84A4 Features

Characteristic	S3P84A4	S3C84A4
Program Memory	4 K byte EPROM	4 K bytes mask ROM
Operating Voltage (V_{DD})	2.7 V to 5.5 V	2.7 V to 5.5V
OTP Programming Mode	V_{DD} = 5 V, V_{PP} (TEST) = 12.5V	
Pin Configuration	64 QFP	64 QFP
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP} (TEST) pin of S3P84A4, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 19-3 below.

Table 19-3. Operating Mode Selection Criteria

V_{DD}	Vpp (TEST)	REG/ MEM	Address (A15-A0)	R/W	Mode
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.

D.C. ELECTRICAL CHARACTERISTICS

Table 19-4. D/C Electrical Characteristics

(T_A = – 40°C to + 85°C, V_{DD} = 2.7 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating voltage	V_{DD}	F_{OSC} = 30 MHz (instruction clock = 7.5 MHz)	4.5	–	5.5	V
Input high voltage	V_{IH1}	All input pins except V_{IH2}, V_{IH3}	0.51 V_{DD}	–	V_{DD}	V
	V_{IH2}	RESET	0.8 V_{DD}			
	V_{IH3}	X_{IN}	V_{DD} – 0.5			
Input low voltage	V_{IL1}	All input pins except V_{IL2}	–	–	0.2 V_{DD}	V
	V_{IL2}	X_{IN}			0.4	
Output high voltage	V_{OH}	V_{DD}= 5 V, I_{OH} = – 1 mA	V_{DD} – 1.0	–	–	V
		I_{OH} = – 100 uA	V_{DD} – 0.5	–	–	
Output low voltage	V_{OL1}	V_{DD} = 5 V, I_{OL} = 2 mA All output pins except port 2	–	–	0.4	V
	V_{OL2}	V_{DD} = 5 V I_{OL} = 15 mA, port 2	–	0.5	1.0	
Input high leakage current	I_{LIH1}	V_{IN} = V_{DD} All input pins except X_{IN}	–	–	3	µA
	I_{LIH2}	V_{IN} = V_{DD} X_{IN}			20	
Input low leakage current	I_{LIL1}	V_{IN} = 0 V All input pins except X_{IN}	–	–	– 3	
	I_{LIL2}	V_{IN} = 0 V, X_{IN}			– 20	
Output high leakage current	I_{LOH}	V_{OUT} = V_{DD} All I/O pins and output pins	–	–	5	
Output low leakage current	I_{LOL}	V_{OUT} = 0 V All I/O pins and output pins	–	– 0	– 5	
Pull-up and pull-down resistor	R_{L1}	V_{IN} = 0 V; V_{DD} = 5 V Ports 0–3, T_A = 25 °C	30	46	80	kΩ
	R_{L2}	V_{IN} = 0 V; V_{DD} = 5 V T_A = 25 °C, RESET only	30	50	80	

Table 19-4. D/C Electrical Characteristics (Continued)

(T_A = – 40°C to + 85°C, V_{DD} = 2.7 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current (note)	I_{DD1}	V_{DD} = 5 V ± 10% 30 MHz oscillation	–	30	60	mA
	I_{DD2}	Idle mode; V_{DD} = 5 V ± 10% 30 MHz oscillation		10	20	
	I_{DD3}	Stop mode; V_{DD} = 5 V ± 10% LVD enable, T_A = 25°C		100	200	µA

NOTE: Supply current does not include current drawn through internal pull-up resistors or external output current loads.