Lattice™ Semiconductor Corporation

Specifications *ispLSI and pLSI 3192*
ispLSI® and pLSI® 3192

High Density Programmable Logic

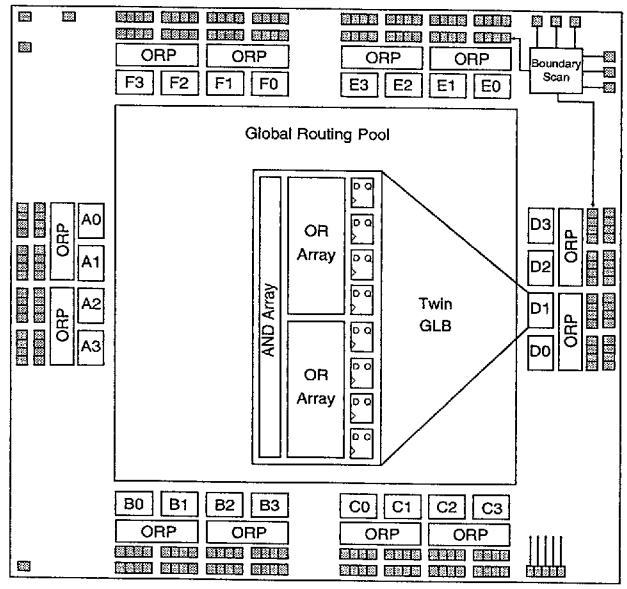
Features

- **HIGH-DENSITY PROGRAMMABLE LOGIC**
  - — 192 I/O Pins
  - — 9000 PLD Gates
  - — 384 Registers
  - — High Speed Global Interconnect
  - — Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  - — Small Logic Block Size for Random Logic
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - — f_{max} = 100 MHz Maximum Operating Frequency
  - — t_{pd} = 10 ns Propagation Delay
  - — TTL Compatible Inputs and Outputs
  - — Electrically Erasable and Reprogrammable
  - — Non-Volatile
  - — 100% Tested at Time of Manufacture
  - — Unused Product Term Shutdown Saves Power
- **ispLSI OFFERS THE FOLLOWING ADDED FEATURES**
  - — In-System Programmable™ (ISP™) 5-Volt Only
  - — Increased Manufacturing Yields, Reduced Time-to-Market, and Improved Product Quality
  - — Reprogram Soldered Devices for Faster Debugging
- **100% IEEE 1149.1 BOUNDARY SCAN COMPATIBLE**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - — Complete Programmable Device Can Combine Glue Logic and Structured Designs
  - — Five Dedicated Clock Input Pins
  - — Synchronous and Asynchronous Clocks
  - — Programmable Output Slew Rate Control to Minimize Switching Noise
  - — Flexible Pin Placement
  - — Optimized Global Routing Pool Provides Global Interconnectivity
- **ispLSI AND pLSI DEVELOPMENT TOOLS**

  pDS® Software
  - — Easy to Use PC Windows™ Interface
  - — Boolean Logic Compiler
  - — Manual Partitioning
  - — Automatic Place and Route
  - — Static Timing Table

  ispDS+™ Software
  - — Industry Standard, Third Party Design Environments
  - — Schematic Capture, State Machine, HDL
  - — Automatic Partitioning and Place and Route
  - — Comprehensive Logic and Timing Simulation
  - — PC and Workstation Platforms

Functional Block Diagram



0139/3192

Description

The ispLSI and pLSI 3192 are High Density Programmable Logic Devices which contain 384 Registers, 192 Universal I/O pins, five Dedicated Clock Input Pins, twelve Output Routing Pools (ORP), and a Global Routing Pool (GRP) which allows complete inter-connectivity between all of these elements. The ispLSI 3192 features 5-Volt in-system programmability and in-system diagnostic capabilities. The ispLSI 3192 offers non-volatile "on-the-fly" reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems. It is architecturally and parametrically compatible to the pLSI 3192 devices.

The basic unit of logic on the ispLSI and pLSI 3192 devices is the Twin Generic Logic Block (Twin GLB) labelled A0, A1...F3. There are a total of 24 of these Twin GLBs in the ispLSI and pLSI 3192 devices. Each Twin GLB has 24 inputs, a programmable AND array and two OR/Exclusive-OR Arrays, and eight outputs which can be configured to be either combinatorial or registered. All Twin GLB inputs come from the GRP.

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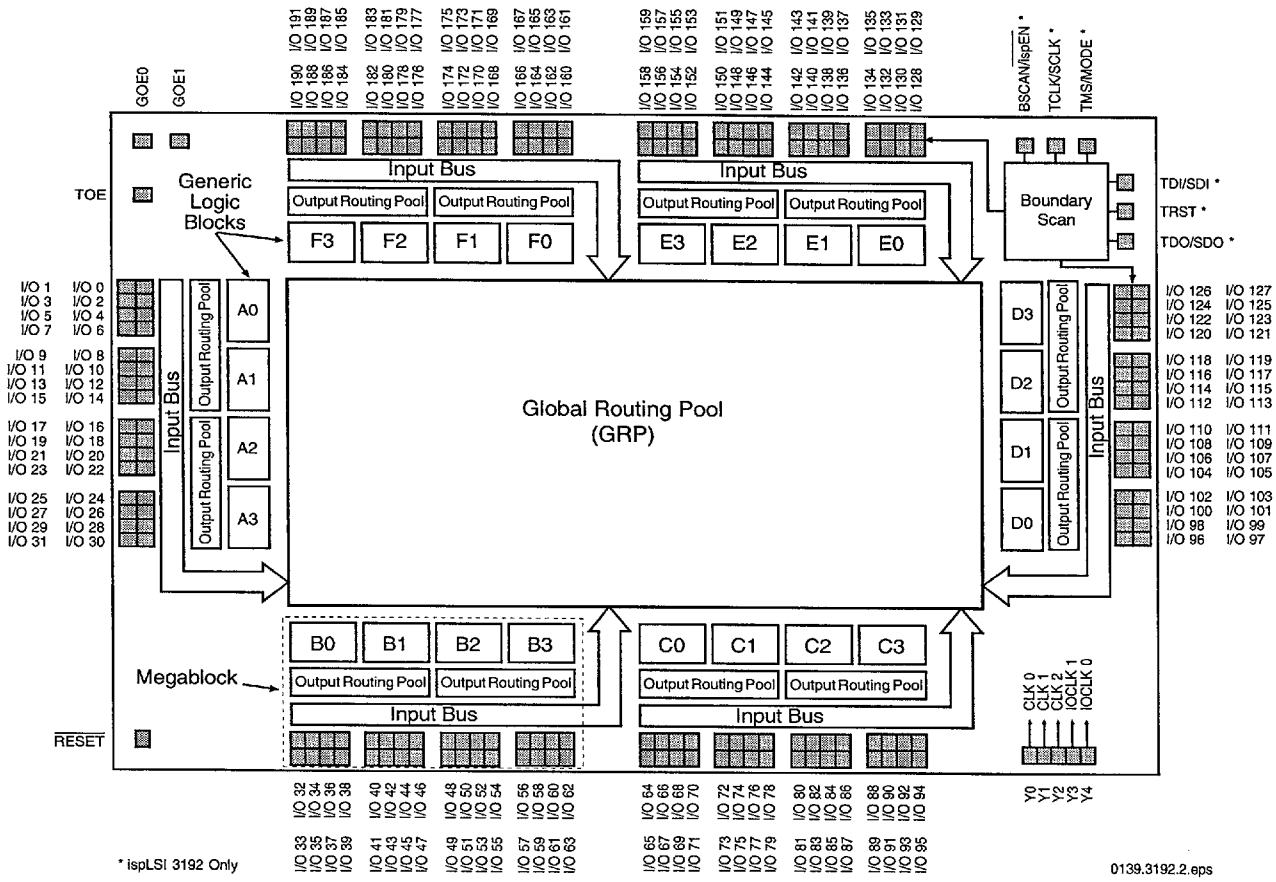
ISP Encyclopedia

Functional Block Diagram

Figure 1. ispLSI and pLSI 3192 Functional Block Diagram



Description (continued)

All local logic block outputs are brought back into the GRP so they can be connected to the inputs of any other logic block on the device. The device also has 192 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, a registered input, a latched input, an output or a bidirectional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

The 192 I/O Cells are grouped into six sets of 32 bits. Each of these I/O groups is associated with a logic Megablock through the use of the ORP. Each Megablock is able to provide one Product Term Output Enable (PTOE) signal which is globally distributed to all I/O cells. That PTOE signal can be generated within any GLB in the Megablock. Each I/O cell can select either a Global OE or a PTOE.

Four Twin GLBs, 32 I/O Cells and two ORPs are connected together to make a logic Megablock. The Megablock is defined by the resources that it shares. The outputs of the four Twin GLBs are connected to a set of 32 I/O cells by the two ORPs. The ispLSI and pLSI 3192 device contains six of these Megablocks.

The GRP has as its inputs the outputs from all of the Twin GLBs and all of the inputs from the bidirectional I/O cells. All of these signals are made available to the inputs of the Twin GLBs. Delays through the GRP have been equalized to minimize timing skew and logic glitching.

Clocks in the ispLSI and pLSI 3192 devices are provided through five dedicated clock pins. The five pins provide three clocks to the Twin GLBs and two clocks to the I/O cells.

The table below lists key attributes of the device along with the number of resources available.

An additional feature of the ispLSI and pLSI 3192 is the Boundary Scan capability, which is composed of cells connected between the on-chip system logic and the device's input and output pins. All I/O pins have associated boundary scan registers, with 3-state I/O using three boundary scan registers and inputs using one.

The ispLSI and pLSI 3192 supports all IEEE 1149.1 mandatory instructions, which include BYPASS, EXTEST and SAMPLE.

Key Attributes of the ispLSI and pLSI 3192

Attribute	Quantity
Twin GLBs	24
Registers	384
I/O Pins	192
Global Clocks	5
Global OE	2
Test OE	1

e - 003/3192

Absolute Maximum Ratings [1]

Supply Voltage V_{cc} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specific tion is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to +70°C	4.75	5.25	V
		Industrial	T_A = -40°C to +85°C	4.5	5.5	V
V_{IL}	Input Low Voltage			0	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+1	V

Table 2 - 0005/3192

Capacitance (T_A=25°C,f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	I/O Capacitance	10	pf	V_{CC}= 5.0V, $V_{I/O}$ = 2.0V
C_2	Clock Capacitance	15	pf	V_{CC}= 5.0V, V_Y = 2.0V

Table 2 - 0006/3192

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles
pLSI Erase/Reprogram Cycles	100	–	Cycles

Table 2- 0008B

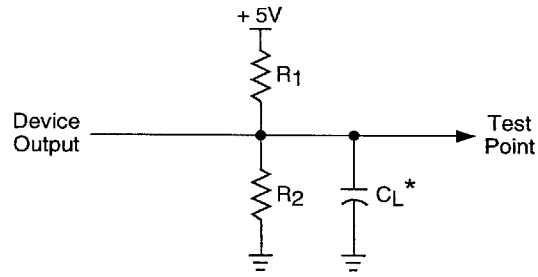
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Ouput Timing Reference Levels	1.5V
Output Load	See figure 2

Table 2 - 0003

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213A

Output Load conditions (See figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH}-0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL}+0.5V	470Ω	390Ω	5pF

Table 2 - 0004A

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL}= 8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH}= -4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}		–	–	10	µA
I_{IL-isp}	Bscan/$\overline{ispEN}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC}= 5V, V_{OUT} = 0.5V		–	–	-200	mA
I_{CC}[2,4]	Operating Power Supply Current	V_{IL}= 0.0V, V_{IH}= 3.0V, f_{TOGGLE} = 1 MHz	Commercial	–	320	–	mA
			Industrial	–	320	–	mA

Table 2 - 0007isp/3192

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2. Measured using twelve 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this datasheet and Thermal Management section of this Data Book to estimate maximum I_{CC}.

External Switching Characteristics[1, 2, 3]

Over Recommended Operating Conditions

PARAMETER	TEST[5] COND.	#[2]	DESCRIPTION[1]	-100		-70		UNITS
				MIN.	MAX.	MIN.	MAX.	
tpd1	A	1	Data Prop. Delay, 4PT Bypass, ORP Bypass	—	10	—	15	ns
tpd2	A	2	Data Propagation Delay	—	13	—	18	ns
fmax	A	3	Clock Frequency with Internal Feedback[3]	100	—	70	—	MHz
fmax (Ext.)	—	4	Clock Freq. with Ext. Feedback,1/(tsu2 + tco1)	80	—	50	—	MHz
fmax (Tog.)	—	5	Clock Frequency, Max Toggle[4]	125	—	83	—	MHz
tsu1	—	6	GLB Reg. Setup Time before Clock, 4PT bypass	5.5	—	9	—	ns
tco1	A	7	GLB Reg. Clock to Output Delay, ORP bypass	—	6	—	9	s
th1	—	8	GLB Reg. Hold Time after Clock, 4PT bypass	0	—	0	—	s
tsu2	—	9	GLB Reg. Setup Time before Clock	6.5	—	11	—	ns
tco2	—	10	GLB Reg. Clock to Output Delay	—	6.5	—	10	ns
th2	—	11	GLB Reg. Hold Time after Clock	0	—	0	—	s
tr1	A	12	Ext. Reset Pin to Output Delay	—	13.5	—	15	ns
trw1	—	13	Ext. Reset Pulse Duration	6.5	—	12	—	ns
tptoeen	B	14	Input to Output Enable	—	15	—	18	ns
tptoedis	C	15	Input to Output Disable	—	15	—	18	ns
tgoeen	B	16	Global OE Output Enable	—	9	—	12	ns
tgoedis	C	17	Global OE Output Disable	—	9	—	12	ns
ttoeen	—	18	Test OE Output Enable	—	12	—	15	ns
ttoedis	—	19	Test OE Output Disable	—	12	—	15	ns
twh	—	20	Ext. Sync. Clock Pulse Duration, High	4	—	6	—	s
twl	—	21	Ext. Sync. Clock Pulse Duration, Low	4	—	6	—	s
tsu3	—	22	I/O Reg. Setup Time before Ext. Sync. Clock (Y3, Y4)	3.5	—	5	—	ns
th3	—	23	I/O Reg. Hold Time after Ext. Sync. Clock (Y3, Y4)	0	—	0	—	s

1. Unless noted otherwise, all parameters use 20 PTXOR path and ORP.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. fmax (Toggle) may be less than 1/(twh + twl). This is to allow for a clock duty cycle
5. Reference Switching Test Conditions section.

Timing Ext.6192.eps

Internal Timing Parameters[1]

Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-100		-70		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
tiobp	24	I/O Register Bypass	—	1.3	—	1.9	ns
tiolat	25	I/O Latch Delay	—	9.2	—	13.2	ns
tiosu	26	I/O Register Setup Time before Clock	6.5	—	9.3	—	ns
tioh	27	I/O Register Hold Time after Clock	-3.0	—	-4.3	—	ns
tioch	28	I/O Register Clock to Out Delay	—	1.5	—	2.3	ns
tior	29	I/O Register Reset to Out Delay	—	3.3	—	3.9	ns
GRP							
tgrp	30	GRP Delay	—	1.4	—	2.1	ns
GLB							
t4ptbp	31	4 Product Term Bypass Path Delay (Comb.)	—	4.3	—	7.8	ns
t4ptbr	32	4 Product Term Bypass Path Delay (Reg.)	—	5.5	—	7.4	ns
t1ptxor	33	1 Product Term/XOR Path Delay	—	6.0	—	8.3	ns
t20ptxor	34	20 Product Term/XOR Path Delay	—	6.5	—	9.4	ns
txoradj	35	XOR Adjacent Path Delay[3]	—	7.1	—	10.3	ns
tgbp	36	GLB Register Bypass Delay	—	0.3	—	0.4	ns
tgsu	37	GLB Register Setup Time before Clock	0.2	—	1.7	—	ns
tgh	38	GLB Register Hold Time after Clock	3.5	—	5.3	—	ns
tgco	39	GLB Register Clock to Output Delay	—	0.1	—	1.7	ns
tgro	40	GLB Register Reset to Output Delay	—	2.4	—	2.8	ns
tptre	41	GLB Product Term Reset to Register Delay	—	5.0	—	7.5	ns
tptoe	42	GLB Product Term Output Enable to I/O Cell Delay	—	7.6	—	9.2	ns
tptck	43	GLB Product Term Clock Delay	4.9	5.9	7.4	8.8	ns
ORP							
torp	44	ORP Delay	—	1.1	—	1.7	ns
torpbp	45	ORP Bypass Delay	—	0.6	—	0.7	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Internal Timing Parameters[1]

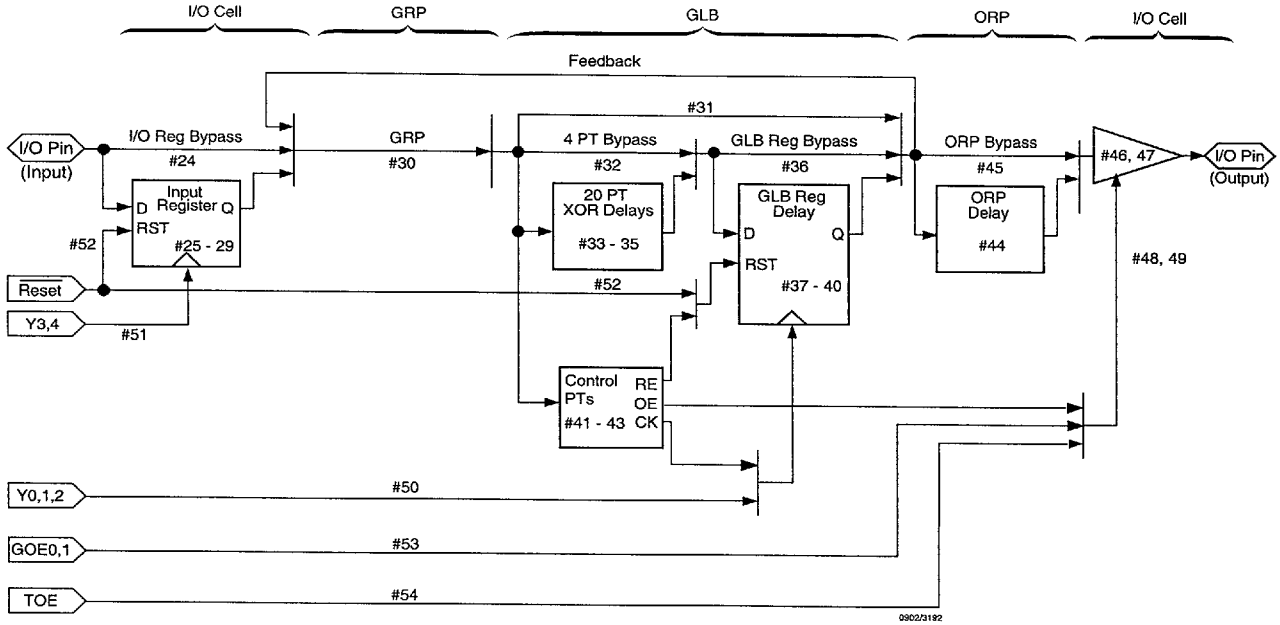
Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-100		-70		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
tob	46	Output Buffer Delay	—	2.4	—	2.5	ns
tobs	47	Output Buffer Delay, Slow Slew	—	22.4	—	27.5	ns
toen	48	I/O Cell OE to Output Enabled	—	4.7	—	4.8	ns
todis	49	I/O Cell OE to Output Disabled	—	4.7	—	4.8	ns
Clocks							
tgy0/1/2	50	Clock Delay, Y0 or Y1 or Y2 to Global GLB Clk Line	2.9	2.9	4.1	4.1	ns
tioy3/4	51	Clock Delay, Y3 or Y4 to I/O Cell Global Clock Line	3.0	3.0	4.3	4.3	ns
Global Reset							
tgr	52	Global Reset to GLB and I/O Registers	—	7.6	—	8.0	ns
tgoe	53	Global OE Pad Buffer	—	4.3	—	7.2	ns
ttoe	54	Test OE Pad Buffer	—	7.3	—	10.2	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

Timing Int.2.3192.eps

ispLSI and pLSI 3192 Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

tsu = Logic + Reg su - Clock (min)
= (**t**iobp + **t**grp + **t**20ptxor) + (**t**gsu) - (**t**iobp + **t**grp + **t**ptck(min))
= (#24+ #30+ #34) + (#37) - (#24+ #30+ #43)
1.8 ns = (1.3 + 1.4 + 6.5) + (0.2) - (1.3 + 1.4 + 4.9)

th = Clock (max) + Reg h - Logic
= (**t**iobp + **t**grp + **t**ptck(max)) + (**t**gh) - (**t**iobp + **t**grp + **t**20ptxor)
= (#24+ #30+ #43) + (#38) - (#24+ #30+ #34)
2.9 ns = (1.3 + 1.4 + 5.9) + (3.5) - (1.3 + 1.4 + 6.5)

tco = Clock (max) + Reg co + Output
= (**t**iobp + **t**grp + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
= (#24 + #30 + #43) + (#39) + (#44 + #46)
12.2 ns = (1.3 + 1.4 + 5.9) + (0.1) + (1.1 + 2.4)

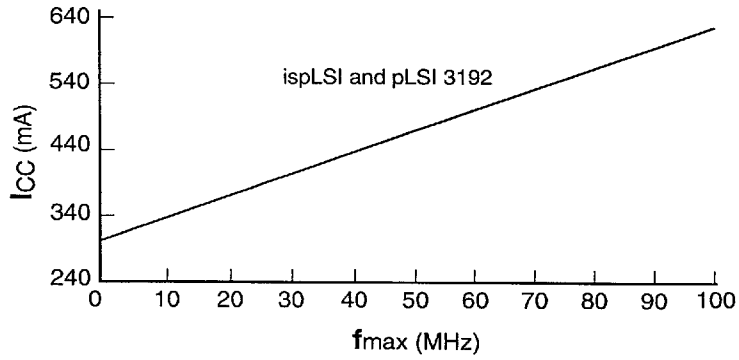
Table 2- 0042-3192

Note: Calculations are based upon timing specifications for the ispLSI and pLSI 3192-100L.

Power Consumption

Power Consumption in the ispLSI and pLSI 3192 device depends on two primary factors: the speed at which the device is operating and the number of product terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of 16 16-bit Counters
Typical Current at 5V, 25° C

I_{CC} can be estimated for the ispLSI and pLSI 3192 using the following equation:

I_{CC} = 50 + (# of PTs * 0.65) + (# of nets * Max. freq * 0.015) where:
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max. freq = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

0127/3192

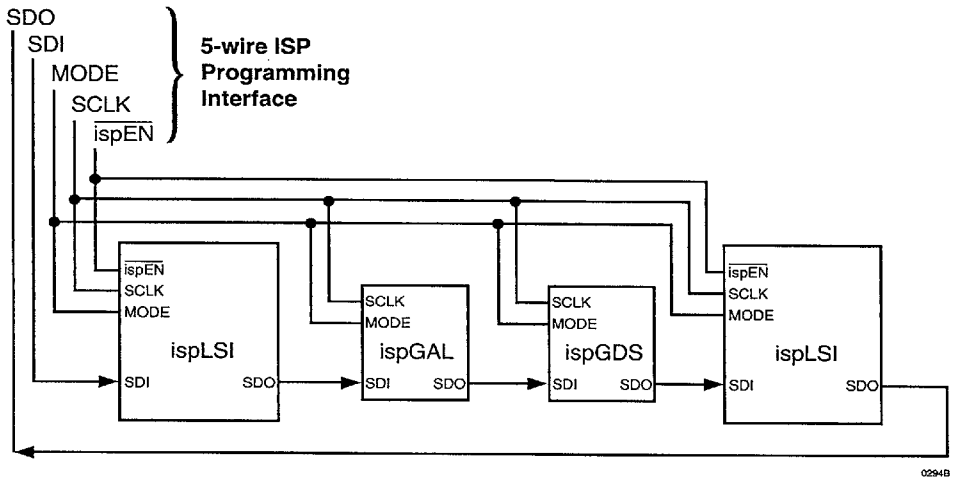
In-System Programmability

The ispLSI devices are the in-system programmable versions of the Lattice Semiconductor high density programmable Large Scale Integration (pLSI) devices. By integrating all the high voltage programming circuitry on-chip, programming can be accomplished by simply shifting data into the device. Once the function is programmed, the non-volatile E^2CMOS cells will not lose the pattern even when the power is turned off.

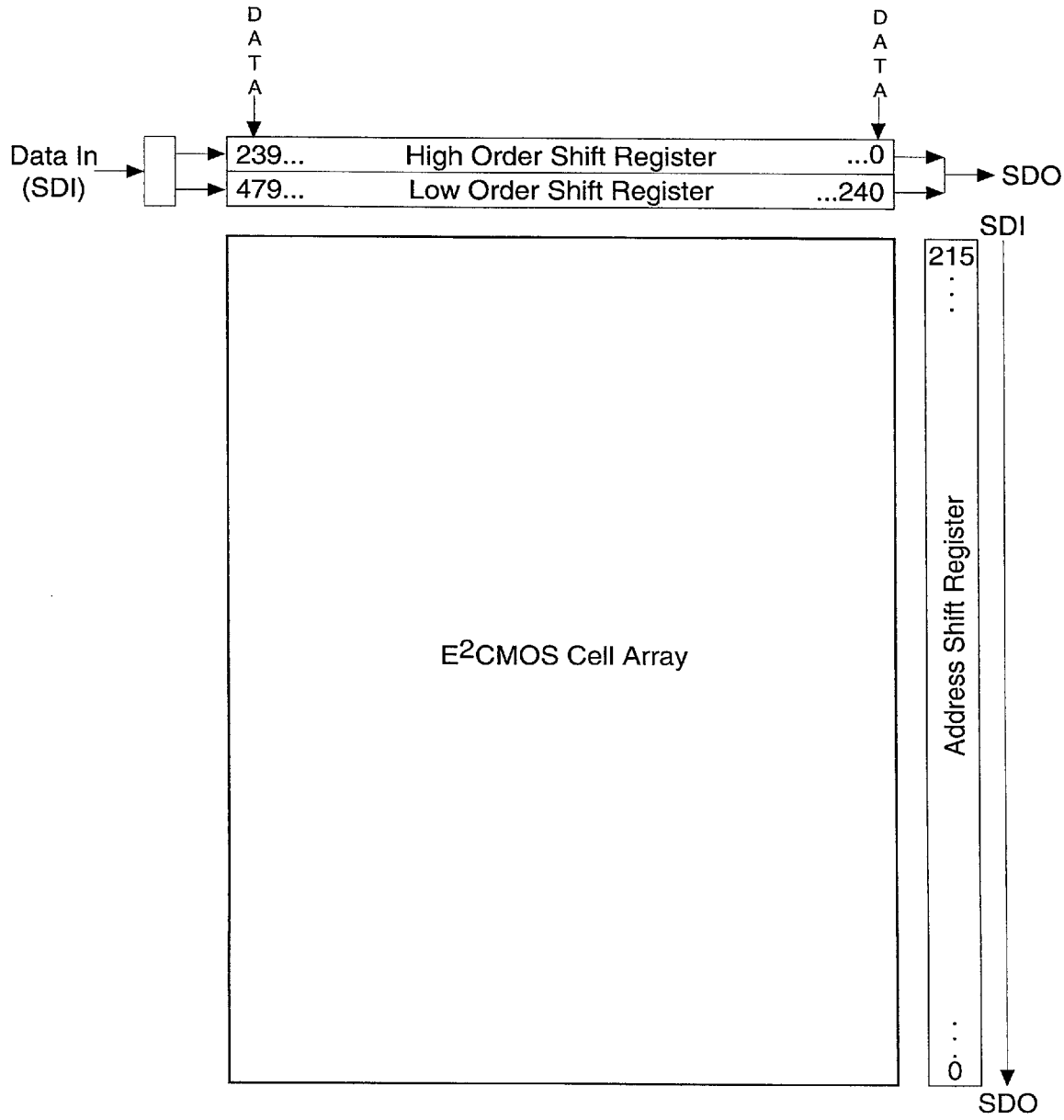
All necessary programming is done via five TTL level logic interface signals. These five signals are fed into the on-chip programming circuitry where a state machine controls the programming. The simple signals for interface include isp™ Enable ($\overline{\text{ispEN}}$), Serial Data In (SDI), Serial Data Out (SDO), Serial Clock (SCLK) and Mode (MODE) control. Figure 4 illustrates the block diagram of one possible scheme of the programming interface for the ispLSI devices. For details on the operation of the internal state machine and programming of the device please refer to the ISP Architecture and Programming section in this Data Book.

The device identifier for the ispLSI 3192 is 0010 0001 (21 hex). This code is the unique device identifier which is generated when a read ID command is performed.

Figure 4. ISP Programming Interface



ispLSI 3192 Shift Register Layout



Note: A logic "1" in the address shift register enables the row for programming or verification. A logic "0" disables it.

Lattice Semiconductor offers support for the IEEE 1149.1 Boundary Scan specification on the 3000 Family of devices.

The user interfaces to the boundary scan circuitry through the Test Access Port (TAP). The TAP consists of a control state machine, instruction decoder and instruction register.

The TAP is controlled using the test control lines: Test Data IN (TDI), Test Data Out (TDO), Test Mode Select (TMS), Test Reset ($\overline{TRST}$) and Test Clock (TCK).

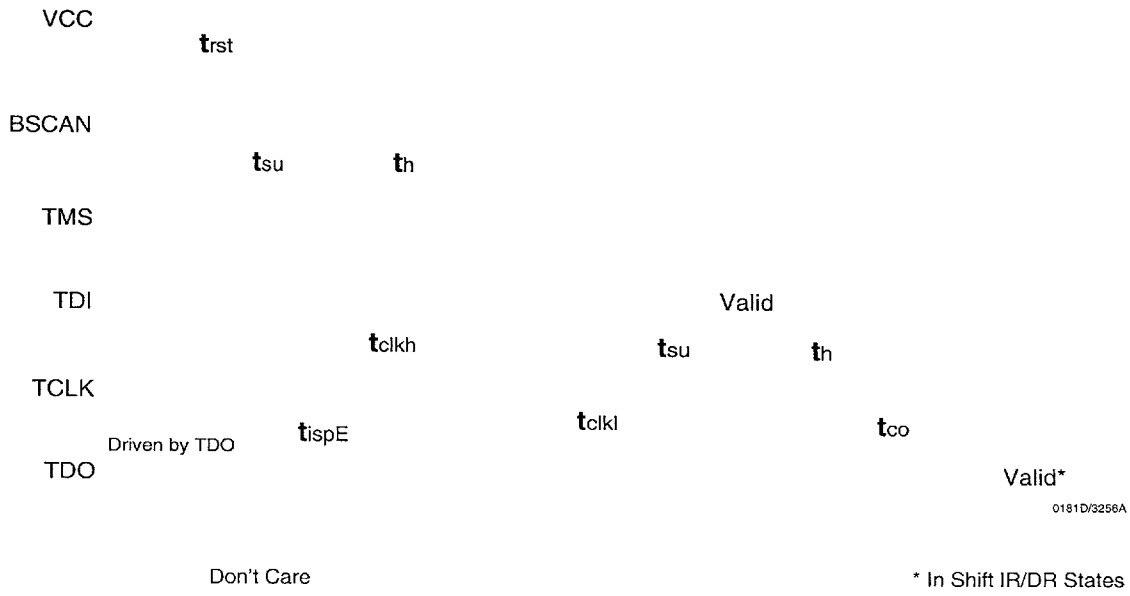
All of the input cells and I/O cells are serially connected together in a long chain. The scan out of one cell is connected to the scan in of the next cell. The cells are connected in the following order: TDI to GOE0, GOE1, Y0, Y1, Y2, Y3, Y4, TOE, $\overline{RESET}$, I/O95 thru I/O0 to I/O96 thru I/O191 to TDO.

The timing specifications for Boundary Scan are listed below. The waveforms are shown in figure 5.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
t_{rst}	Reset Time from Valid V_{CC}		100	–	–	µs
t_{su}	Setup Time		60	–	–	ns
t_h	Hold Time		10	–	–	ns
t_{co}	Clock to Output		–	–	60	ns
t_{clkh}	Clock Pulse Duration, High		60	–	–	ns
t_{clkl}	Clock Pulse Duration, Low		60	–	–	ns
t_{ispE}	$\overline{ispEN}$ / BSCAN to TDO		–	–	1	µs

Table 2 - 0028Aisp-3K/6K

Figure 5. Boundary Scan Waveforms



Pin Description

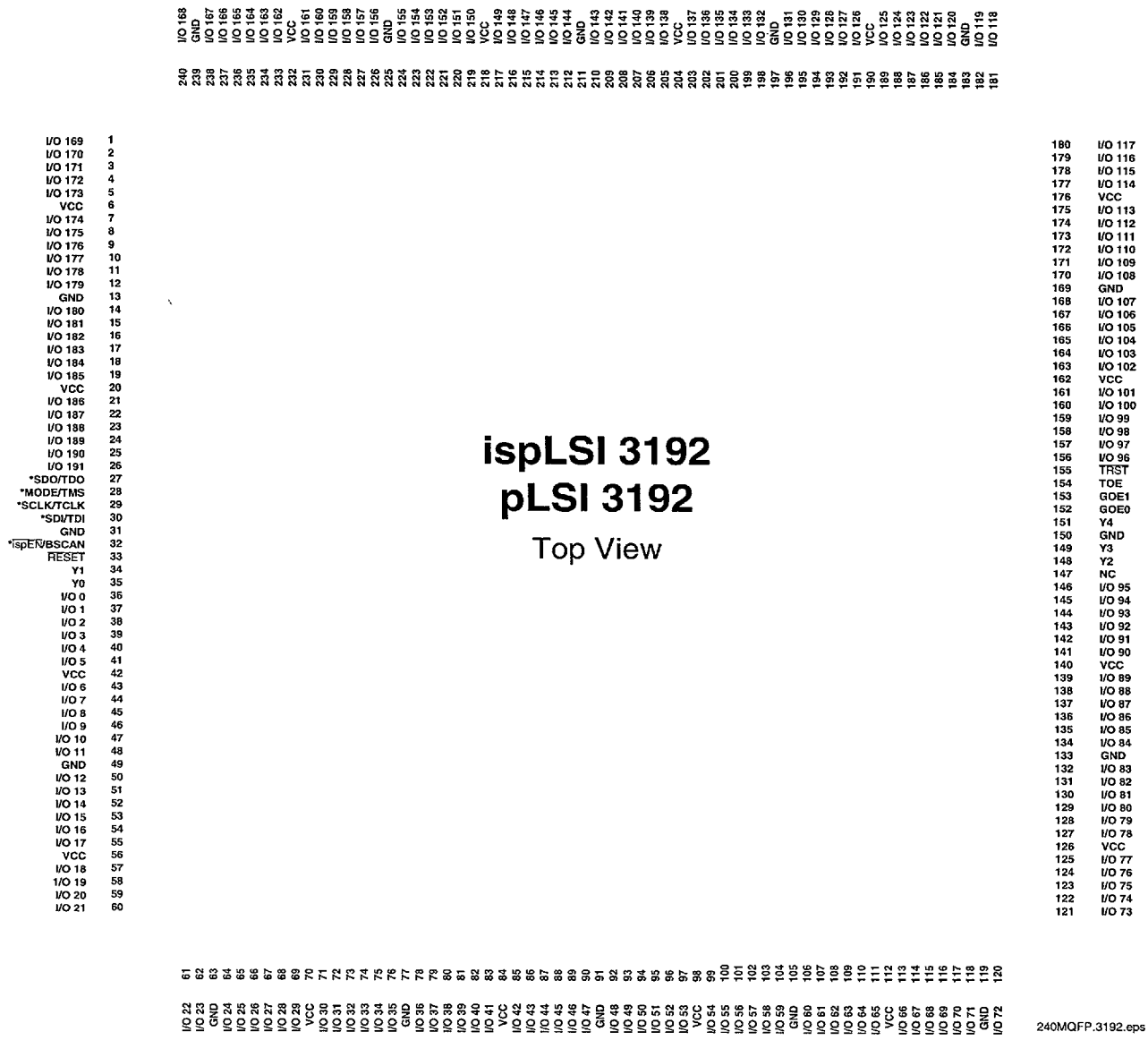
NAME	MQFP PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 5 I/O 6 - I/O 11 I/O 12 - I/O 17 I/O 18 - I/O 23 I/O 24 - I/O 29 I/O 30 - I/O 35 I/O 36 - I/O 41 I/O 42 - I/O 47 I/O 48 - I/O 53 I/O 54 - I/O 59 I/O 60 - I/O 65 I/O 66 - I/O 71 I/O 72 - I/O 77 I/O 78 - I/O 83 I/O 84 - I/O 89 I/O 90 - I/O 95 I/O 96 - I/O 101 I/O 102 - I/O 107 I/O 108 - I/O 113 I/O 114 - I/O 119 I/O 120 - I/O 125 I/O 126 - I/O 131 I/O 132 - I/O 137 I/O 138 - I/O 143 I/O 144 - I/O 149 I/O 150 - I/O 155 I/O 156 - I/O 161 I/O 162 - I/O 167 I/O 168 - I/O 173 I/O 174 - I/O 179 I/O 180 - I/O 185 I/O 186 - I/O 191	36, 37, 38, 39, 40, 41, 43, 44, 45, 46, 47, 48, 50, 51, 52, 53, 54, 55, 57, 58, 59, 60, 61, 62, 64, 65, 66, 67, 68, 69, 71, 72, 73, 74, 75, 76, 78, 79, 80, 81, 82, 83, 85, 86, 87, 88, 89, 90, 92, 93, 94, 95, 96, 97, 99, 100, 101, 102, 103, 104, 106, 107, 108, 109, 110, 111, 113, 114, 115, 116, 117, 118, 120, 121, 122, 123, 124, 125, 127, 128, 129, 130, 131, 132, 134, 135, 136, 137, 138, 139, 141, 142, 143, 144, 145, 146, 156, 157, 158, 159, 160, 161, 163, 164, 165, 166, 167, 168, 170, 171, 172, 173, 174, 175, 177, 178, 179, 180, 181, 182, 184, 185, 186, 187, 188, 189, 191, 192, 193, 194, 195, 196, 198, 199, 200, 201, 202, 203, 205, 206, 207, 208, 209, 210, 212, 213, 214, 215, 216, 217, 219, 220, 221, 222, 223, 224, 226, 227, 228, 229, 230, 231, 233, 234, 235, 236, 237, 238, 240, 1, 2, 3, 4, 5, 7, 8, 9, 10, 11, 12, 14, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 26	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE0 and GOE1 TOE	152 and 153 154	Global Output Enable input pins. Test output enable pin.
$\overline{\text{RESET}}$ Y0, Y1 and Y2 Y3 and Y4	33 35, 34, 148 149, 151	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device. Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the GLBs on the device. Dedicated Clock inputs. These clock inputs are connected to one of the clock inputs of all the I/O cells in the device.
BSCAN/$\overline{\text{ispEN}}$** TDI/SDI* TCLK/SCLK* TMS/MODE* $\overline{\text{TRST}}$ TDO/SDO*	32 30 29 28 155 27	Boundary Scan Enable. Input - Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active. Input - This pin performs two functions. It is the Test Data input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI is also used as one of the two control pins for the isp state machine. Input - This pin performs two functions. It is the Test Clock input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register. Input - This pin performs two functions. It is the Test Mode Select input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as pin to control the operation of the isp state machine. Input - Test Reset, active low to reset the Boundary Scan State Machine. Output - This pin performs two functions. When $\overline{\text{ispEN}}$ is logic low, it functions as the pin to read the isp data. When $\overline{\text{ispEN}}$ is high it functions as Test Data Out.
GND VCC	13, 31, 49, 63, 77, 91, 105, 119, 133, 150, 169, 183, 197, 211, 225, 239 6, 20, 42, 56, 70, 84, 98, 112, 126, 140, 162, 176, 190, 204, 218, 232	Ground (GND) V_{CC}

Table 2 - 0002/3192

* ispLSI 3192 only

** $\overline{\text{ispEN}}$ for ispLSI 3192 only, NC for pLSI 3192 must be left floating or tied to V_{CC}, must not be grounded or tied to any other signal.

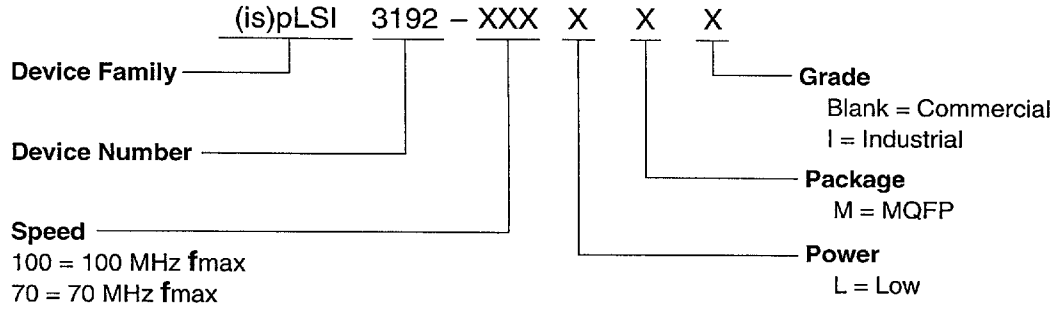
ispLSI and pLSI 3192 240-pin MQFP



240MQFP.3192.eps

*Pins have dual function capability for ispLSI 3192 only.

Part Number Description



0212/3192

Ordering Information

COMMERCIAL

Family	fmax	tpd	Ordering Number	Package
ispLSI	100	10	ispLSI 3192-100LM	240-Pin MQFP
	70	15	ispLSI 3192-70LM	240-Pin MQFP
pLSI	100	10	pLSI 3192-100LM	240-Pin MQFP
	70	15	pLSI 3192-70LM	240-Pin MQFP

41/3192

INDUSTRIAL

Family	fmax	tpd	Ordering Number	Package
ispLSI	70	15	ispLSI 3192-70LMI	240-Pin MQFP

042/3192