NB100LVEP56

2.5V / 3.3V / 5V ECL Dual Differential 2:1 Multiplexer

The NB100LVEP56 is a dual, fully differential 2:1 multiplexer. The differential data path makes the device ideal for multiplexing low skew clock or differential data signals. The device features both individual and common select inputs to address both data path and random logic applications. Common and individual selects can accept both ECL and CMOS input voltage levels. Multiple V_{BB} pins are provided.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input operation, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- Maximum Input Clock Frequency > 2.5 GHz Typical
- Maximum Input Data Rate > 2.5 Gb/s Typical
- 525 ps Typical Propagation Delays
- Low Profile QFN Package
- PECL Mode Operating Range: V_{CC} = 2.375 V to 5.5 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = -2.375 V to -5.5 V
- Separate, Common Select, and Individual Select (Compatible with ECL and CMOS Input Voltage Levels)
- Q Output Will Default LOW with Inputs Open or at V_{EE}
- Multiple V_{BB} Outputs

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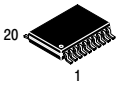
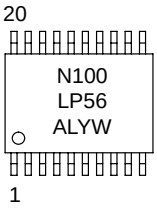
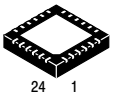
MARKING DIAGRAMS*

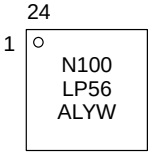


TSSOP-20
DT SUFFIX
CASE 948E





24 PIN QFN
MN SUFFIX
CASE 485L



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
NB100LVEP56DT	TSSOP-20	75 Units/Rail
NB100LVEP56DTR2	TSSOP-20	2500 Tape & Reel
NB100LVEP56MN	QFN-24	92 Units/Rail
NB100LVEP56MNR2	QFN-24	3000 Tape & Reel

Table 1. PIN DESCRIPTION

Pin No.		Name	I/O	Default State	Description
TSSOP	QFN				
14,20	3,9,18,19, 20	V_{CC}	-	-	Positive Supply Voltage. All VCC Pins must be Externally Connected to Power Supply to Guarantee Proper Operation.
11	15,24	V_{EE}	-	-	Negative Supply Voltage. All VEE Pins must be Externally Connected to Power Supply to Guarantee Proper Operation.
3,8	6,12	V_{BB0}, V_{BB1}	-	-	ECL Reference Voltage Output
1	4	D0a	ECL Input	Low	Noninverted Differential Data a Input to MUX 0. Internal 75 kΩ to V_{EE}.
2	5	$\overline{D0a}$	ECL Input	High	Inverted Differential Data a Input to MUX 0. Internal 75 kΩ to V_{EE} and 37 kΩ to V_{CC}.
4	7	D0b	ECL Input	Low	Noninverted Differential Data b Input to MUX 0. Internal 75 kΩ to V_{EE}.
5	8	$\overline{D0b}$	ECL Input	High	Inverted Differential Data b Input to MUX 0. Internal 75 kΩ to V_{EE} and 37 kΩ to V_{CC}.
6	10	D1a	ECL Input	Low	Noninverted Differential Data a Input to MUX 1. Internal 75 kΩ to V_{EE}.
7	11	$\overline{D1a}$	ECL Input	High	Inverted Differential Data a Input to MUX 1. Internal 75 kΩ to V_{EE} and 37 kΩ to V_{CC}.
9	13	D1b	ECL Input	Low	Noninverted Differential Data b Input to MUX 1. Internal 75 kΩ to V_{EE}.
10	14	$\overline{D1b}$	ECL Input	High	Inverted Differential Data b Input to MUX 1. Internal 75 kΩ to V_{EE} and 37 kΩ to V_{CC}.
19	2	Q0	ECL Output	-	Noninverted Differential Output MUX 0. Typically Terminated with 50 Ω to $V_{TT} = V_{CC}$ - 2 V.
18	1	$\overline{Q0}$	ECL Output	-	Inverted Differential Output MUX 0. Typically Terminated with 50 Ω to $V_{TT} = V_{CC}$ - 2 V.
13	17	Q1	ECL Output	-	Noninverted Differential Output MUX 1. Typically Terminated with 50 Ω to $V_{TT} = V_{CC}$ - 2 V.
12	16	$\overline{Q1}$	ECL Output	-	Inverted Differential Output MUX 1. Typically Terminated with 50 Ω to $V_{TT} = V_{CC}$ - 2 V.
17	23	SEL0	ECL, CMOS Input	Low	Noninverted Differential Select Input to MUX 0. Internal 75 Ω to V_{EE}.
16	22	COM_SEL	ECL, CMOS Input	Low	Noninverted Differential Common Select Input to Both MUX. Internal 75 Ω to V_{EE}.
15	21	SEL1	ECL, CMOS Input	Low	Noninverted Differential Select Input to MUX 1. Internal 75 Ω to V_{EE}.
N/A	-	EP	-		Exposed Pad. (Note 1)

1. The thermally conductive exposed pad on the package bottom (see case drawing) must be attached to a heat sinking conduit.

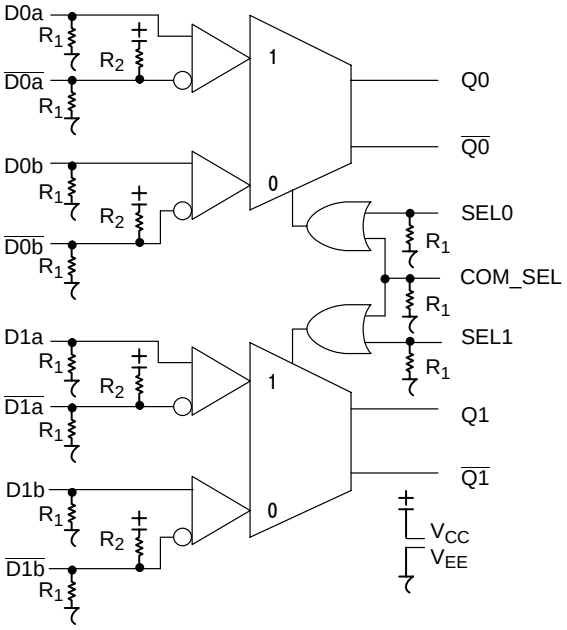


Figure 1. Logic Diagram

Table 2. TRUTH TABLE

SEL0	SEL1	COM_SEL	Q0, $\overline{Q0}$	Q1, $\overline{Q1}$
X	X	H	a	a
L	L	L	b	b
L	H	L	b	a
H	H	L	a	a
H	L	L	a	b

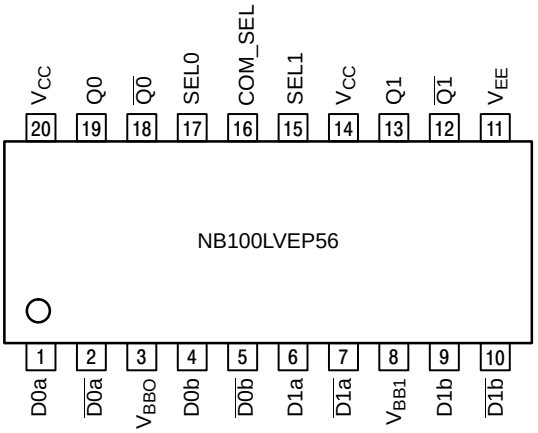


Figure 1. TSSOP-20 Lead Pinout (Top View)

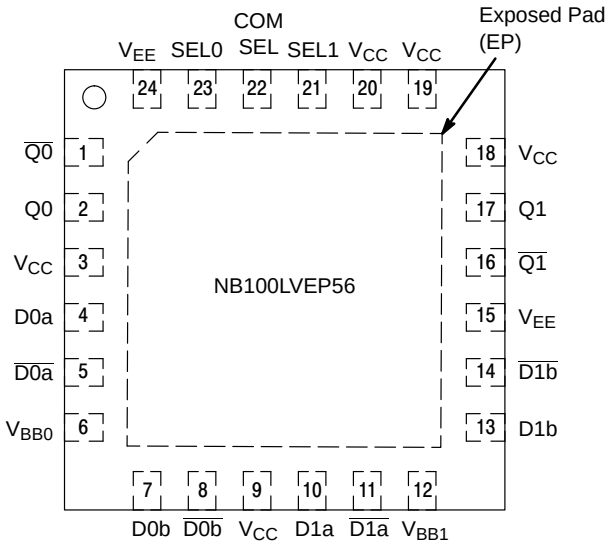


Figure 2. QFN-24 Lead Pinout (Top View)

Table 3. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor	(R1)	75 kΩ
Internal Input Pullup Resistor	(R2)	37 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 150 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		354 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Mode Power Supply	V_{EE} = 0 V		6	V
V_{EE}	Negative Mode Power Supply	V_{CC} = 0 V		-6	V
V_I	Positive Mode Input Voltage Negative Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 -6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			±0.5	mA
T_A	Operating Temperature Range			-40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) JEDEC 51-3 (1S - Single Layer Test Board)	0 LFPM 500 LFPM	20 TSSOP 20 TSSOP	140 50	°C/W °C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient) JEDEC 51-6 (2S2P-Multi Layer Test Board) with Filled Thermal Vias	0 LFPM 500 LFPM	24 QFN 24 QFN	37 32	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	20 TSSOP 24 QFN	23 to 41 11	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

Table 5. DC CHARACTERISTICS, PECL V_{CC} = 2.5 V, V_{EE} = 0 V (Note 3)

		-40 °C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Negative Power Supply Current	35	45	55	35	45	55	35	48	58	mA
V_{OH}	Output HIGH Voltage (Note 4)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{OL}	Output LOW Voltage (Note 4)	555	775	900	555	775	900	555	775	900	mV
V_{IH}	Input HIGH Voltage (SEL0, SEL1, COM_SEL) Input HIGH Voltage (D Inputs) (Note 5)	1335 1335		V_{CC} 1620	1335 1335		V_{CC} 1620	1275 1275		V_{CC} 1620	mV
V_{IL}	Input LOW Voltage (SEL0, SEL1, COM_SEL) Input LOW Voltage (D Inputs) (Note 5)	V_{EE} 555		875 875	V_{EE} 555		875 875	V_{EE} 555		875 875	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 6)	1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input HIGH Current (@V_{IH})			150			150			150	μA
I_{IL}	Input LOW Current (@V_{IL}) D $\overline{D}$ SEL	0.5 -150 -150			0.5 -150 -150			0.5 -150 -150			μA

NOTE: LVEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

3. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.125 V to -1.3 V.
4. All loading with 50 Ω to V_{CC}-2.0 V.
5. Do not use V_{BB} at V_{CC} < 3.0 V.
6. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 6. DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 7)

		-40 °C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Negative Power Supply Current	35	45	55	35	45	55	35	48	58	mA
V_{OH}	Output HIGH Voltage (Note 8)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 8)	1355	1575	1700	1355	1575	1700	1355	1575	1700	mV
V_{IH}	Input HIGH Voltage (SEL0, SEL1, COM_SEL) Input HIGH Voltage (D Inputs)	2135 2135		V_{CC} 2420	2135 2135		V_{CC} 2420	2135 2135		V_{CC} 2420	mV
V_{IL}	Input LOW Voltage (SEL0, SEL1, COM_SEL) Input LOW Voltage (D Inputs)	V_{EE} 1355		1675 1675	V_{EE} 1355		1675 1675	V_{EE} 1355		1675 1675	mV
V_{BB}	Output Reference Voltage (Note 9)	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 10)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current (@V_{IH})			150			150			150	μA
I_{IL}	Input LOW Current (@V_{IL}) D $\overline{D}$ SEL	0.5 -150 -150			0.5 -150 -150			0.5 -150 -150			μA

NOTE: LVEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

7. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925 V to -0.5 V.
8. All loading with 50 Ω to V_{CC}-2.0 V.
9. Single-Ended input operation is limited to $V_{CC} \geq$ 3.0 V in PECL mode.
10. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 7. DC CHARACTERISTICS, PECL V_{CC} = 5.0 V, V_{EE} = 0 V (Note 11)

		-40 °C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Negative Power Supply Current	40	50	60	40	50	60	45	55	65	mA
V_{OH}	Output HIGH Voltage (Note 12)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
V_{OL}	Output LOW Voltage (Note 12)	3055	3275	3400	3055	3275	3400	3055	3275	3400	mV
V_{IH}	Input HIGH Voltage (SEL0, SEL1, COM_SEL) Input HIGH Voltage (D Inputs)	3775 3775		V_{CC} 4120	3775 3775		V_{CC} 4120	3775 3775		V_{CC} 4120	mV
V_{IL}	Input LOW Voltage (SEL0, SEL1, COM_SEL) Input LOW Voltage (D Inputs)	V_{EE} 3055		3375 3375	V_{EE} 3055		3375 3375	V_{EE} 3055		3375 3375	mV
V_{BB}	Output Voltage Reference	3475	3575	3675	3475	3575	3675	3475	3575	3675	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13)	1.2		5.0	1.2		5.0	1.2		5.0	V
I_{IH}	Input HIGH Current (@V_{IH})			150			150			150	μA
I_{IL}	Input LOW Current (@V_{IL}) D $\overline{D}$ SEL	0.5 -150 -150			0.5 -150 -150			0.5 -150 -150			μA

NOTE: LVEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

11. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +2.0 V to -0.5 V.
12. All loading with 50 ohms to V_{CC}-2.0 V.
13. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 8. DC CHARACTERISTICS, NECL V_{CC} = 0 V, V_{EE} = -3.8 V to -2.375 V (Note 14)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current	35	45	55	35	45	55	35	48	58	mA
V_{OH}	Output HIGH Voltage (Note 15)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
V_{OL}	Output LOW Voltage (Note 15)	-1945	-1725	-1600	-1945	-1725	-1600	-1945	-1725	-1600	mV
V_{IH}	Input HIGH Voltage (SEL0, SEL1, COM_SEL) Input HIGH Voltage (D Inputs)	-1165 -1165		V_{CC} -880	-1165 -1165		V_{CC} -880	-1165 -1165		V_{CC} -880	mV
V_{IL}	Input LOW Voltage (SEL0, SEL1, COM_SEL) Input LOW Voltage (D Inputs)	V_{EE} -1945		-1600 -1600	V_{EE} -1945		-1600 -1600	V_{EE} -1945		-1600 -1600	mV
V_{BB}	Output Reference Voltage (Note 16)	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 17)	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V
I_{IH}	Input HIGH Current (@V_{IH})			150			150			150	μA
I_{IL}	Input LOW Current (@V_{IL}) D $\overline{D}$ SEL	0.5 -150 -150			0.5 -150 -150			0.5 -150 -150			μA

NOTE: LVEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

14. Input and output parameters vary 1:1 with V_{CC}.
15. All loading with 50 Ω to V_{CC}-2.0 V.
16. Single-Ended input operation is limited to V_{EE} from -3.0 V to -5.5 V in NECL mode.
17. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 9. DC CHARACTERISTICS, NECL V_{CC} = 0 V, V_{EE} = -3.8 V to -5.5 V (Note 18)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Negative Power Supply Current	40	50	60	40	50	60	45	55	65	mA
V_{OH}	Output HIGH Voltage (Note 19)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
V_{OL}	Output LOW Voltage (Note 19)	-1945	-1725	-1600	-1945	-1725	-1600	-1945	-1725	-1600	mV
V_{IH}	Input HIGH Voltage (SEL0, SEL1, COM_SEL) Input HIGH Voltage (D Inputs)	-1165 -1165		V_{CC} -880	-1165 -1165		V_{CC} -880	-1165 -1165		V_{CC} -880	mV
V_{IL}	Input LOW Voltage (SEL0, SEL1, COM_SEL) Input LOW Voltage (D Inputs)	V_{EE} -1945		-1600 -1625	V_{EE} -1945		-1600 -1625	V_{EE} -1945		-1600 -1625	mV
V_{BB}	Output Reference Voltage (Note 20)	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 21)	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V
I_{IH}	Input HIGH Current (@V_{IH})			150			150			150	μA
I_{IL}	Input LOW Current (@V_{IL}) D $\overline{D}$ SEL	0.5 -150 -150			0.5 -150 -150			0.5 -150 -150			μA

NOTE: LVEP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

18. Input and output parameters vary 1:1 with V_{CC}.
19. All loading with 50 Ω to V_{CC}-2.0 V.
20. Single-Ended input operation is limited to V_{EE} from -3.0 V to -5.5 V in NECL mode.
21. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 10. AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = -2.375 V to -3.8 V or V_{CC} = 2.375 V to 3.8 V; V_{EE} = 0 V (Note 22)

		-40 °C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{OUTPP}	Output Voltage Amplitude $f_{in} \leq$ 1 GHz (See Figure 2) f_{in} = 2 GHz f_{in} = 2.5 GHz	525 500 400	700 600 500		550 500 350	700 600 450		500 400 200	700 500 300		mV
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential D to Q, $\overline{Q}$ SEL to Q, $\overline{Q}$ COM_SEL to Q, $\overline{Q}$	 375 575 550	 500 775 750	 625 975 950	 400 625 600	 525 825 800	 650 1025 1000	 450 700 700	 575 900 900	 700 1100 1100	ps
t_{Skew}	Pulse Skew (Note 23) Within Device Input Skew (Note 24) Within Device Output Skew (Note 25) Device-to-Device Skew (Note 26)		10 5 15 50	50 30 50 200		10 5 15 50			10 5 15 50	50 30 50 200	ps
t_{JITTER}	RMS Random Clock Jitter f_{in} = 2.5 GHz (Note 27) Peak-to-Peak Data Dependent Jitter f_{in} =1.5 Gb/s (Note 28) f_{in} = 2.5 Gb/s		 5 15	1		 10 25	1		 10 25	1	ps
V_{INPP}	Input Voltage Swing (Differential Configuration) (Note 29)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times @ 50 MHz Q, $\overline{Q}$ (20% - 80%)	60	110	150	60	120	170	90	140	230	ps

22. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC}-2.0 V. Input edge rates 150 ps (20% - 80%).
23. Pulse Skew $|t_{PLH} - t_{PHL}|$
24. Worst case difference between D0a and D0b (or between D1a or D1b), when both output come from same input.
25. Worst case difference between Q0 and Q1 outputs.
26. Skew is measured between outputs under identical transitions.
27. Additive RMS jitter with 50% Duty Cycle Clock Signal at f_{in} = 2.5 GHz.
28. Additive Peak-to-Peak jitter with input NRZ data at PRBS 2^{31}-1 at f_{in} = 2.5 Gb/s.
29. Input voltage swing is a single-ended measurement operating in differential mode.

Table 11. AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = -4.2 V to -5.5 V or V_{CC} = 4.2 V to 5.5 V; V_{EE} = 0 V (Note 30)

		-40 °C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{OUTPP}	Output Voltage Amplitude $f_{in} \leq$ 1 GHz (See Figure 3) f_{in} = 2 GHz f_{in} = 2.5 GHz	600 550 400	750 650 550		600 500 350	750 600 450		600 400 200	750 500 300		mV
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential D to Q, $\overline{Q}$ SEL to Q, $\overline{Q}$ COM_SEL to Q, $\overline{Q}$	 375 575 550	 500 775 750	 625 975 950	 400 625 600	 525 825 800	 650 1025 1000	 450 700 700	 575 900 900	 700 1100 1100	ps
t_{Skew}	Pulse Skew (Note 31) Within Device Input Skew (Note 32) Within Device Output Skew (Note 33) Device-to-Device Skew (Note 34)		5 15 20 50	50 30 50 200		5 15 20 50	50 30 50 200		5 15 20 50	50 30 50 200	ps
t_{JITTER}	RMS Random Clock Jitter f_{in} = 2.5 GHz (Note 35) Peak-to-Peak Data Dependent Jitter f_{in} =1.5 Gb/s (Note 36) f_{in} = 2.5 Gb/s		 5 15	1		 10 25	1		 10 20	1	ps
V_{INPP}	Input Voltage Swing (Differential Configuration) (Note 37)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times @ 50 MHz Q, $\overline{Q}$ (20% - 80%)	60	110	150	60	120	170	90	140	230	ps

30. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC}-2.0 V. Input edge rates 150 ps (20% - 80%).
31. Pulse Skew $|t_{PLH} - t_{PHL}|$
32. Worst case difference between D0a and D0b (or between D1a or D1b), when both output come from same input.
33. Worst case difference between Q0 and Q1 outputs.
34. Skew is measured between outputs under identical transitions.
35. Additive RMS jitter with 50% Duty Cycle Clock Signal at f_{in} = 2.5 GHz.
36. Additive Peak-to-Peak jitter with input NRZ data at PRBS 2^{31}-1 at f_{in} = 2.5 Gb/s.
37. Input voltage swing is a single-ended measurement operating in differential mode.

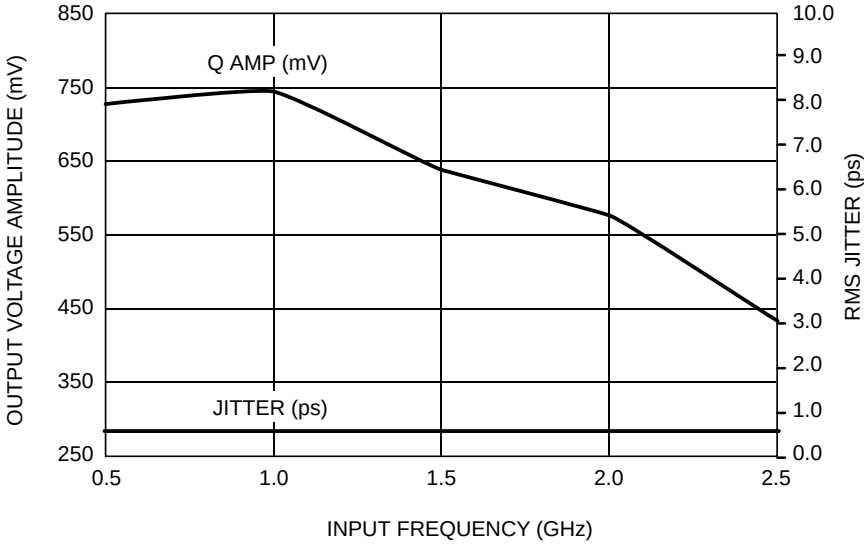


Figure 2. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) at V_{CC} = 2.5 V, 25°C

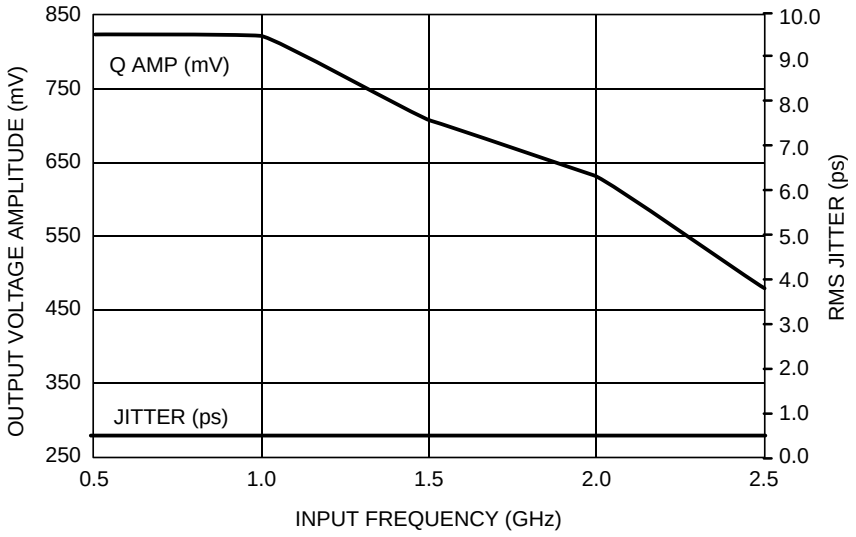


Figure 3. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) at V_{CC} = 5.0 V, 25°C

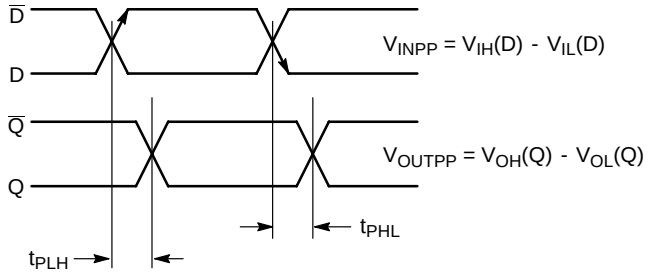


Figure 4. AC Reference Measurement

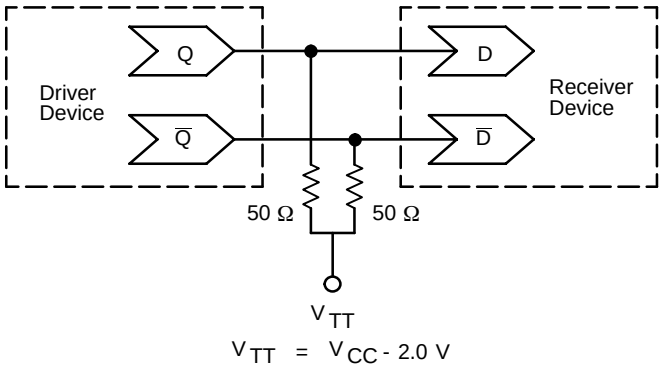


Figure 5. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 - Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 - ECLinPS Circuit Performance at Non-Standard V_{IH} Levels

AN1405 - ECL Clock Distribution Techniques

AN1406 - Designing with PECL (ECL at +5.0 V)

AN1504 - Metastability and the ECLinPS Family

AN1568 - Interfacing Between LVDS and ECL

AN1672 - The ECL Translator Guide

AND8002 - Marking and Date Codes

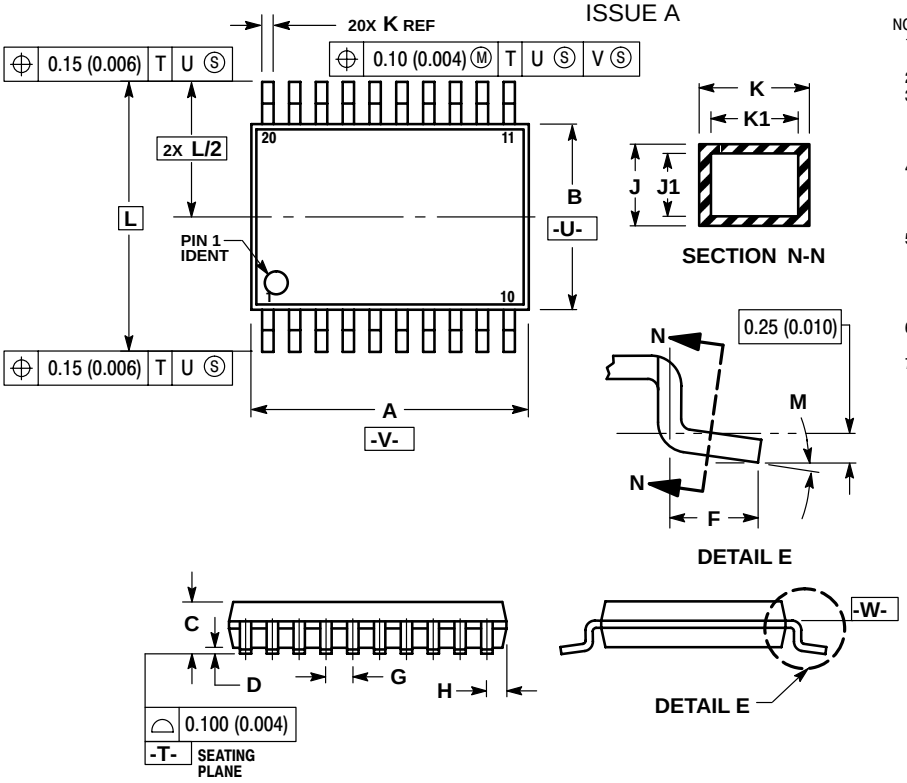
AND8009 - ECLinPS Plus Spice I/O Model Kit

AND8020 - Termination of ECL Logic Devices

For an updated list of Application Notes, please see our website at http://onsemi.com.

PACKAGE DIMENSIONS

TSSOP-20
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948E-02
ISSUE A

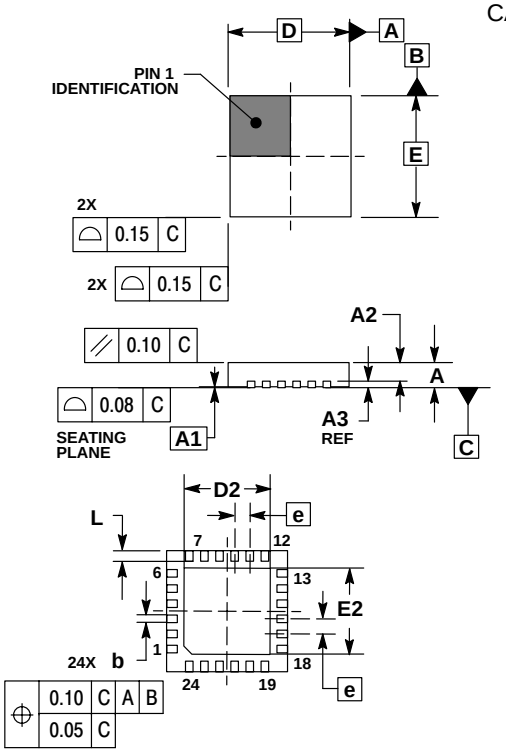


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. ICONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

PACKAGE DIMENSIONS

QFN 24
MN SUFFIX
24 PIN QFN, 4x4
CASE 485L-01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.80
A3	0.20 REF	
b	0.23	0.28
D	4.00 BSC	
D2	2.70	2.90
E	4.00 BSC	
E2	2.70	2.90
e	0.50 BSC	
L	0.35	0.45

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