LXP2176
T1 Receive Buffer

General Description

The LXP2176 is one of a family of Level One T1 interface solutions and is compatible with the LXT300/301 Transceiver, the LXP2180A Framer/Formatter, and the LXP600/601 Clock Rate Adapter. The LXP2176 is a low-power CMOS device specifically designed for synchronizing receive side loop-timed T-carrier data streams with system side timing. The device has several flexible operating modes which simplify interfacing incoming data to parallel and serial TDM backplanes. The device extracts, buffers and integrates ABCD signaling; signaling updates are prohibited during alarm or slip conditions. The buffer replaces extensive hardware in existing applications with one integrated chip. The LXP2176 is a fully pin-compatible drop-in replacement for the DS2176.

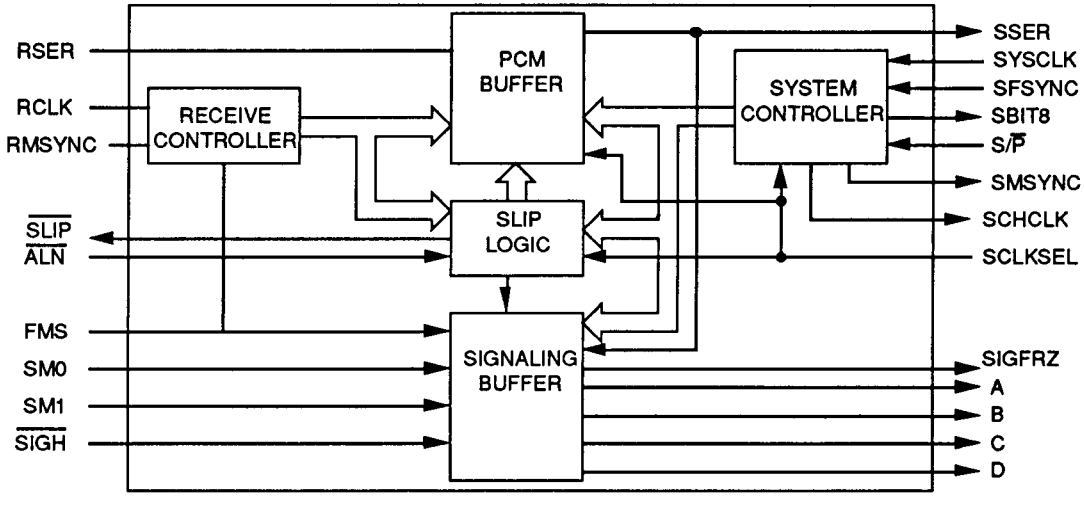
Applications

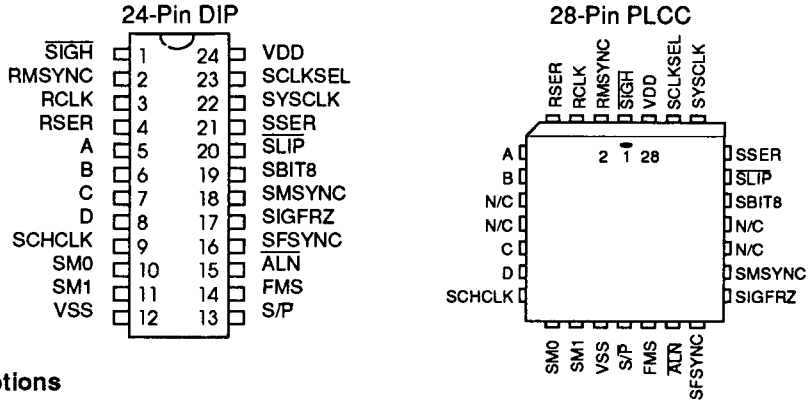
- Digital Trunks
- Drop and Insert Equipment
- Transcoders
- Digital Cross-connects (DACS)
- Private Network Equipment
- PABX-to-computer interfaces such as DMI and CPI.

Features

- Drop-in replacement for the DS2176
- Synchronizes loop-timed and system timed TI data streams
- Two-frame buffer depth; slips occur on frame boundaries
- Output indicates when slip occurs
- Buffer may be recentered externally
- Ideal for 1.544 to 2.048 MHz rate conversion
- Interfaces to parallel or serial backplanes
- Extracts and buffers robbed-bit signaling
- Inhibits signaling updates during alarm or slip conditions
- Integration feature "debounces" signaling
- Slip-compensated output indicates when signaling updates occur
- Compatible with LXP2180A T1 framer/formatter
- Choice of 24-pin DIP or 28-pin PLCC (surface mount)

Figure 1: Block Diagram





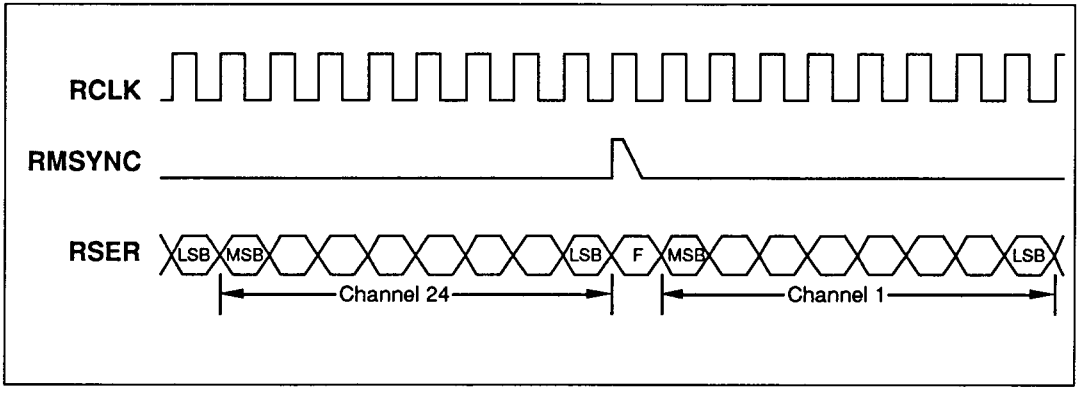
Pin Descriptions

Pin DIP	Pin PLCC	Sym	I/O	Name	Description
1	1	$\overline{\text{SIGH}}$	I	Signaling Inhibit	When low, ABCD signaling updates are disabled for a period determined by SM0 and SM1, or until returned high.
2	2	RMSYNC	I	Receive Multi-frame Sync	Must be pulsed high at multiframe boundaries to establish frame and multiframe alignment.
3	3	RCLK	I	Receive Clock	Primary 1.544 MHz clock.
4	4	RSER	I	Receive Serial Data	Sampled on falling edge of RCLK.
5 6 7 8	5 6 9 10	A B C D	O	RBS Outputs	Robbed-Bit Signaling Outputs
9	11	SCHCLK	I	System Channel Clock	Transitions high on channel boundaries; useful for serial-to-parallel conversion of channel data.
10 11	12 13	SM0 SM1	O	Signaling Modes 0 and 1	Select signaling supervision technique.
12	14	VSS	–	Signal Ground	Signal Ground. 0.0 volts.
13	15	S/$\overline{\text{P}}$	I	Serial Parallel Select	Tie to VSS for parallel backplane applications, to VDD for serial.
14	16	FMS	I	Frame Mode Select	Tie to VSS to select 193S (D4) framing, to VDD for 193E (extended).
15	17	$\overline{\text{ALN}}$	I	Align	Recenters buffer on next system side frame boundary when forced low.
16	18	SFSYNC	I	System Frame Sync	Rising edge establishes start of frame.

Pin Descriptions continued

Pin		Sym	I/O	Name	Description
DIP	PLCC				
17	19	SIGFRZ	O	Signaling Freeze	When high, indicates signaling updates have been disabled internally via a slip or externally by forcing $\overline{SIGH}$ low.
18	20	SMSYNC	O	System Multi-frame Sync	Slip-compensated multiframe output; indicates when signaling updates are made.
19	23	SBIT8	I	System Bit 8	High during the LSB time of each channel. Used to reinsert extracted signaling into outgoing data stream.
20	24	$\overline{SLIP}$	O	Frame Slip	Active low, open collector output. Held low for 64 SCLK cycles when a slip occurs.
21	25	SSER	O	System Serial Output	Updated on rising edge of SYSCLK.
22	26	SYSCLK	I	System Clock	1.544 or 2.048 MHz data clock.
23	27	SCLKSEL	I	System Clock Select	Tie to VSS for 1.544 MHz applications, to VDD for 2.048 MHz.
24	28	VDD	I	Positive Supply	+5 Volt power supply input.

Figure 2: Receive Side Timing



OVERVIEW

The LXP2176 performs two primary functions:

1) Synchronization of received T1 PCM data (looped timed) to host backplane frequencies
2) Supervision of robbed-bit signalling data embedded in the data stream.

The buffer, while optimized for use with the LXP2180A T1 Framer/formatter, is also compatible with other framers and transceivers. The LXP2180A data sheet should serve as a valuable reference when designing with the LXP2176.

DATA SYNCHRONIZATION

PCM Buffer

The LXP2176 utilizes a two-frame buffer (386 bits) to synchronize incoming PCM data to the system backplane clock. The buffer samples data at RSER on the falling edge of RCLK. Output data appears at SSER and is updated on the rising edge of SYSCLK. A rising edge at RMSYNC establishes receive side frame and multiframe alignment as shown in Figure 2. A rising edge at SFSYNC establishes system side frame alignment. The buffer depth is constantly monitored by on-board contention logic, a "slip" occurs when the buffer is completely emptied or filled. Slips automatically recenter the buffer to a one-frame depth and always occur on frame boundaries.

Slip Correction Capability

The two-frame buffer depth is adequate for most T-carrier applications where short-term jitter synchronization, rather than correction of significant frequency differences, is required. The LXP2176 provides a balance between total delay and slip correction capability.

Buffer Recentering

$\overline{\text{SLIP}}$ is held low for 65 SYSCLK cycles when a slip occurs. $\overline{\text{SLIP}}$ is an active-low, open-collector output.

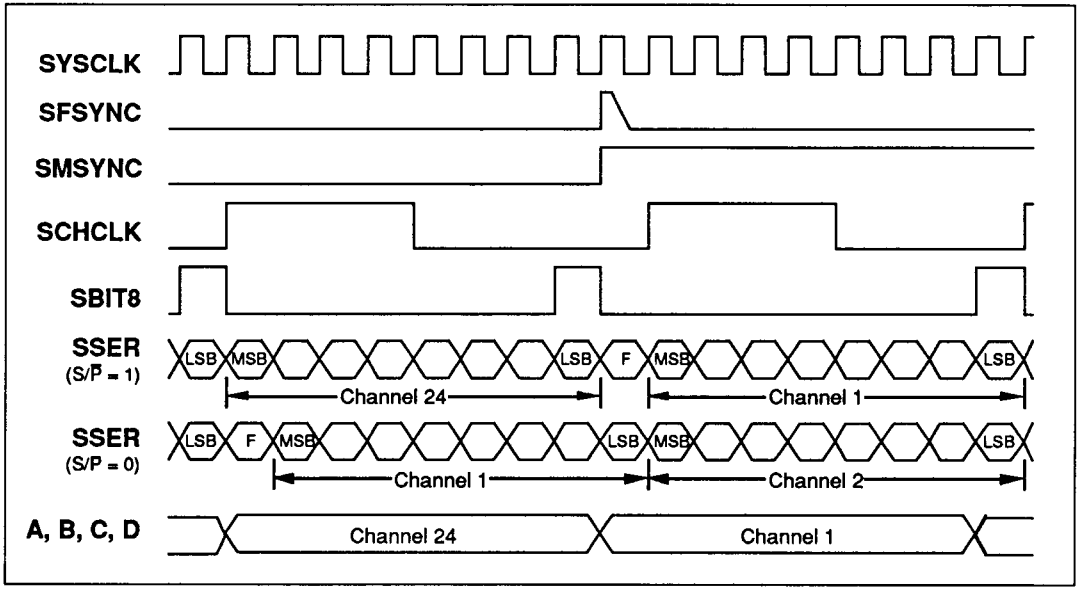
Buffer Depth Monitoring

SMSYNC is a system side output pulse which indicates system side multiframe boundaries. The distance between rising edges at RMSYNC and SMSYNC indicates the current buffer depth. Slip direction and/or an impending slip condition may be determined by monitoring RMSYNC and SMSYNC in real time. SMSYNC is held high for 65 SYSCLK cycles.

Clock Select

The LXP2176 is compatible with two common backplane frequencies: 1.544 MHz, selected when SCLKSEL=0; and 2.048 MHz, selected when SCLKSEL= 1. In 1.544 MHz

Figure 3: System Multiframe Boundary Timing (SYSCLK = 1.544 MHz)



applications the F-bit is passed through the receive buffer and presented at SSER immediately after a rising edge on SFSYNC. The F-bit is dropped in 2.048 MHz applications and the MSB of channel 1 appears at SSER one bit period after a rising edge at SFSYNC. SSER is forced to 1 in all channels greater than 24. See Figures 3 and 4.

In 2.048 MHz applications (SCLKSEL=1), the PCM buffer control logic establishes slip criteria different from that used in 1.544 MHz applications to compensate for the faster system-side read frequency.

Figure 4: System Multiframe Boundary Timing (SYSCLK = 2.048 MHz)

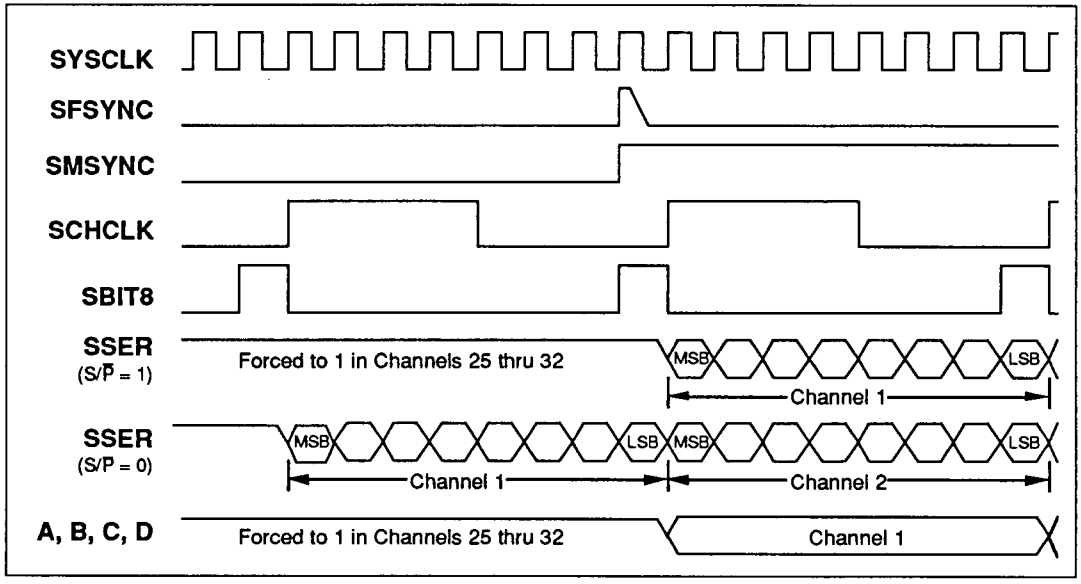


Figure 5: 193S System Multiframe Timing

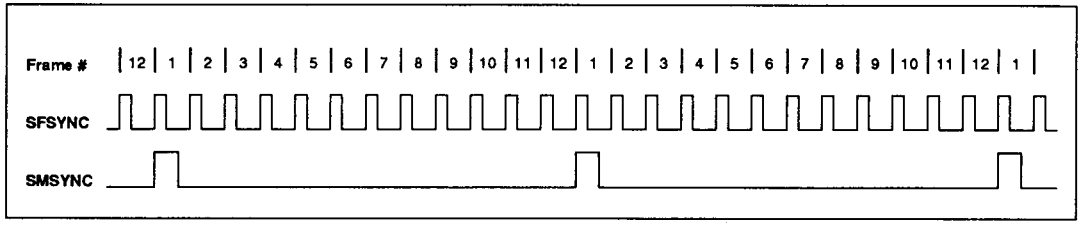
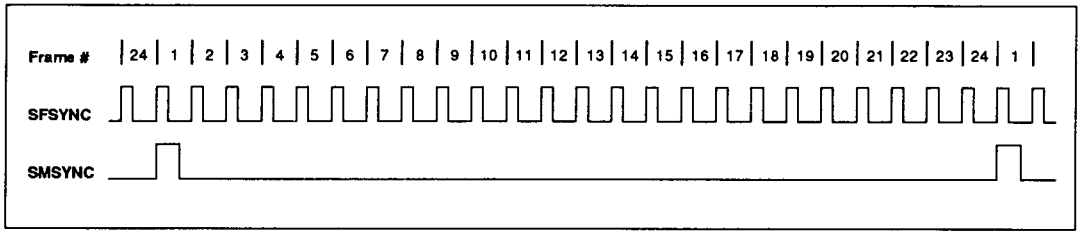


Figure 6: 193E System Multiframe Timing



Parallel Compatibility

The LXP2176 is compatible with parallel and serial backplanes. Channel 1 data appears at SSER after a rising edge at SFSYNC as shown in Figures 3 and 4 (serial applications, S/$\overline{P}$ = 1). The device utilizes a look-ahead circuit in parallel applications (S/$\overline{P}$ = 0). Data is output 8 clocks earlier, allowing a user to parallel convert data externally.

SIGNALING SUPERVISION

Extraction

In digital channel banks, robbed bit signaling data is inserted into the LSB of each channel during signaling frames. In 193S framing (FMS = 0) applications, A signaling data is inserted into frame 6 and B signaling data is inserted into frame 12. 193E framing (FMS = 1) includes two additional signaling bits: C signaling data is inserted into frame 18 and D signaling data is inserted into frame 24. This embedded signaling data is synchronized to system side timing (via the PCM buffer) before being extracted and presented at outputs A, B, C, and D. Outputs A, B, C and D are valid for each individual channel time and are repeated per channel for all frames of the multiframe. In 193S applications, outputs C and D contain the previous multiframe's A and B data. Signaling updates occur once per multiframe, at the rising edge of SMSYNC unless prohibited by a freeze.

Freeze

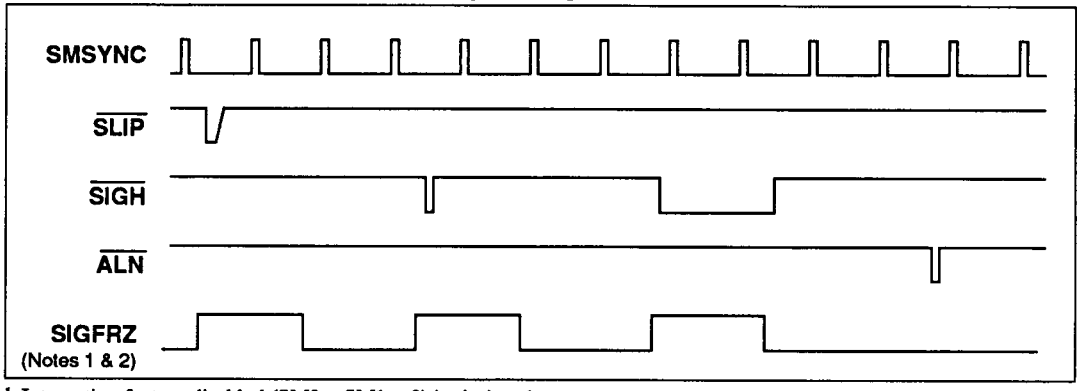
The signaling buffer allows the LXP2176 to "freeze" (prevent update of) signaling information during alarm or slip conditions. A slip condition or forcing $\overline{SIGH}$ low freezes signaling; duration of the freeze is dependent on SM0 and SM1. Updates will be unconditionally prohibited when $\overline{SIGH}$ is held low. During freezing conditions "old" data is recirculated in the output registers and appears at A,B,C and D. SIGFRZ is held high during the freeze condition, and returns low on the next signaling update. Input to output delay of signaling data is equal to one multiframe (the depth

Table 2: Signaling Supervision Modes

SM0	SM1	FMS	Selected Mode
0	0	0	193S framing, no integration, 1 multiframe freeze.
0	0	1	193E framing, no integration, 1 multiframe freeze.
0	1	0	193S framing, 2 multiframes integration and freeze.
0	1	1	193E framing, 2 multiframes integration and freeze.
1	0	0[1]	193S framing, 5 multiframes integration, 2 multiframes freeze.
1	0	1[1]	193E framing, 3 multiframes integration, 2 multiframes freeze.
1	1	0	Test mode.
1	1	1	Test mode.

[1] During slip or alarm conditions, integration is limited to 2 multiframes to minimize signaling delay.

Figure 7: Slip and Signaling Supervision Logic Timing



[1] Integration feature disabled (SM0 = SM1 = 0) in timing shown.

[2] Depending on present buffer depth, forcing $\overline{ALN}$ low may or may not cause a slip condition.

of the signaling buffer) + the current depth of the PCM buffer (1 frame + approximately 1 frame).

Integration

Signaling integration is another feature of the LXP2176. When selected, it minimizes the impact of random noise hits on the span and resultant robbed-bit signaling corruption. Integration requires that per-channel signaling data be in the same state for two or more multiframes before appearing at A, B, C, and D. SM0 and SM1 are used to select the degree of integration or to bypass the feature totally. Integration is limited to two multiframes during slip or alarm conditions to minimize update delay.

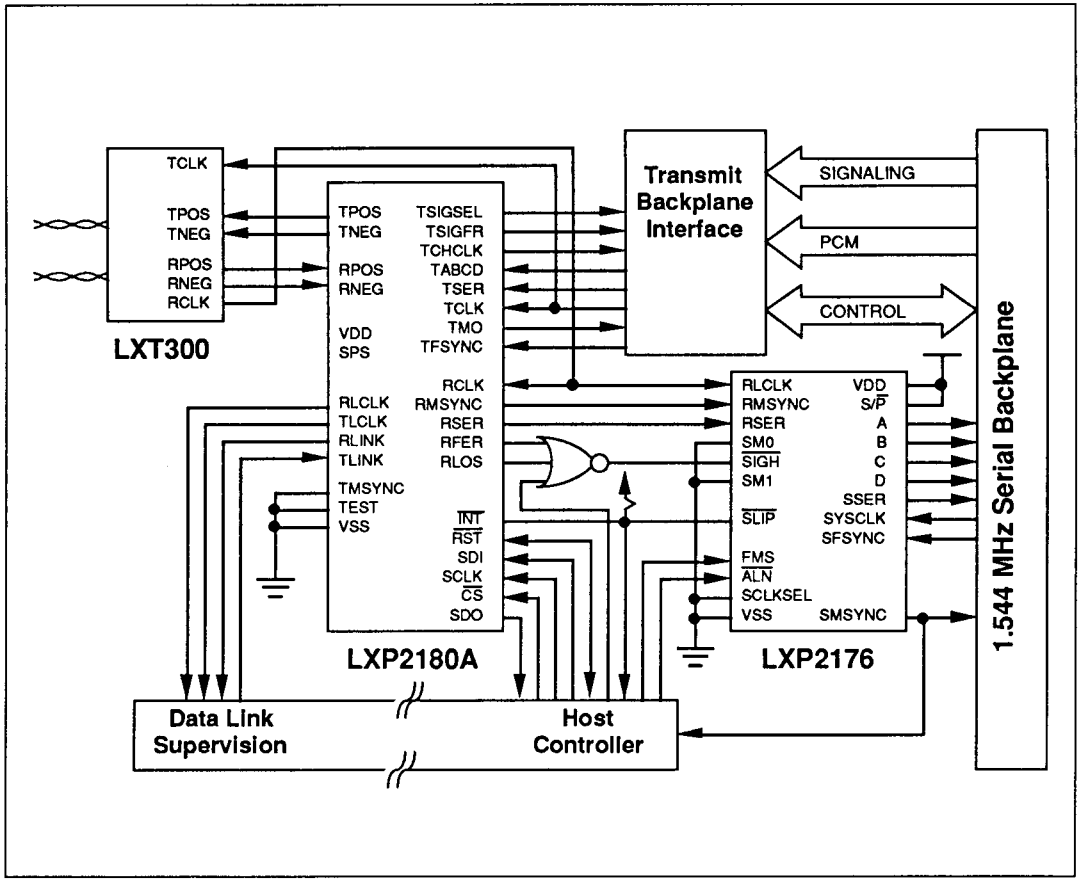
Clear Channel Considerations

The LXP2176 does not merge the "processed" signaling information with outgoing PCM data at SSER. This assures integrity of data in clear channel applications. SBIT8 indicates the LSB position of each channel. When combined with off-chip support logic, it allows the user to selectively insert robbed-bit signaling data into the outgoing data stream.

LXP2176/LXP2180A System Application

Figure 8 shows how the LXP2180A T1 Framer/Formatter and the LXP2176 Receive Buffer interconnect in a typical application.

Figure 8: Serial 1.544 MHz Backplane Interface Application



Absolute Maximum Ratings*

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

- Voltage on any pin relative to ground -1.0V to + 7V
- Operating temperature -40 °C (min) to 85 °C (max)
- Storage temperature -55 °C (min) to 125 °C (max)
- Soldering temperature 260 °C for 10 seconds

Recommended Operating Conditions (Voltages are with respect to ground (GND) unless otherwise stated)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Logic 1	V_{IH}	2.0	–	V_{DD} + .3	V	
Logic 0	V_{IL}	-0.3	–	+0.8	V	
Supply voltage	V_{DD}	4.5	5	5.5	V	
Capacitance						
Input capacitance	C_{IN}	–	–	5	pF	
Output capacitance	C_{OUT}	–	–	7	pF	
DC Electrical Characteristics - Clocked operation over recommended temperature and power supply ranges						
Supply current	I_{DD}	–	6	10	mA	See Notes 2 and 3
Input leakage	I_{IL}	-1.0	–	+1.0	µA	
Output high current	I_{OH}	-1.0	–	–	mA	V_{OH} = 2.4 V, See Note 4
Output low current	I_{OL}	+4.0	–	–	mA	V_{OL} = 0.4 V, See Note 5
Output leakage	I_{LO}	-1.0	–	+1.0	µA	See Note 6

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
[2] TCLK = RCLK = 1.544 MHz
[3] Outputs Open
[4] All outputs except $\overline{SLIP}$, which is open collector.
[5] All outputs.
[6] Applies to $\overline{SLIP}$ when tristated.

A.C. Electrical Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units
RCLK Period	t_{RCLK}	250	648		ns
RCLK, SYSCLK Rise and Fall	t_R, t_F			20	ns
RCLK Pulse Width	t_{RWH}, t_{RWL}	125	324		ns
SYSCLK Pulse Width	t_{SWH}, t_{SWL}	100	244		ns
SYSCLK Period	t_{SCLK}	200	488		ns
RMSYNC Setup to RCLK Rising	t_{SC}	$-t_{RWH}/2$		$+t_{RWL}/2$	ns
SFSYNC Setup to SYSCLK Rising	t_{SC}	$-t_{SWH}/2$		$+t_{SWL}/2$	ns
RMSYNC, SFSYNC, $\overline{SIGH}$, $\overline{ALN}$ Pulse Width	t_{PW}	100			ns
RSER Setup to RCLK Falling	t_{SD}	50			ns
RSER Hold from RCLK Falling	t_{HD}	50			ns
Propagation Delay SYSCLK to SSER, A, B, C, D	t_{PVD}			100	ns
Propagation Delay SYSCLK to SMSYNC High	t_{PSS}			75	ns
Propagation Delay SYSCLK or RCLK to $\overline{SLIP}$ Low	t_{PS}			100	ns
Propagation Delay SYSCLK to SIGFRZ Low/High	t_{PSF}			75	ns
$\overline{ALN}$, $\overline{SIGH}$ Setup to SFSYNC Rising	t_{SR}	500			ns

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2 TCLK = RCLK = 1.544 MHz
3 Outputs Open
4 All outputs except SLIP, which is open collector.
5 All outputs.
6 Applies to SLIP when tristated.

Figure 9: Receive A.C. Timing Diagram

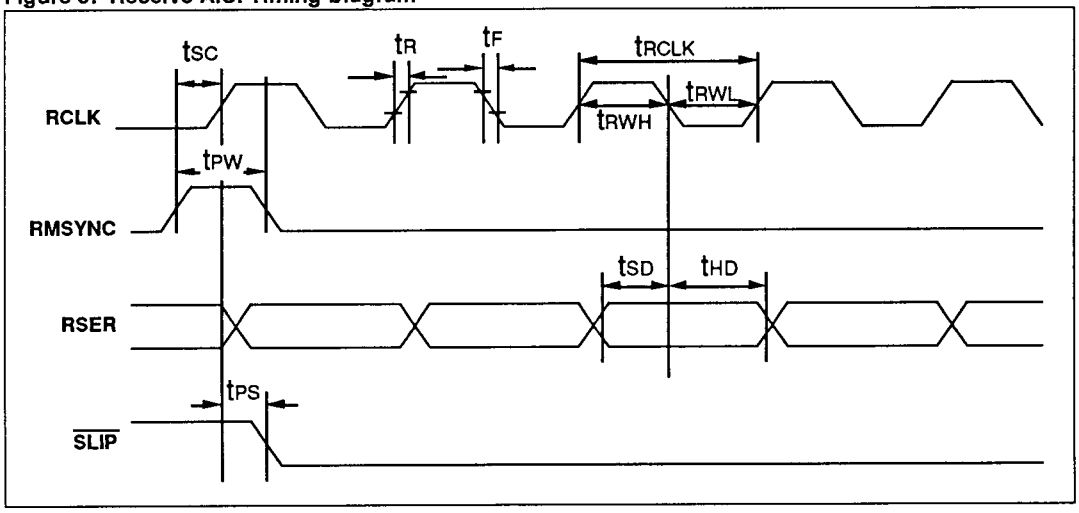


Figure 10: System A.C. Timing Diagram