IS27LV020

262,144 x 8 HIGH-SPEED, LOW VOLTAGE CMOS EPROM

ADVANCE INFORMATION
JULY 1996

FEATURES

- Fast read access time: 90 ns
- Industrial and commercial temperature ranges available
- 5V ±10% or 2.7V to 3.6V power supply tolerance
- JEDEC-approved pinout
- Standard 32-pin PLCC and TSOP packages

DESCRIPTION

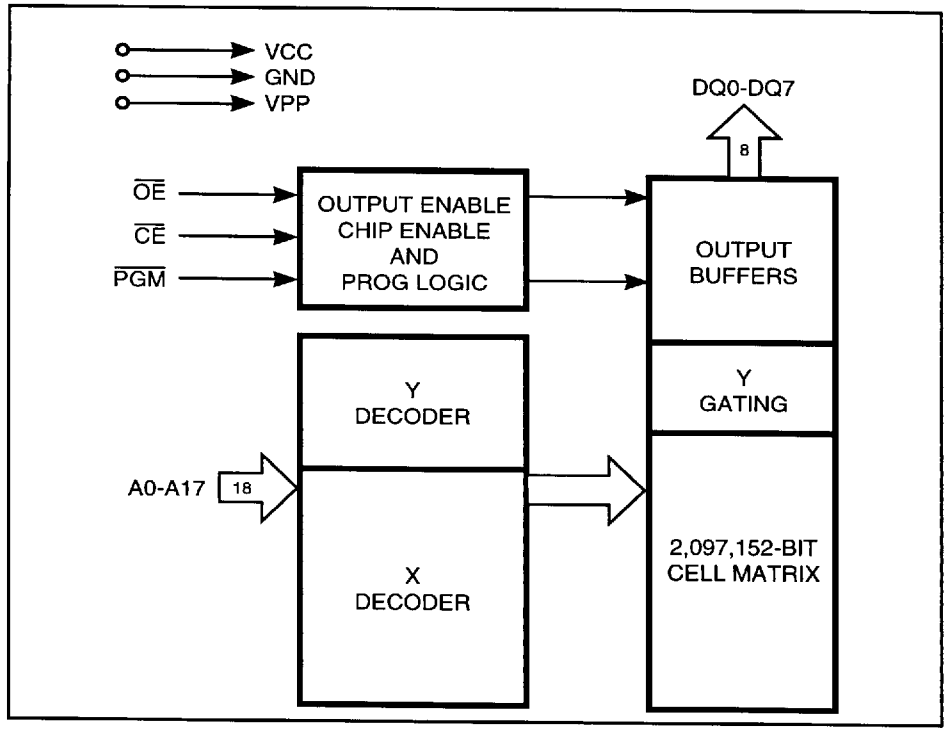
The *ISSI* IS27LV020 is a high-speed, low voltage 2 megabit (256K-word by 8-bit) Ultraviolet Erasable CMOS Programmable Read-Only Memory. This superior random access capability and low voltage operation results from a focused high-speed design.

The device is ideal for use with battery powered applications. Designers may take full advantage of high-speed digital signal processors and microprocessors at battery voltages by allowing code to be executed at full speed directly out of EPROM.

The IS27LV020 uses *ISSI*'s write programming algorithm which allows the entire chip to be programmed in typically less than 30 seconds.

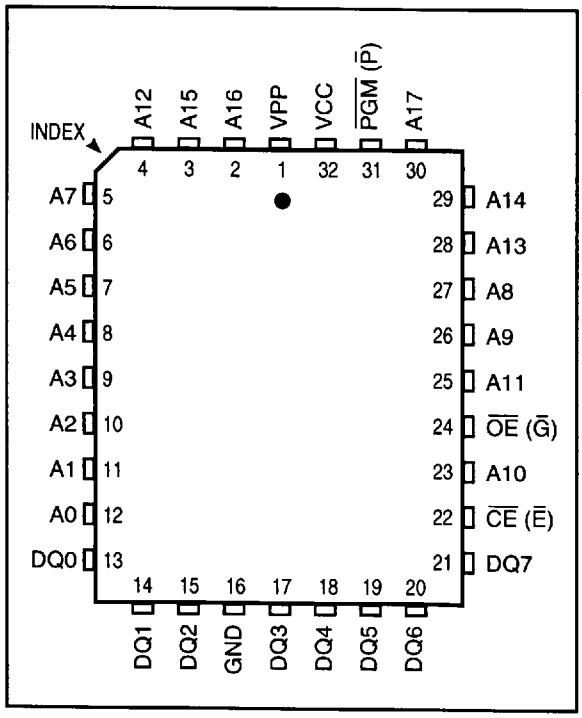
This product is available in One-Time Programmable (OTP) PLCC and TSOP packages over commercial and industrial temperature ranges.

FUNCTIONAL BLOCK DIAGRAM

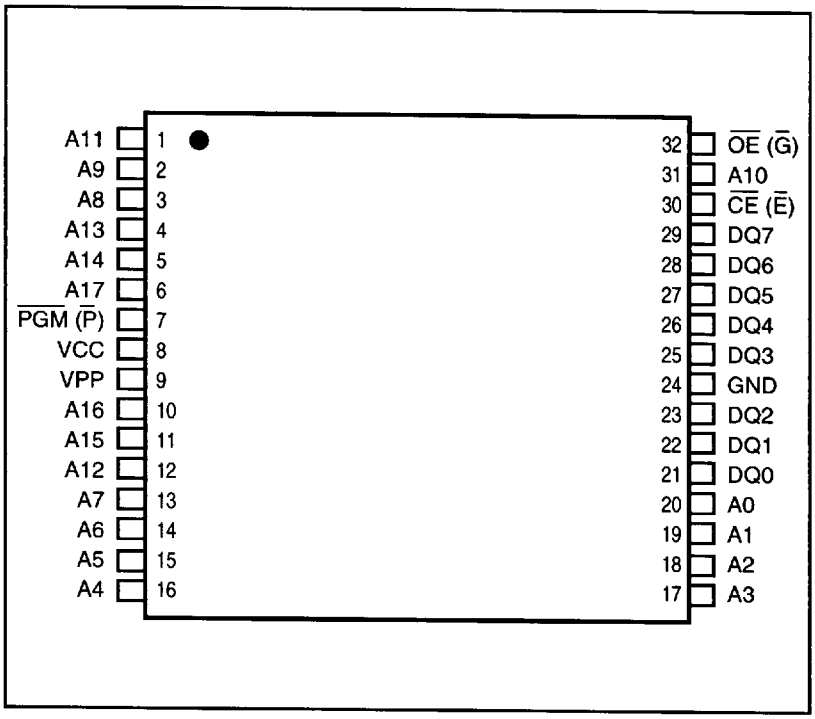


PIN CONFIGURATIONS\

32-Pin PLCC



32-Pin TSOP



PIN DESCRIPTIONS

A0-A17	Address Inputs
CE (E)	Chip Enable Input
DQ0-DQ7	Data Inputs/Outputs
OE (G)	Output Enable Input
PGM (P)	Program Enable Input
Vcc	Power Supply Voltage
VPP	Program Supply Voltage
GND	Ground

FUNCTIONAL DESCRIPTION

Erasing the IS27LV020

In order to clear all locations of their programmed contents, it is necessary to expose the IS27LV020 to an ultraviolet light source. A dosage of 30W - sec/cm^2 is required to completely erase the IS27LV020. This dosage can be obtained by exposure to an ultraviolet lamp-wavelength of 2537 Angstroms (Å)—with intensity of 12,000 µW/cm^2 for 30 to 40 minutes. The IS27LV020 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the IS27LV020, and similar devices, will erase with light sources having wavelengths shorter than 4000Å. The exposure to fluorescent light and sunlight will eventually erase the IS27LV020 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the IS27LV020

Upon delivery, or after each erasure, the IS27LV020 has 2,097,152 bits in the "ONE", or HIGH state. "ZEROs" are loaded into the IS27LV020 through the procedure of programming.

The programming mode is entered when 12.75 ± 0.25V is applied to the V_{PP} pin, V_{CC} = 6.25V, $\overline{CE}$ and $\overline{PGM}$ is at V_{IL}, and $\overline{OE}$ is at V_{IH}. For programming, the data to be programmed is applied eight bits in parallel to the data output pins.

The write programming algorithm reduces programming time by using 100 µs programming pulses followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the EPROM.

The write programming algorithm programs and verifies at V_{CC} = 6.25V and V_{PP} = 12.75V. After the final address is completed, all byte are compared to the original data with V_{CC} = 5.25V.

Program Inhibit

Programming of multiple IS27LV020s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel IS27LV020 may be common. A TTL low-level program pulse applied to an IS27LV020 $\overline{CE}$ input with V_{PP} = 12.75 ± 0.25V, $\overline{PGM}$ LOW and $\overline{OE}$ HIGH will program that IS27LV020. A high-level $\overline{CE}$ input inhibits the other IS27LV020 from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH}, and V_{PP} between 12.5V and 13.0V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the IS27LV020.

To activate this mode, the programming equipment must force 12.0 ± 0.5V on address line A9 of the IS27LV020. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code, and byte 1 (A0 = V_{IH}), the device identifier code. For the IS27LV020, these two identifier bytes are given in the Mode Select table. All identifiers manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The IS27LV020 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Output Enable ($\overline{OE}$) is the output control and should be used to get data to the output pins, independent of device selection. Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$ assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The IS27LV020 has a standby mode which reduces the maximum V_{CC} active current. It is placed in standby mode when $\overline{CE}$ is at V_{IH}. The amount of current drawn in standby mode depends on the frequency and the number of address pins switching. The IS27LV020 is specified with 50% of the address lines toggling at 10 MHz. A reduction of the frequency or quantity of address lines toggling will

significantly reduce the actual standby current.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation, and
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device at a minimum, a 0.1 µF ceramic capacitor (high-frequency, low inherent inductance) should be used on each device between Vcc and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between Vcc and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

TRUTH TABLE[1,2]

Mode		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A0	A9	VPP	Outputs
Read		VIL	VIL	X	X	X	VCC	DOUT
Output Disable		VIL	VIH	X	X	X	VCC	Hi-Z
Standby		VIH	X	X	X	X	VCC	Hi-Z
Program		VIL	VIH	VIL	X	X	VPP	DIN
Program Verify		VIL	VIL	VIH	X	X	VPP	DOUT
Program Inhibit		VIH	X	X	X	X	VPP	Hi-Z
Auto Select[3]	Manufacturer Code	VIL	VIL	X	VIL	VH	VCC	D5H
	Device Code	VIL	VIL	X	VIH	VH	VCC	97H

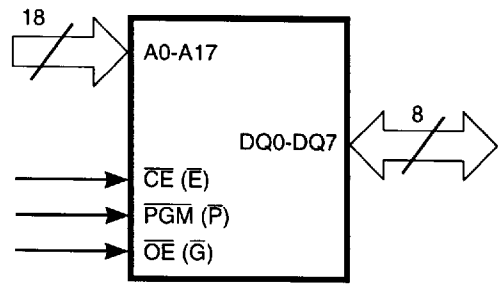
Notes:
1. VH = 12.0V ± 0.5V.
2. X = Either VIH or VIL.
3. A1-A8 = A10-A17 = VIL.
4. See DC Programming Characteristics for VPP voltage during programming.

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	2.7V to 3.6V or 5V ± 10%
Industrial[1]	–40°C to +85°C	2.7V to 3.6V or 5V ± 10%

Note:
1. Operating ranges define those limits between which the functionally of the device is guaranteed.

LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND		
	All pins except A9 and V_{PP}	−0.6 to V_{CC} + 0.5[2]	V
	V_{PP}	V_{CC} − 0.3 to 13.5[2,3]	V
	A9	−0.6 to 13.5[2,3]	V
	V_{CC}	−0.6 to 7.0[2]	V
T_A	Ambient Temperature with Power Applied	−65 to +125	°C
T_{STG}	Storage Temperature (OTP)	−65 to +125	°C
T_{STG}	Storage Temperature (All others)	−65 to +150	°C

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Minimum DC input voltage is −0.5V. During transitions, inputs may undershoot to −2.0V for periods less than 10 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2.0V for periods less than 10 ns.
3. Maximum DC voltage on A9 or V_{PP} may overshoot to +13.5V for periods less than 10 ns.

DC ELECTRICAL CHARACTERISTICS[1,2,3] (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5V, I_{OH} = −400 µA	2.4	—	V
		V_{CC} = 2.7V, I_{OH} = −2.0 mA	2.4	—	
		V_{CC} = 2.7V, I_{OH} = −100 mA	V_{CC} − 0.2	—	
		V_{CC} = 2.7V, I_{OH} = −20 µA	V_{CC} − 0.1	—	
V_{OL}	Output LOW Voltage	V_{CC} = 4.5V, I_{OL} = 2.1 mA	—	0.45	V
		V_{CC} = 2.7V, I_{OL} = 2.0 mA	—	0.40	
		V_{CC} = 2.7V, I_{OL} = 100 mA	—	0.20	
		V_{CC} = 2.7V, I_{OL} = 20 µA	—	0.10	
V_{IH}	Input HIGH Voltage[4]	V_{CC} = 4.5V	2.0	V_{CC} + 0.5	V
		V_{CC} = 3.0V to 3.6V	2.0	V_{CC} + 0.5	
		V_{CC} = 2.7V to 3.6V	0.7 x V_{CC}	V_{CC} + 0.5	
V_{IL}	Input LOW Voltage[4]	V_{CC} = 4.5V	−0.5	0.8	V
		V_{CC} = 3.0V to 3.6V	2.0	V_{CC} + 0.5	
		V_{CC} = 2.7V to 3.6V	0.7 x V_{CC}	V_{CC} + 0.5	
I_{LI}	Input Load Current	V_{IN} = 0V to +V_{CC}	—	5.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to +V_{CC}	—	5	µA

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. Never try to force V_{PP} LOW to 1V below V_{CC}. Manufacturer suggests to tie V_{PP} and V_{CC} together during the READ operation.
2. **Caution:** the IS27LV020 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
3. Minimum DC input voltage is −0.5V. During transitions, the inputs may undershoot to −2.0V for periods less than 10 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2.0V for periods less than 10 ns.
4. Tested under static DC conditions.

POWER SUPPLY CHARACTERISTICS[1,2,5] (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{CC1}	Vcc Operating Supply Current[3]	V_{CC} = 5.5V, $\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, f = 5 MHz	—	25	mA
		V_{CC} = 3.3V, $\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, f = 5 MHz	—	8	mA
I_{PP1}	V_{PP} Current During Read[4]	V_{CC} = Max., $\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}	—	10	µA
I_{CCSB0}	Vcc CMOS Standby Current	CE ≥ V_{CC} ± 0.3V, V_{CC} = 5.0V	—	100	µA
		$\overline{CE}$ ≥ V_{CC} ± 0.3V, V_{CC} = 3.0V	—	20	µA
I_{CCSB1}	Vcc TTL Standby Current	CE ≥ V_{IH}, V_{CC} = 5.0V	—	1.0	mA
		$\overline{CE}$ ≥ V_{IH}, V_{CC} = 3.0V	—	100	µA

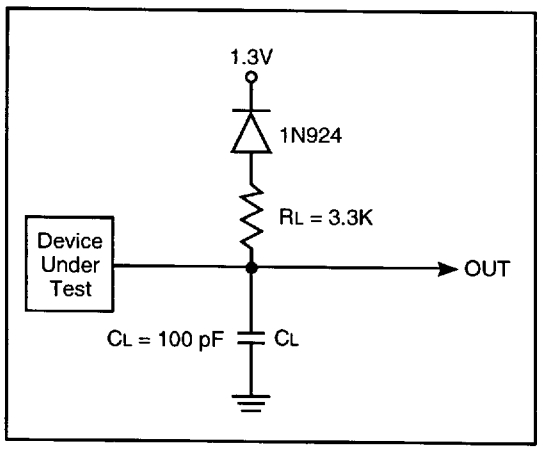
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. Never try to force V_{PP} LOW to 1V below V_{CC}. Manufacturer suggests to tie V_{PP} and Vcc together during the READ operation.
2. **Caution:** the IS27LV020 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
3. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
4. Maximum active power usage is the sum of I_{CC} and I_{PP}.
5. Minimum DC input voltage is –0.5V. During transitions, the inputs may undershoot to –2.0V for periods less than 10 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2.0V for periods less than 10 ns.

CAPACITANCE[1,2,3]

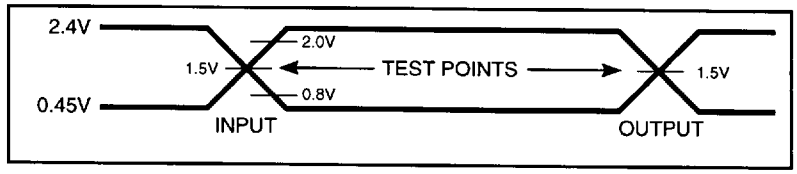
Symbol	Parameter	Conditions	Typ.	Max.	Unit
C_{IN}	Address Input Capacitance	V_{IN} = 0V	4	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

Notes:
1. Typical values are for nominal supply voltage.
2. This parameter is only sampled, but not 100% tested.
3. Test conditions: T_A = 25°C, f = 1 MHz.

SWITCHING TEST CIRCUIT



SWITCHING TEST WAVEFORM



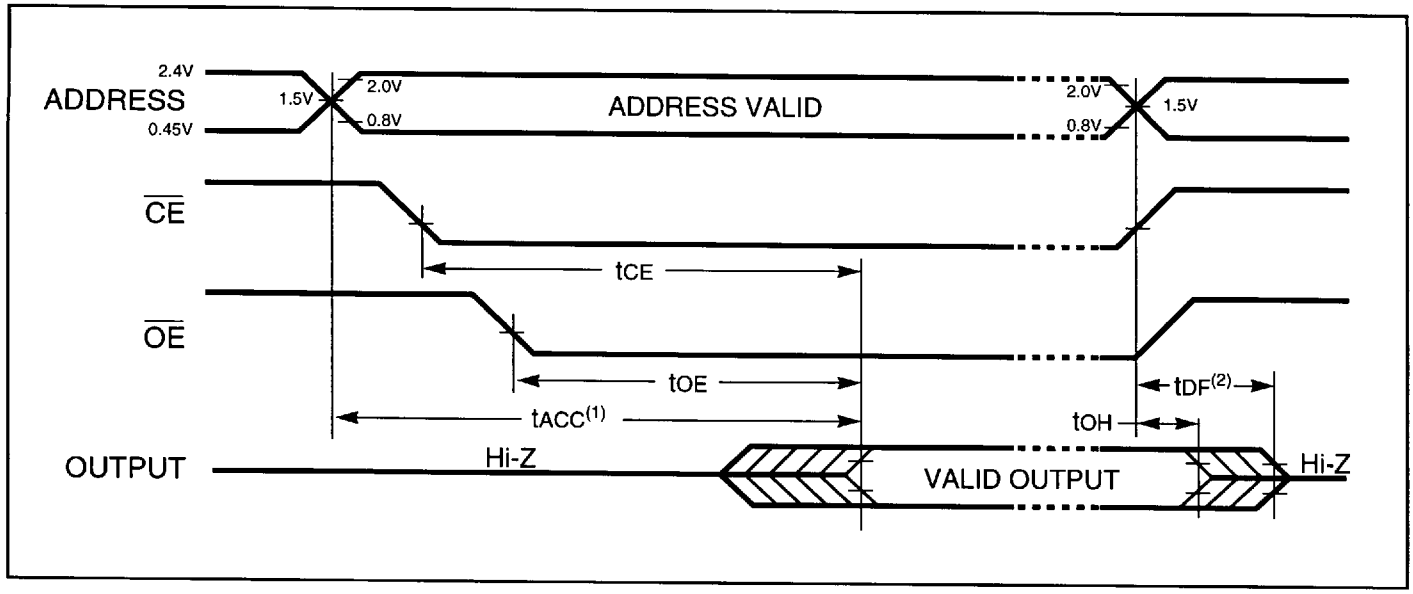
Notes:
AC Testing:
1. Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
2. Input pulse rise and fall skew rate ≥ 1.5V/ns.

SWITCHING CHARACTERISTICS[1,3,4] (Over Operating Range)

JEDEC Symbol	Std. Symbol	Parameter	Test Conditions	-90 Min.	-90 Max.	-100 Min.	-100 Max.	-120 Min.	-120 Max.	Unit
t_{AVQA}	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$	—	90	—	100	—	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	—	90	—	100	—	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	—	35	—	45	—	45	ns
t_{EHQZ}, t_{GHQZ}	t_{DF}[2]	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		0	20	0	20	0	25	ns
t_{AVOX}	t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ whichever occured first		0	—	0	—	0	—	ns

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled, not 100% tested.
3. **Caution:** The IS27LV020 must not be removed from (or inserted into) a socket or board when V_{PP} or V_{CC} applied.
4. Output Load: 1 TTL gate and C = C_L.
   Input Rise and Fall times: 20 ns.
   Input Pulse Levels: 0.45 to 2.4V.
   Timing Measurement Reference Level: 0.8V nd 2.0V inputs and outputs.

SWITCHING WAVEFORMS



Notes:
1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

DC PROGRAMMING CHARACTERISTICS[1,2,3,4] (T_A = +25°C ± 5°C)

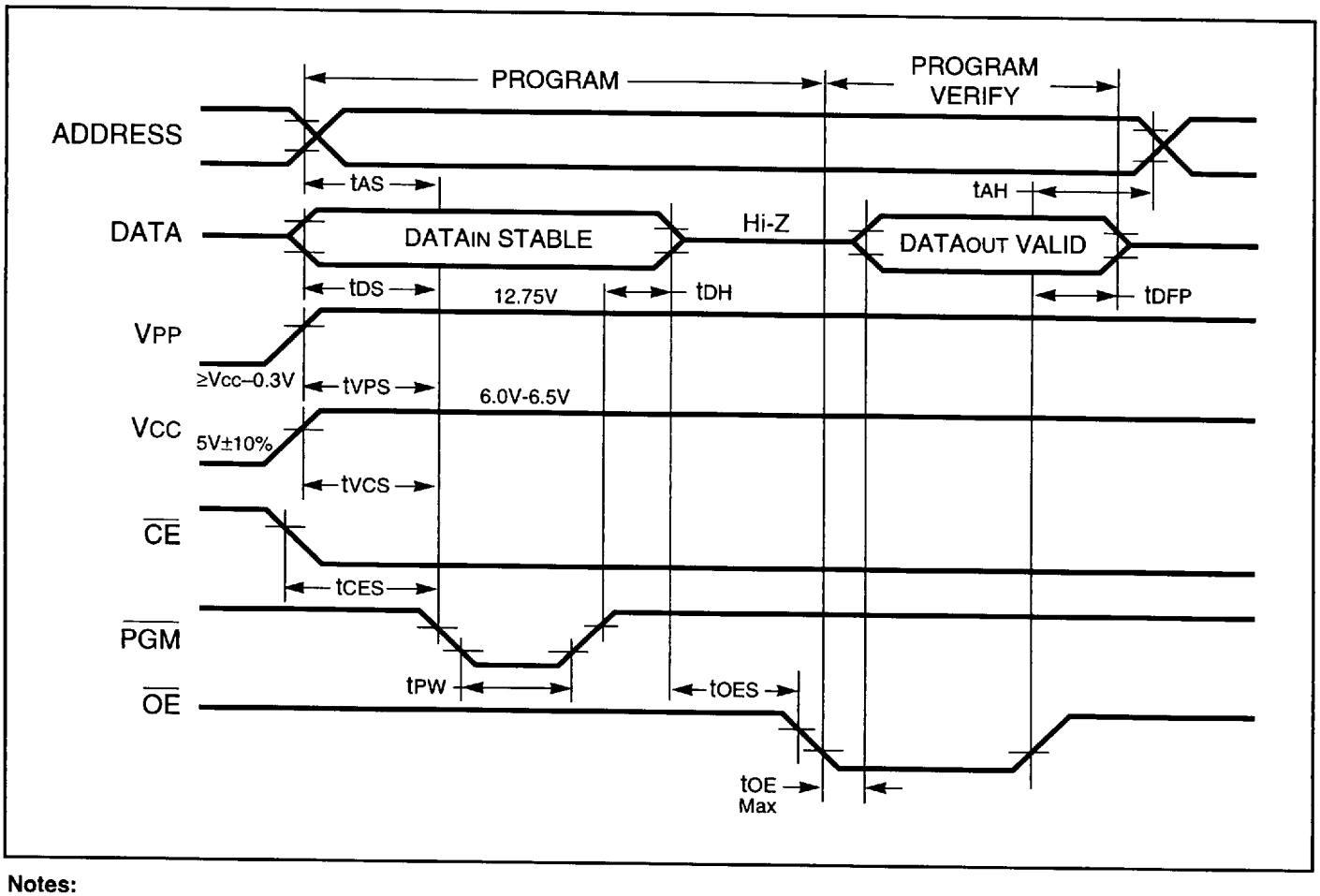
Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage During Verify	I_{OH} = –400 µA	2.4	—	V
V_{OL}	Output LOW Voltage During Verify	I_{OL} = 2.1 mA	—	0.45	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage (All Inputs)		–0.5	0.8	V
V_H	A9 Auto Select Voltage		11.5	12.5	V
I_{LI}	Input Current (All Inputs)	V_{IN} = V_{IL} or V_{IH}	—	1.0	µA
I_{CC}	Vcc Supply Current		—	50	mA
I_{PP}	V_{PP} Supply Current	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	—	30	mA
V_{CC}	Supply Voltage		6.0	6.5	V
V_{PP}	Programming Voltage		12.5	13.0	V

SWITCH PROGRAMMING CHARACTERISTICS[1,2,3,4] (T_A = +25°C ± 5°C)

JEDEC Symbol	Std. Symbol	Parameter	Min.	Max.	Unit
t_{AVEL}	t_{AS}	Address Setup Time	2	—	µs
t_{DZGL}	t_{OES}	$\overline{OE}$ Setup Time	2	—	µs
t_{DVEL}	t_{DS}	Data Setup Time	2	—	µs
t_{GHAX}	t_{AH}	Address Hold Time	0	—	µs
t_{EHDX}	t_{DH}	Data Hold Time	2	—	µs
t_{GHQZ}	t_{DFP}	$\overline{OE}$ HIGH to Output Float Delay	0	130	ns
t_{VPS}	t_{VPS}	V_{PP} Setup Time	2	—	µs
t_{ELEH1}	t_{PW}	$\overline{PGM}$ Program Pulse Width	95	105	µs
t_{VCS}	t_{VCS}	Vcc Setup Time	2	—	µs
t_{ELPL}	t_{CES}	$\overline{CE}$ Setup Time	2	—	µs
t_{GLQV}	t_{OE}	Data Valid from $\overline{OE}$	—	150	ns

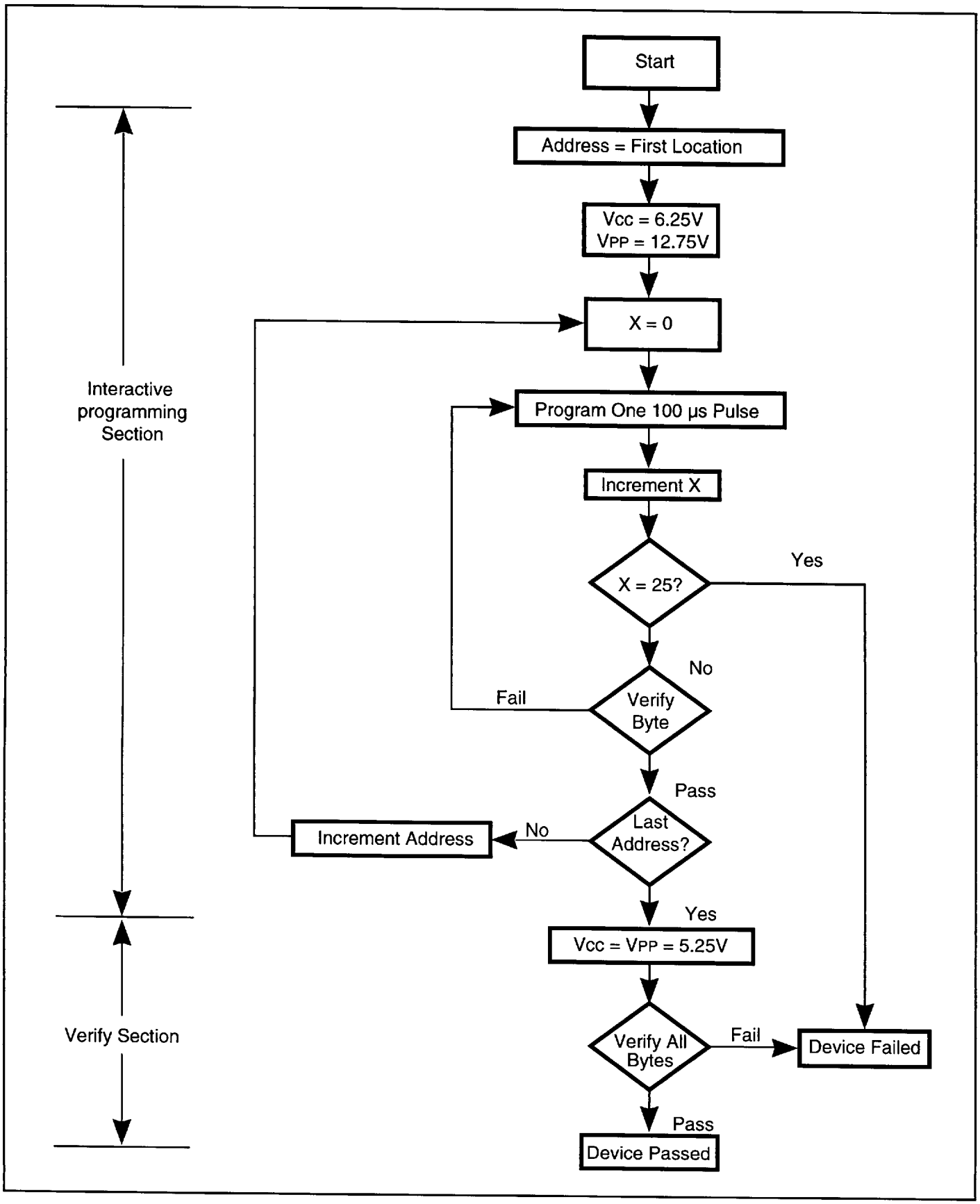
Notes:
1. Vcc must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} must be ≥ Vcc during the entire programming and verifying procedure.
3. When programming IS27LV020, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.
4. Programming characteristics are sampled but not 100% tested at worst-case conditions.

PROGRAMMING ALGORITHM WAVEFORM[1,2]



Notes:
1. The timing reference level is 1.5V for inputs and outputs.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

PROGRAMMING FLOW CHART



ORDERING INFORMATION
Commercial Range: 0°C to +70°C

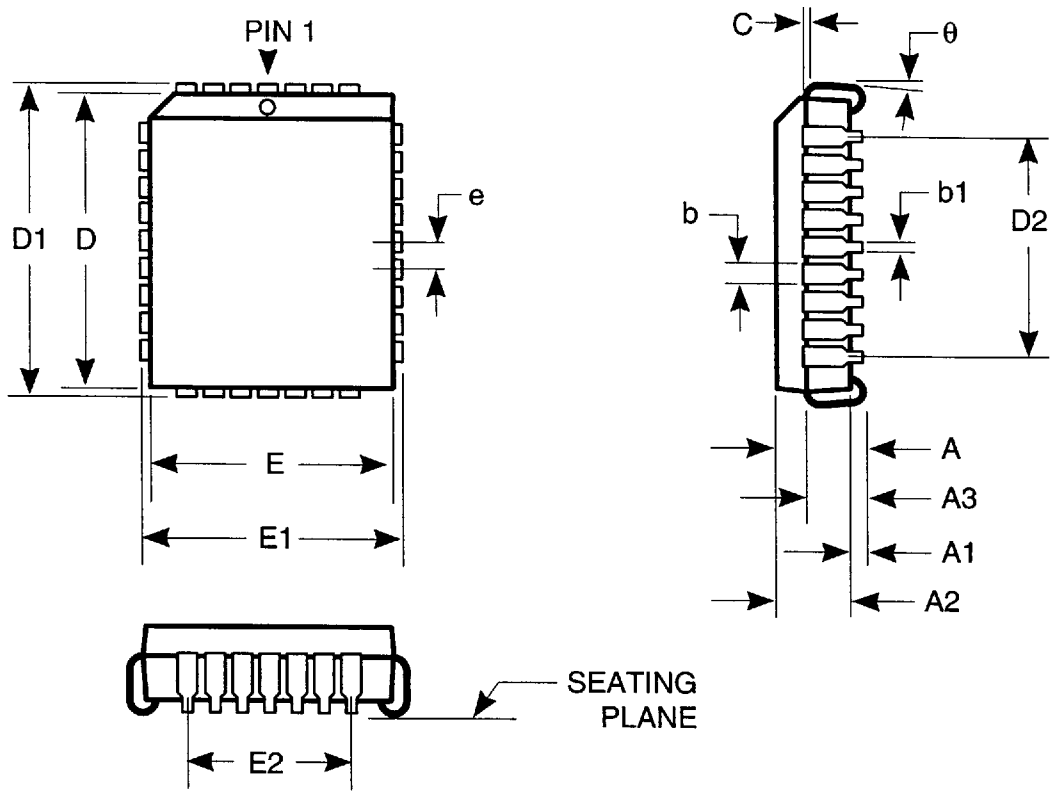
Speed (ns)	Order Part Number	Package
90	IS27LV020-90PL	PLCC – Plastic Leaded Chip Carrier
90	IS27LV020-90T	TSOP
100	IS27LV020-10PL	PLCC – Plastic Leaded Chip Carrier
100	IS27LV020-10T	TSOP
120	IS27LV020-12PL	PLCC – Plastic Leaded Chip Carrier
120	IS27LV020-12T	TSOP

ORDERING INFORMATION
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part Number	Package
90	IS27LV020-90PLI	PLCC – Plastic Leaded Chip Carrier
90	IS27LV020-90TI	TSOP
100	IS27LV020-10PLI	PLCC – Plastic Leaded Chip Carrier
100	IS27LV020-10TI	TSOP
120	IS27LV020-12PLI	PLCC – Plastic Leaded Chip Carrier
120	IS27LV020-12TI	TSOP

Integrated Silicon Solution, Inc.
680 Almanor Avenue
Sunnyvale, CA 94086
Tel: (408) 733-4774
Fax: (408) 245-4774
Tool Free: 1-800-379-4774
http://www.issiusa.com

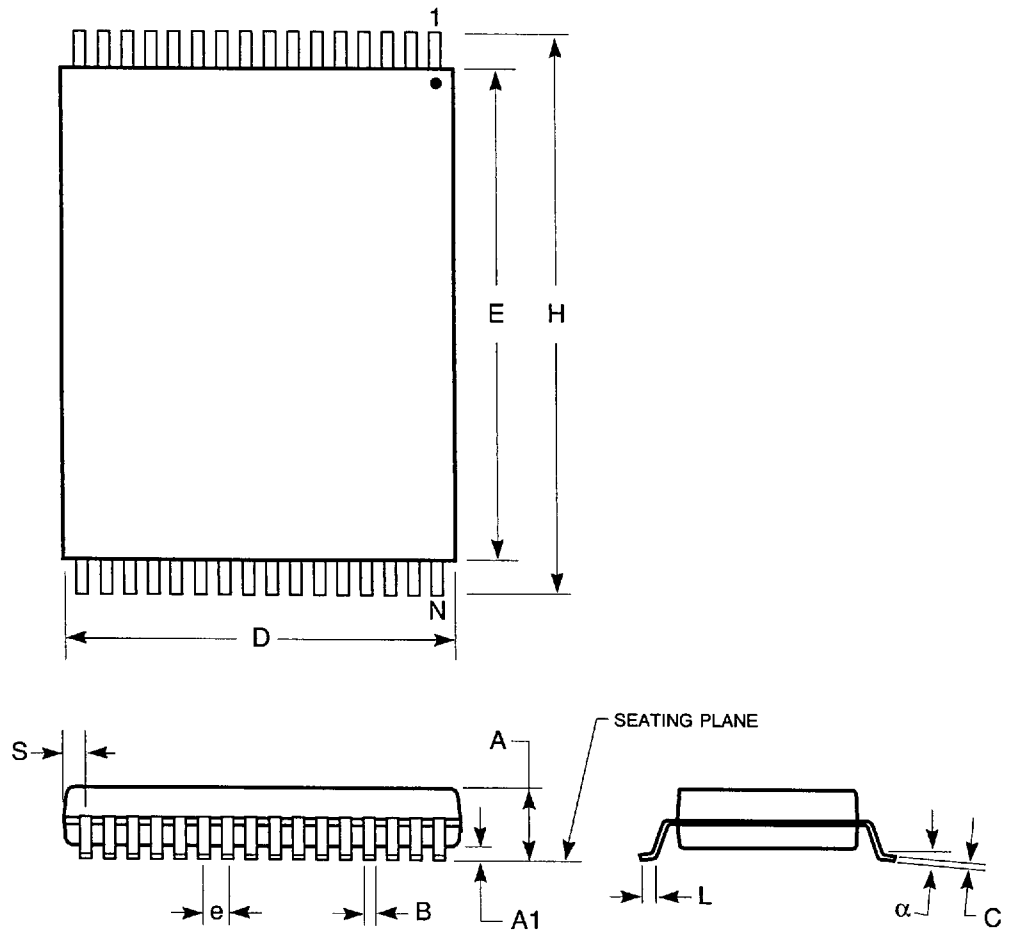
PLCC (Plastic Leaded Chip Carrier)
Package Code: PL



Plasstic Leaded Chip Carrier (PL)				
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
Ref. Std.				
No. Leads		32		
A	3.33	3.56	0.131	0.140
A1	0.50	—	0.020	—
A2	2.67	2.93	0.105	0.115
A3	1.91	2.41	0.075	0.095
b	0.66	0.81	0.026	0.032
b1	0.33	0.54	0.013	0.021
C	0.20	0.35	0.008	0.014
D	13.89	14.05	0.547	0.553
D1	14.86	15.10	0.585	0.595
D2	—	10.16	—	0.400
E	11.35	11.51	0.447	0.453
E1	12.32	12.57	0.485	0.495
E2	—	7.62	—	0.300
e	1.27 BSC		0.050 BSC	
θ	0°	10°	0°	10°

Notes:
1. Controlling dimension: millimeters/inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.
5. ND and NE represent the number of leads in D and E directions, respectively.
6. D1 and E1 should be measured from the bottom of the package.

Plastic TSOP - 32 pins
Package Code: T (Type I)



Plastic TSOP (T—Type I)				
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
Ref. Std.				
No. Leads		32		
A	—	1.20	—	0.047
A1	0.05	0.25	0.002	0.010
B	0.17	0.23	0.007	0.009
C	0.12	0.17	0.006	0.014
D	7.90	8.10	0.308	0.316
E	18.30	18.50	0.714	0.722
H	19.80	20.20	0.772	0.788
e	0.50 BSC		0.020 BSC	
L	0.40	0.60	0.016	0.024
α	0°	8°	0°	8°

Notes:
1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.