HYUNDAI

HY514460B Series

256K x 16-bit CMOS DRAM with 2 CAS & WPB

PRELIMINARY

DESCRIPTION

The HY514460B is the new generation and fast dynamic RAM organized 262,144 x 16-bit configuration employing advanced submicron CMOS process technology and advanced circuit design technique to achieve fast access time. Independant read and write of upper and lower byte is controlled by 2 separate $\overline{CAS}$ inputs. It gives Write-Per-Bit function useful for graphics applications.
Refresh control is provided through $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, hidden refresh and self refresh modes. The HY514460B conforms to JEDEC pinpoint standards and is available in industry standard 400mil 40pin SOJ and 40/44pin TSOP-II and reverse TSOP-II packages.

FEATURES

- **Low power dissipation**
  Max. battery back-up 1.1mW (L-part)
  Max. CMOS standby 0.825mW (L-part)
  5.5mW
  Max. TTL standby 5.5mW
  Max. Self refresh 1.1mW (SL-part)
  Max. operating

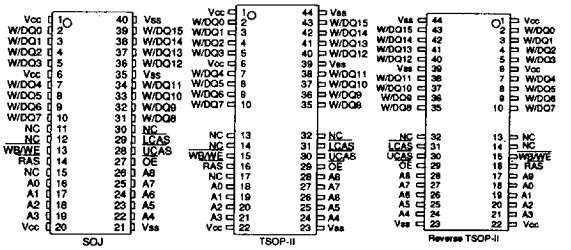
Speed	Power
60	715.0mW
70	660.0mW
80	605.0mW

- **Single power supply of 5V±10%**
- **TTL compatible inputs and outputs**
- **Fast access time**

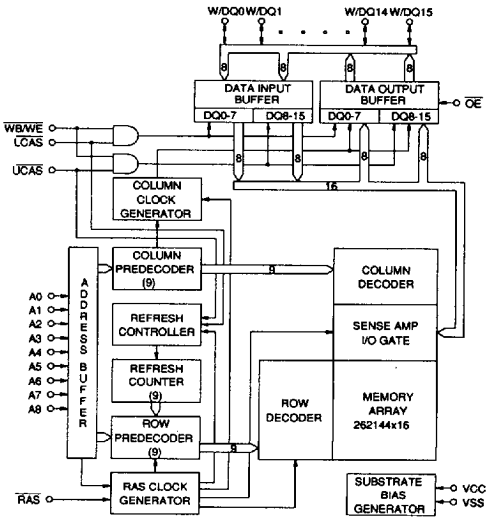
Speed	tRAC	tCAC	tPC
60	60ns	15ns	40ns
70	70ns	20ns	40ns
80	80ns	20ns	50ns

- **Fast page mode operation**
- **2 $\overline{CAS}$ inputs for upper and lower byte control**
- **Write-Per-Bit function**
- **Read-Modify-Write capability**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden refresh and Self refresh**
- **512 refresh cycles / 128ms (L-part)**
  512 refresh cycles / 8ms

PIN CONNECTION



BLOCK DIAGRAM



PIN DESCRIPTION

$\overline{RAS}$	Row Address Strobe
$\overline{LCAS}$, $\overline{UCAS}$	Column Address Strobe
$\overline{WB/WE}$	Write-Per-Bit/Write Enable
$\overline{OE}$	Output Enable
A0-A8	Address Input
W/DQ0-15	Write Mask/Data IO
Vcc	Power (+5V)
Vss	Ground

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	–1.0 to 7.0	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	–1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature• Time	260• 10	°C• sec

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	V_{CC}+ 1.0	V
V_{IL}	Input Low Voltage	–1.0	-	0.8	V

NOTE : All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(T_A= 0°C to 70°C, V_{CC}= 5V± 10%, V_{SS}= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
I_{LI}	Input Leakage Current (Any Input Pins)	$V_{SS} \le V_{IN} \le$ 6.5V, All other pins not under test= V_{SS}		-10	10	µA	
I_{LO}	Output Leakage Current (High Impedance State)	$V_{SS} \le V_{OUT} \le$ 5.5V, $\overline{RAS}$ & $\overline{CAS}$ at V_{IH}		-10	10	µA	
I_{CC1}	V_{CC} Supply Current, Operating	t_{RC}= t_{RC} (min.)	60 70 80	- - -	130 120 110	mA	1,2,3
I_{CC2}	V_{CC} Supply Current, TTL Standby	$\overline{RAS}$ & $\overline{CAS}$ at V_{IH}, other inputs≥ V_{SS}		-	1	mA	
I_{CC3}	V_{CC} Supply Current, $\overline{RAS}$-only refresh	t_{RC}= t_{RC} (min.)	60 70 80	- - -	130 120 110	mA	1,2,3
I_{CC4}	V_{CC} Supply Current, Fast Page mode	t_{PC}= t_{PC} (min.)	60 70 80	- - -	80 70 60	mA	1,2,3
I_{CC5}	V_{CC} Supply Current, CMOS Standby	$\overline{RAS}$ & $\overline{CAS}$ ≥ V_{CC}–0.2V	 L-part	- -	1 0.15	mA	 5
I_{CC6}	V_{CC} Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_{RC}= t_{RC} (min.)	60 70 80	- - -	130 120 110	mA	1,2,3
I_{CC7}	V_{CC} Supply Current, Battery Back Up (L-part only)	t_{RC}= 250µs, $t_{RAS} \le$ 1µs $\overline{CAS}$= CBR cycling or 0.2V $\overline{OE}$ & $\overline{WB/WE}$= V_{CC}–0.2V, A0-A8= V_{CC}–0.2V or 0.2V W/DQ0-15= 0.2V, V_{CC}–0.2V or open		-	200	µA	1,4,5
I_{CC8}	V_{CC} Supply Current, Self refresh (SL-part only)	$\overline{RAS}$ & $\overline{CAS} \le$ 0.2V other pins same as I_{CC7}		-	200	µA	6
V_{OL}	Output Low Voltage	I_{OL}= 4.2mA		-	0.4	V	
V_{OH}	Output High Voltage	I_{OH}= –5mA		2.4	-	V	

NOTE :

1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} and I_{CC7} depend on cycle rate.
2. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading. Specified values are obtained with the output open.
3. Icc is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$= V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CAS}$= V_{IH}.
4. Only t_{RAS}(max.)= 1µs is applied to refresh of battery backup but t_{RAS}(max.)= 10µs is applied to normal functional operation .
5. I_{CC5}(max.)= 0.15mA and I_{CC7} are applied to L-parts (HY514460BLJC, HY514460BLTC, HY514460BLRC HY514460BSLJC, HY514460BSLTC and HY514460BSLRC).
6. I_{CC8} is applied to SL-parts only (HY514460BSLJC, HY514460BSLTC and HY514460BSLRC).

AC CHARACTERISTICS

(TA= 0°C to 70°C, Vcc= 5V± 10%, Vss= 0V, unless otherwise noted.) NOTE : 1, 2, 3, 13

#	SYMBOL	PARAMETER	HY514460BJC/TC/RC/LJC/LTC/LRC/SLJC/SLTC/SLRC						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	155	-	170	-	200	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	40	-	50	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	80	-	80	-	100	-	ns	
5	tRAC	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from $\overline{CAS}$	-	15	-	20	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from Column Precharge	-	35	-	35	-	45	ns	4,15
9	tCLZ	$\overline{CAS}$ to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	15	0	15	0	15	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3
12	tRP	$\overline{RAS}$ Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100K	70	100K	80	100K	ns	
15	tRSH	$\overline{RAS}$ Hold Time	15	-	20	-	20	-	ns	
16	tCSH	$\overline{CAS}$ Hold Time	60	-	70	-	80	-	ns	
17	tCAS	$\overline{CAS}$ Pulse Width	15	10K	20	10K	20	10K	ns	
18	tRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay	15	45	20	50	20	60	ns	9
19	tRAD	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	10
20	tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	15
21	tCP	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	17
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	14
25	tCAH	Column Address Hold Time	15	-	15	-	15	-	ns	14
26	tAR	Column Address Hold Time from $\overline{RAS}$	50	-	55	-	60	-	ns	
27	tRAL	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	14
29	tRCH	Read Command Hold Time Referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	6,14
30	tRRH	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	15	-	15	-	15	-	ns	14
32	tWCR	Write Command Hold Time from $\overline{RAS}$	50	-	55	-	60	-	ns	
33	tWP	Write Command Pulse Width	10	-	10	-	10	-	ns	
34	tRWL	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	20	-	ns	
35	tCWL	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	20	-	ns	16
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	15	-	15	-	15	-	ns	7,
38	tDHR	Data-In Hold Time Referenced to $\overline{RAS}$	50	-	55	-	60	-	ns	
39	tREF	Refresh Period (512cycles)	-	8	-	8	-	8	ms	12
		L-part	-	128	-	128	-	128		11
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8,14

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HY514370BJC/TC/RC/LJC/LTC/LRC/SLJC/SLTC/SLRC						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45	-	50	-	50	-	ns	8,14
42	tRWD	$\overline{RAS}$ to $\overline{WE}$ Delay Time	85	-	95	-	105	-	ns	8,14
43	tAWD	Column Address to $\overline{WE}$ Delay Time	55	-	60	-	65	-	ns	8,14
44	tCSR	$\overline{CAS}$ Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
45	tCHR	$\overline{CAS}$ Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
46	tRPC	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	5	-	ns	
47	tCPT	$\overline{CAS}$ Precharge Time (CBR Counter Test)	30	-	35	-	40	-	ns	
48	tROH	$\overline{RAS}$ Hold Time Reference to $\overline{OE}$	0	-	0	-	0	-	ns	
49	tOEA	$\overline{OE}$ Access Time	-	15	-	20	-	20	ns	
50	tOED	$\overline{OE}$ to Data Delay	15	-	20	-	20	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from $\overline{OE}$	0	15	0	20	0	20	ns	5
52	tOEH	$\overline{OE}$ Command Hold Time	15	-	20	-	20	-	ns	15
53	tCPWD	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	55	-	65	-	75	-	ns	8
54	tRHCP	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	-	40	-	50	-	ns	
55	tWRP	$\overline{WE}$ to $\overline{RAS}$ Precharge Time (CBR Cycle)	5	-	5	-	5	-	ns	
56	tWPH	$\overline{WE}$ to $\overline{RAS}$ Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
57	tRASS	$\overline{RAS}$ Pulse Width (Self Refresh)	100	-	100	-	100	-	µs	
58	tRPS	$\overline{RAS}$ Precharge Time (Self Refresh)	110	-	130	-	150	-	ns	
59	tCHS	$\overline{CAS}$ Hold Time from $\overline{RAS}$ (Self Refresh)	-50	-	-50	-	-50	-	ns	
60	tWBS	Write-Per-Bit Set-Up Time	0	-	0	-	0	-	ns	
61	tWBH	Write-Per-Bit Hold Time	10	-	10	-	10	-	ns	
62	tWDS	Write-Per-Bit Selection Set-Up Time	0	-	0	-	0	-	ns	
63	tWDH	Write-Per-Bit Selection Hold Time	10	-	10	-	10	-	ns	

NOTE :

1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$-only refresh cycles are required.
2. If $\overline{RAS}$= Vss during power-up, the HY514460B could begin an active cycle. This condition results in higher current than necessary current which is demanded from the power supply during power-up. It is recommened that $\overline{RAS}$ and $\overline{CAS}$ track with Vcc during power-up or be held at a valid V_{IH} in order to minimize the power-up current.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min.) and V_{IL}(max.), and are assumed to be 5ns for all inputs.
4. Measured at V_{OH}= 2.4V and V_{OL}= 0.4V with a load equivalent to 2 TTL loads and 100pF.
5. t_{OFF}(max.) and t_{OEZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{LCAS}$ or $\overline{UCAS}$ leading edge in early write cycles and to $\overline{WB/WE}$ leading edge in Read-Modify-Write cycles.
8. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.), and $t_{CPWD} \geq t_{CPWD}$(min.), the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
9. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
10. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
11. t_{REF}(max.)= 128ms is applied to L-parts (HY514460BSLJC, HY514460BSLTC , HY514460BSLRC HY514460BLJC, HY514460BLTC and HY514460BLRC).
12. A burst of 512 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles must be executed within 8ms (128ms for L-part) after exiting self refresh.
13. When both $\overline{LCAS}$ and $\overline{UCAS}$ go low at the same time, all 16-bits data are written into the device. $\overline{LCAS}$ and $\overline{UCAS}$ must be transited simultaneously within a same read or write cycle.
14. These parameters are determined by the earlier falling edge of $\overline{LCAS}$ or $\overline{UCAS}$.
15. These parameters are determined by the later rising edge of $\overline{LCAS}$ or $\overline{UCAS}$.
16. t_{CWL} must be satisfied by both $\overline{LCAS}$ and $\overline{UCAS}$ for 16-bits access cycles.
17. t_{CP} and t_{CPT} are measured when both $\overline{LCAS}$ and $\overline{UCAS}$ are high state.

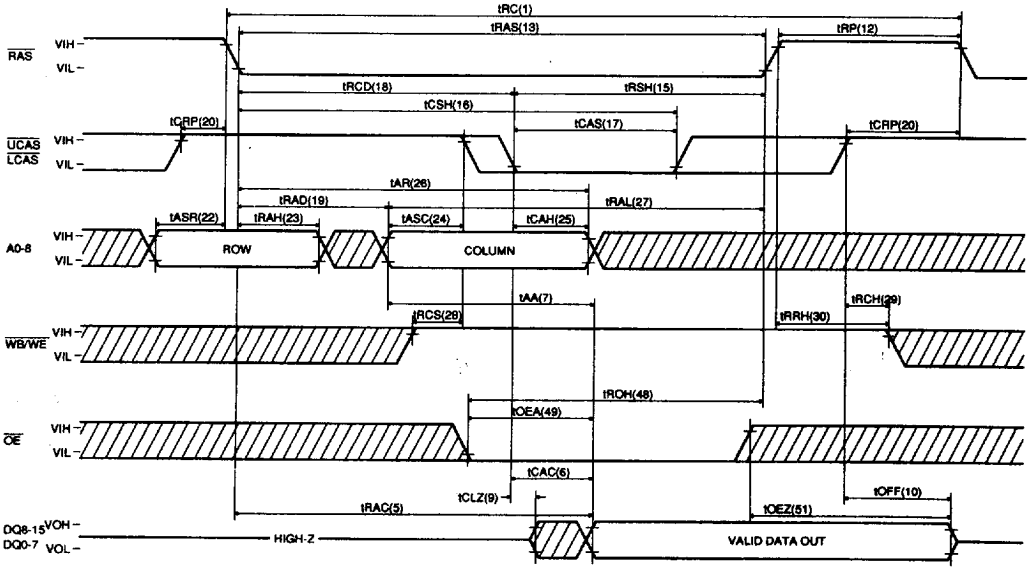
CAPACITANCE

(T_A= 25°C, V_{CC}= 5V± 10%, V_{SS}= 0V, f= 1MHz, unless otherwise noted.)

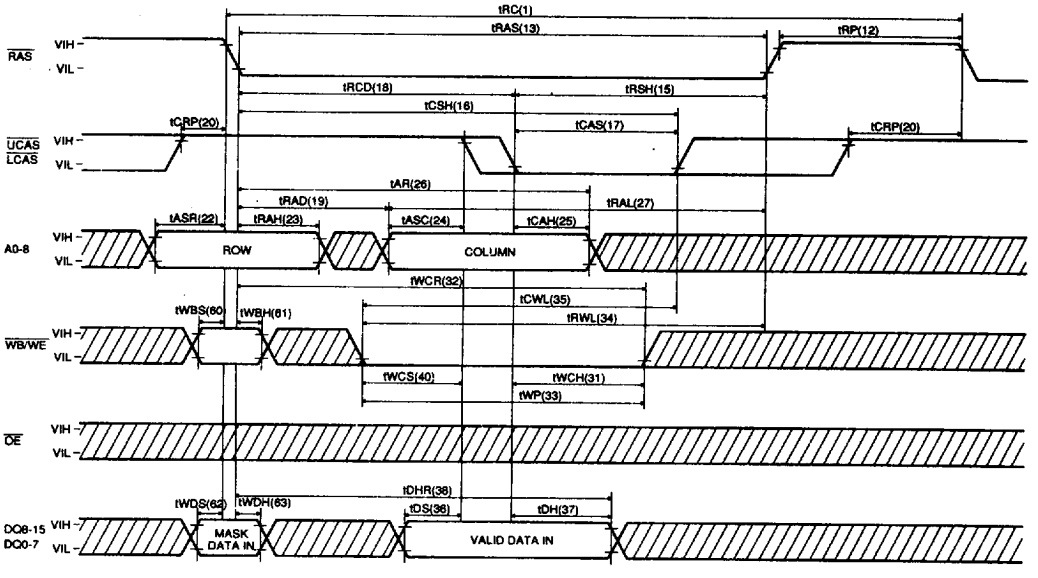
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A8)	-	5	pF
C_{IN2}	Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WB/WE}$, $\overline{OE}$)	-	7	pF
C_{DQ}	Data Input/Output Capacitance (DQ0-DQ15)	-	7	pF

TIMING DIAGRAM

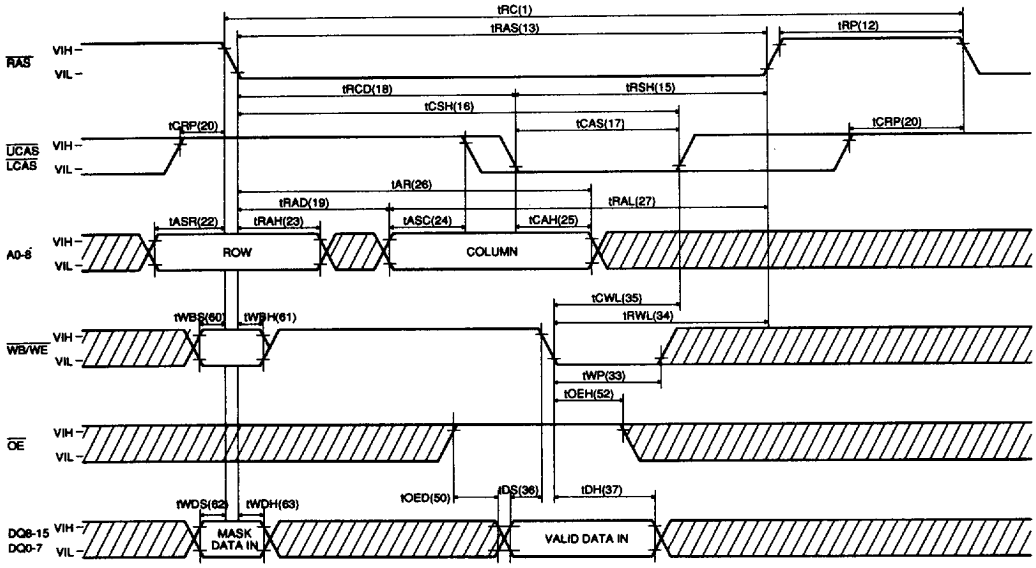
READ CYCLE



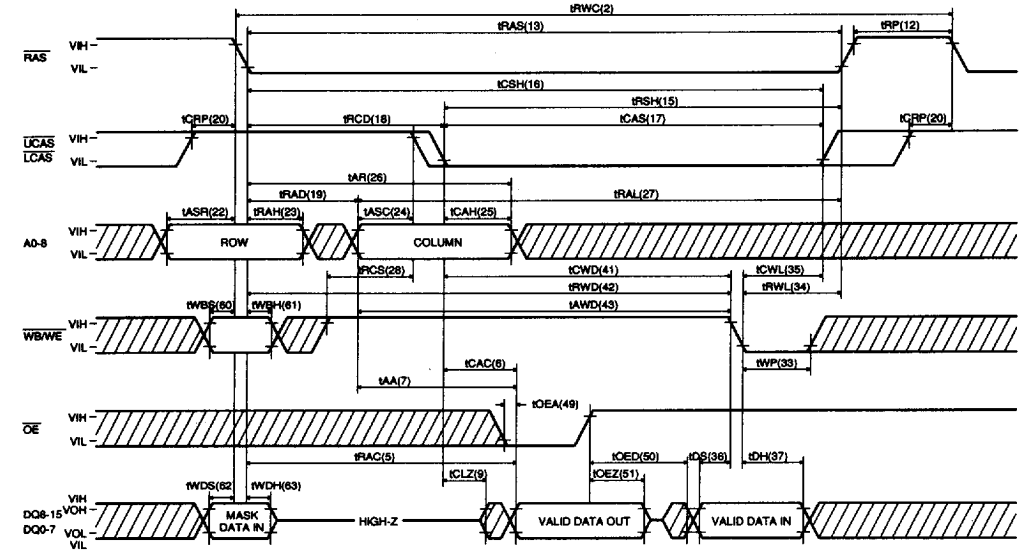
EARLY WRITE CYCLE



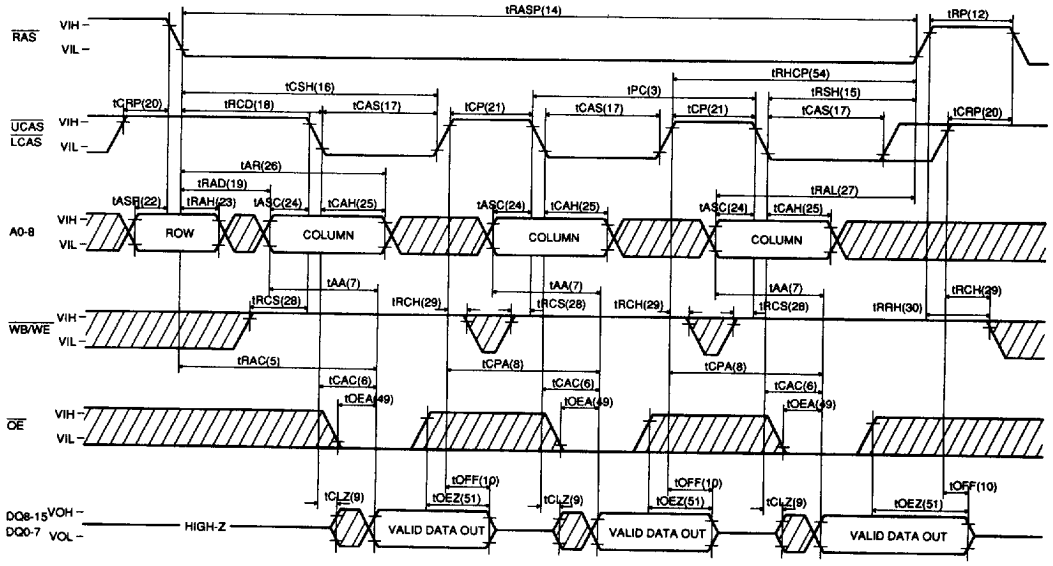
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



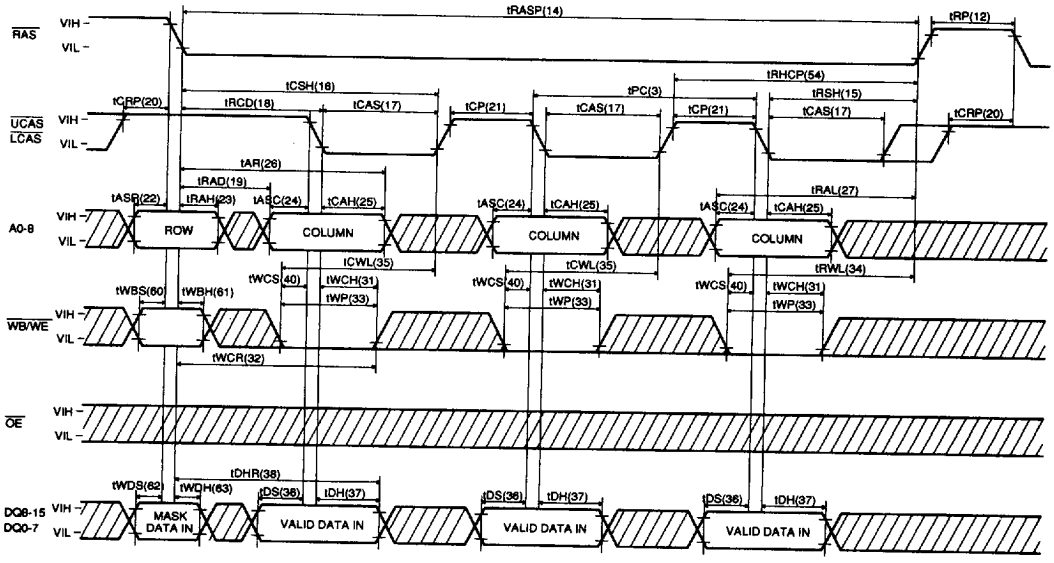
READ-MODIFY-WRITE CYCLE



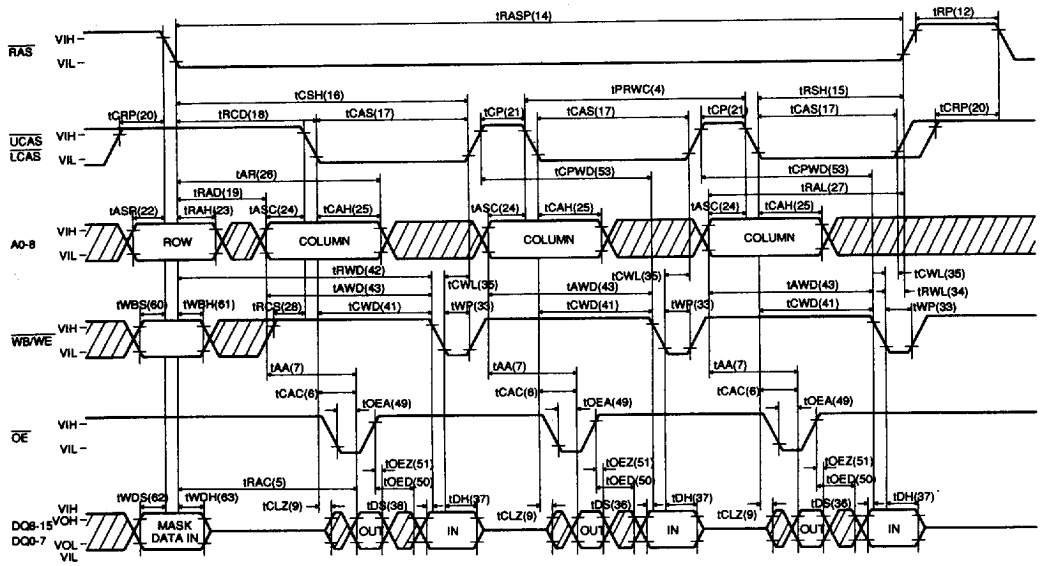
FAST PAGE MODE READ CYCLE



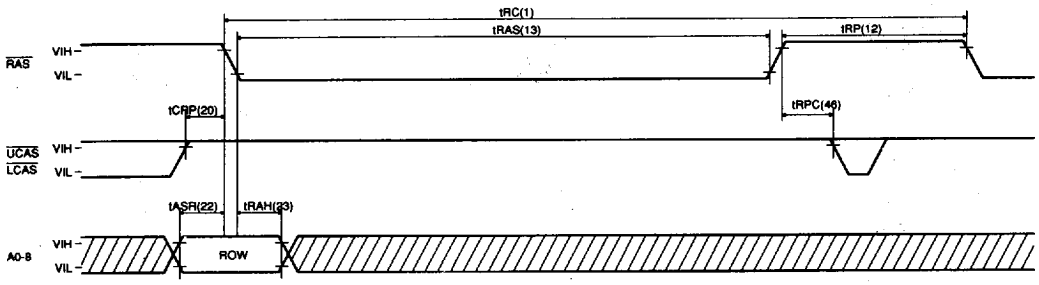
FAST PAGE MODE EARLY WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

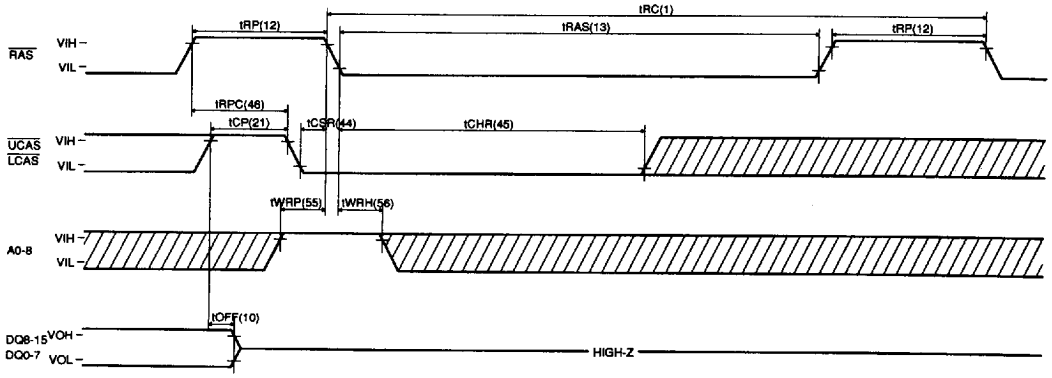


RAS-ONLY REFRESH CYCLE



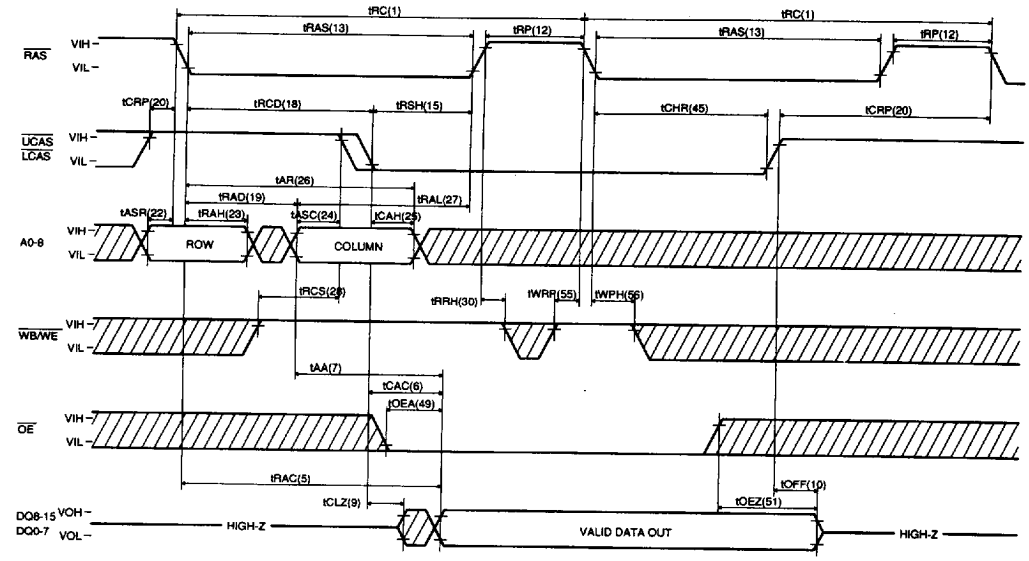
NOTE : $\overline{OE}$ and $\overline{WB/WE}$ = "H" or "L"

CAS-BEFORE-RAS REFRESH CYCLE

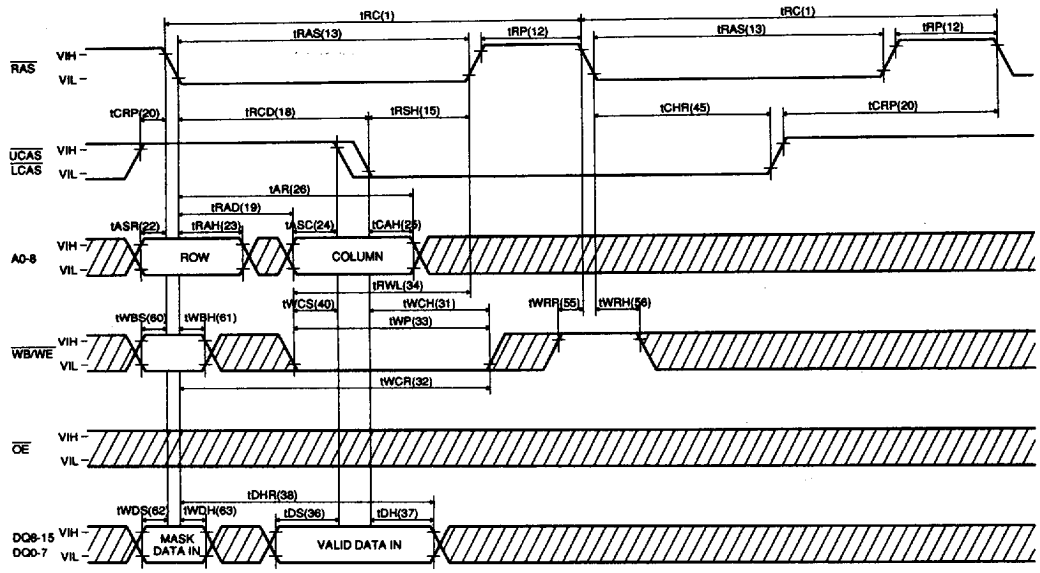


NOTE : A0-8 and $\overline{OE}$ = "H" or "L"

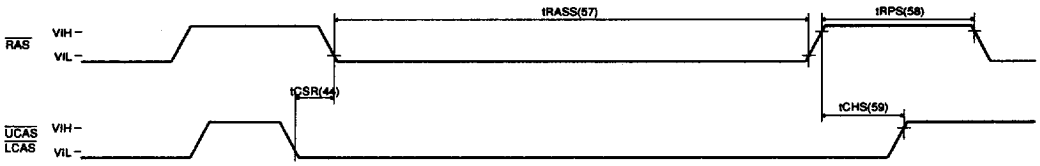
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

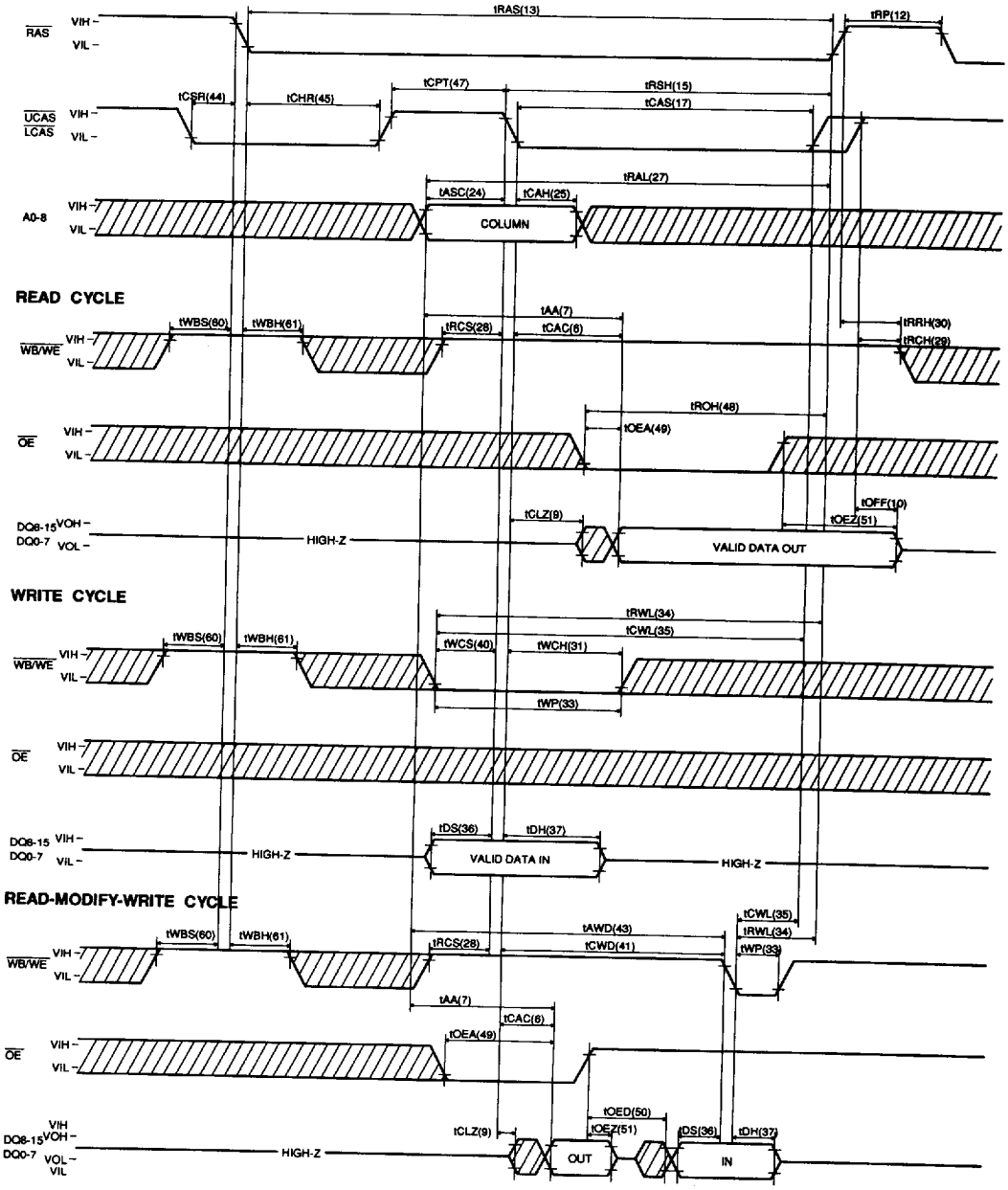


CAS-BEFORE-RAS SELF REFRESH CYCLE



NOTE : A0-8, WB/WE and OE = "H" or "L"

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



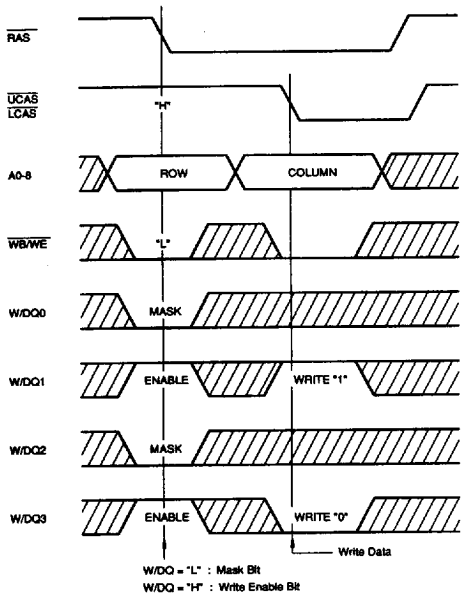
WRITE-PER-BIT FUNCTION

The Write-Per-Bit function selectively controls the internal write enable circuit of the HY514460B. When $\overline{WB/WE}$ is held "Low" at the falling edge of $\overline{RAS}$ during a random access operation, the write mask is enabled. At the sametime, the mask data on the W/DQ pins is located onto the write mask register (WMR). When a "0" is sensed on any of the W/DQ pins, their corresponding write circuits are disabled and new data will not be written. When "1" is sensed on any of the W/DQ pins, their corresponding write circuit will remain enabled so that new data is written. The truth table of the Write-Per-Bit function and an example of the Write-Per-Bit function illustrating its application to displays are shown below.

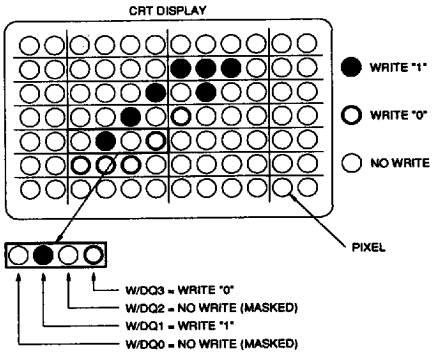
TRUTH TABLE FOR WRITE-PER-BIT FUNCTION

at the falling edge of $\overline{RAS}$			
$\overline{CAS}$	$\overline{WB/WE}$	W/DQ0-15	Function
H	H	Don't Care	Write Enable
H	L	1	Write Enable
		0	Write Mask

WRITE-PER-BIT TIMING DIAGRAM

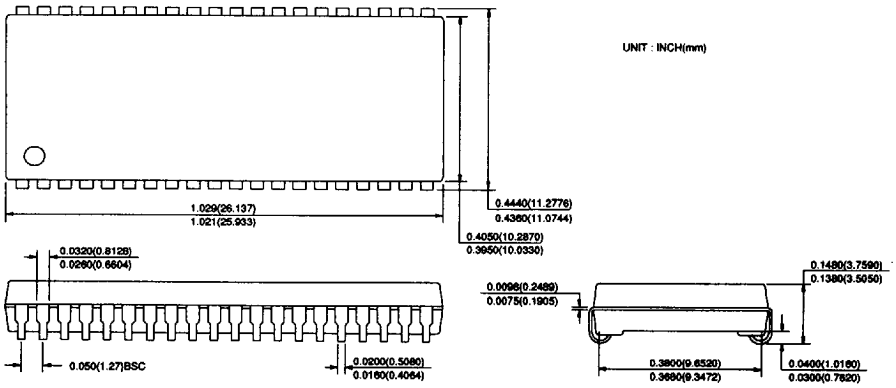


CORRESPONDING BIT MAP

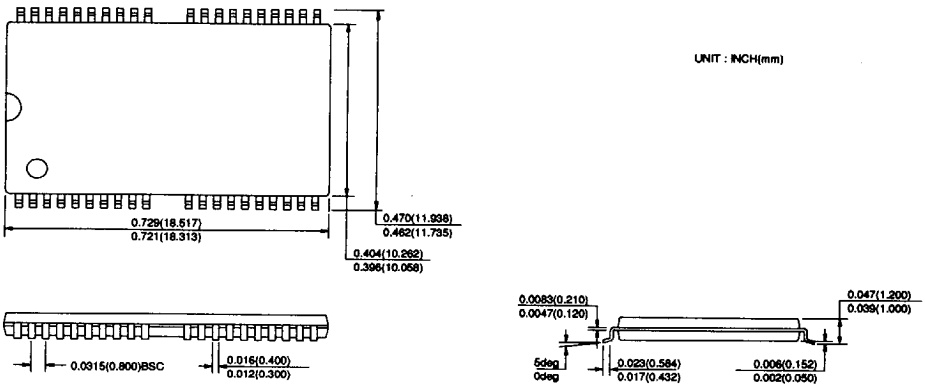


PACKAGE INFORMATION

400 mil 40 pin Small Outline J-form Package (JC)



400 mil 40/44 pin Thin Small Outline Package (TC) (RC)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE
HY514460BJC	60/70/80		SOJ
HY514460BLJC	60/70/80	L-part	SOJ
HY514460BSLJC	60/70/80	SL-part	SOJ
HY514460BTC	60/70/80		TSOP-II
HY514460BLTC	60/70/80	L-part	TSOP-II
HY514460BSLTC	60/70/80	SL-part	TSOP-II
HY514460BRC	60/70/80		TSOP-II(R)
HY514460BLRC	60/70/80	L-part	TSOP-II(R)
HY514460BSLRC	60/70/80	SL-part	TSOP-II(R)