

HM514800, HM514800L Series

524,288-word × 8-bit Dynamic Random Access Memory

HITACHI/ LOGIC/ARRAYS/MEM

The Hitachi HM514800 are CMOS dynamic RAM organized as 524,288-word × 8-bit. HM514800 have realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514800 offer Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514800 to be packaged in standard 400-mil 28-pin plastic SOJ, standard 400-mil 28-pin plastic ZIP, and 400-mil 28-pin plastic TSOP.

Features

- Single 5 V (± 10%)
- High speed
 - Access time: 70 ns/80 ns/100 ns (max)
- Low power dissipation
 - Active mode: 605 mW/550 mW/495 mW (max)
 - Standby mode: 11 mW (max)
 - 1.1 mW (max) (L-version)
- Fast page mode capability
- 1,024 refresh cycles: 16 ms
- 128 ms (L-version)
- 3 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh
- Battery back up operation (L-version)

Ordering Informations

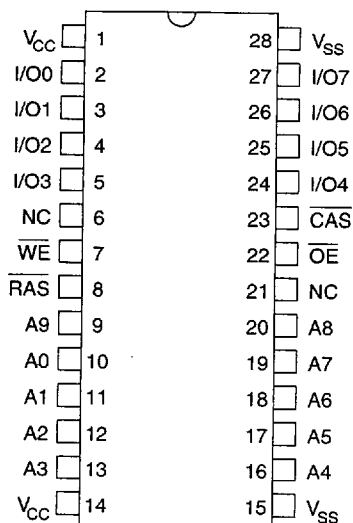
Type No.	Access time	Package
HM514800JP-7	70 ns	400-mil 28-pin plastic SOJ (CP-28D)
HM514800JP-8	80 ns	
HM514800JP-10	100 ns	
HM514800ZP-7	70 ns	400-mil 28-pin plastic ZIP (ZP-28)
HM514800ZP-8	80 ns	
HM514800ZP-10	100 ns	
HM514800TT-7	70 ns	400 mil 28-pin plastic TSOP (TTP-28D)
HM514800TT-8	80 ns	
HM514800TT-10	100 ns	
HM514800RR-7	70 ns	400-mil 28-pin plastic TSOP (TTP-28DR)
HM514800RR-8	80 ns	
HM514800RR-10	100 ns	
HM514800LJP-7	70 ns	400-mil 28-pin plastic SOJ (CP-28D)
HM514800LJP-8	80 ns	
HM514800LJP-10	100 ns	
HM514800LZP-7	70 ns	400-mil 28-pin plastic ZIP (ZP-28)
HM514800LZP-8	80 ns	
HM514800LZP-10	100 ns	
HM514800LTT-7	70 ns	400-mil 28-pin plastic TSOP (TTP-28D)
HM514800LTT-8	80 ns	
HM514800LTT-10	100 ns	
HM514800LRR-7	70 ns	400-mil 28-pin plastic TSOP (TTP-28DR)
HM514800LRR-8	80 ns	
HM514800LRR-10	100 ns	

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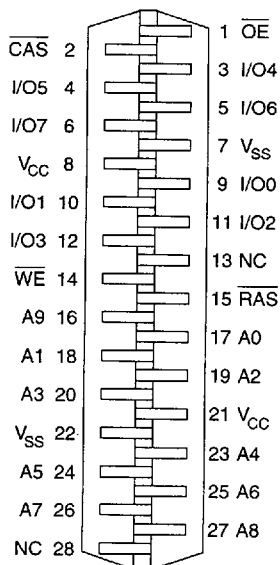
Pin Arrangement

HM514800JP/LJP Series



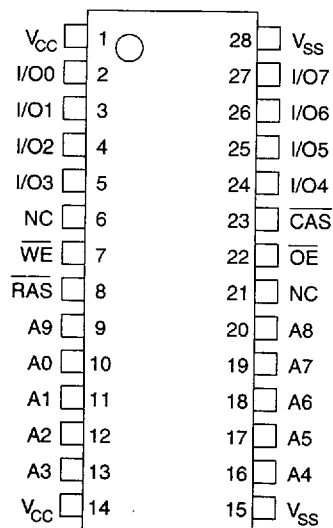
(Top View)

HM514800ZP/LZP Series



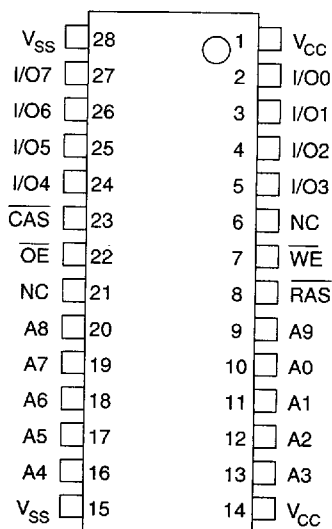
(Bottom View)

HM514800TT/LTT Series



(Top View)

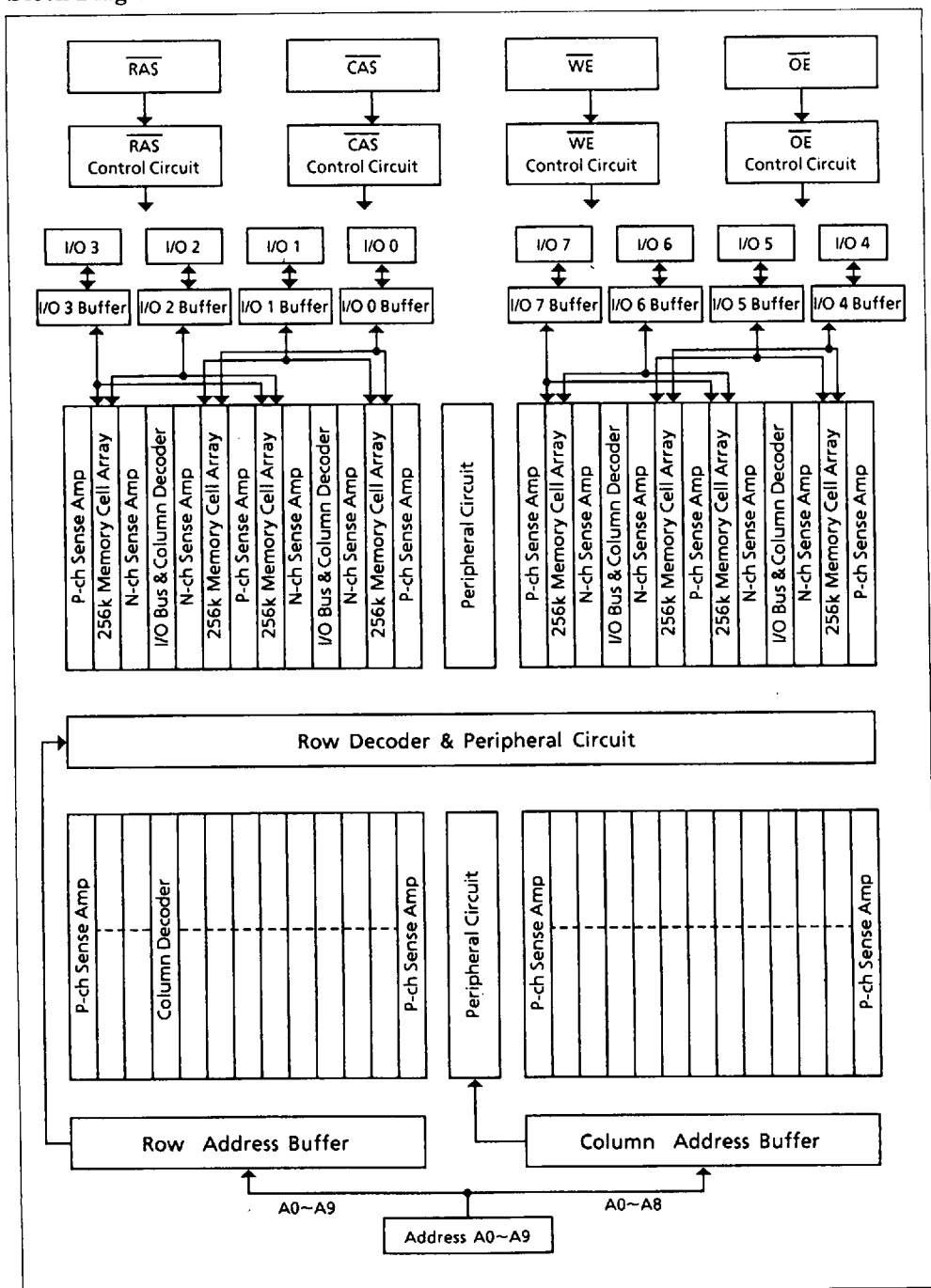
HM514800RR/LRR Series



(Top View)

— HITACHI/ LOGIC/ARRAYS/MEM HM514800, HM514800L Series

Block Diagram



HM514800, HM514800L Series

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Pin Description

Pin name	Function
A0 – A9	Address input – Row address A0 – A9 – Column address A0 – A8 – Refresh address A0 – A9
I/O0 – I/O7	Data-in/data-out
RAS	Row address strobe
CAS	Column address strobe

Pin name	Function
WE	Read/write enable
OE	Output enable
V _{CC}	Power (+5 V)
V _{SS}	Ground

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V _{SS}	V _T	–1.0 to +7.0	V
Supply voltage relative to V _{SS}	V _{CC}	–1.0 to +7.0	V
Short circuit output current	I _{out}	50	mA
Power dissipation	P _T	1.0	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	–55 to +125	°C

Recommended DC Operating Conditions (T_a = 0 to +70°C) *2

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V _{SS}	0	0	0	V	
	V _{CC}	4.5	5.0	5.5	V	1
Input high voltage	V _{IH}	2.4	—	6.5	V	1
Input low voltage	(I/O pin) V _{IL}	–1.0	—	0.8	V	1
	(Others) V _{IL}	–2.0	—	0.8	V	1

- Notes: 1. All voltage referenced to V_{SS}.
2. The supply voltage with all V_{CC} pins must be on the same level.
The supply voltage with all V_{SS} pins must be on the same level.

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DC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$) *5

Parameter	Symbol	HM514800-7		HM514800-8		HM514800-10		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Operating current	I_{CC1}	—	110	—	100	—	90	mA	RAS, CAS cycling $t_{RC} = \min$	1, 2
Standby current	I_{CC2}	—	2	—	2	—	2	mA	TTL interface RAS, CAS = V_{IH} Dout = High-Z	
		—	1	—	1	—	1	mA	CMOS interface RAS, CAS $\geq V_{CC} - 0.2\text{ V}$ Dout = High-Z	
Standby current (L-version)		—	200	—	200	—	200	μA	CMOS interface RAS, CAS $\geq V_{CC} - 0.2\text{ V}$ Dout = High-Z	
RAS-only refresh current	I_{CC3}	—	110	—	100	—	90	mA	$t_{RC} = \min$	2
Standby current	I_{CC5}	—	5	—	5	—	5	mA	RAS = V_{IH} CAS = V_{IL} Dout = enable	1
CAS-before-RAS refresh current	I_{CC6}	—	110	—	100	—	90	mA	$t_{RC} = \min$	
Fast page mode current	I_{CC7}	—	110	—	100	—	90	mA	$t_{PC} = \min$	1, 3
Battery back up current (Standby with CBR refresh) (L-version only)	I_{CC10}	—	300	—	300	—	300	μA	Standby: CMOS interface Dout = High-Z CBR refresh: $t_{RC} = 125\text{ }\mu\text{s}$ 4 $t_{RAS} \leq 1\text{ }\mu\text{s}$, CAS = V_{IL} WE = V_{IH}	
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	μA	$0\text{ V} \leq V_{in} \leq 7\text{ V}$	
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	μA	$0\text{ V} \leq V_{out} \leq 7\text{ V}$ Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = -5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

- Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while RAS = V_{IL} .
3. Address can be changed once or less while CAS = V_{IH} .
4. $V_{IH} \geq V_{CC} - 0.2\text{ V}$, $V_{IL} \leq 0.2\text{ V}$
5. The supply voltage with all V_{CC} pins must be on the same level.
The supply voltage with all V_{SS} pins must be on the same level.

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Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{\text{CAS}} = V_{IH}$ to disable Dout.

AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$) *1, *14, *15, *17

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514800-7		HM514800-8		HM514800-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130	—	150	—	180	—	ns	
RAS precharge time	t_{RP}	50	—	60	—	70	—	ns	
RAS pulse width	t_{RAS}	70	10000	80	10000	100	10000	ns	
CAS pulse width	t_{CAS}	20	10000	20	10000	25	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	15	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	20	—	ns	
RAS to CAS delay time	t_{RCD}	20	50	20	60	25	75	ns	8
RAS to column address delay time	t_{RAD}	15	35	15	40	20	55	ns	9
RAS hold time	t_{RSH}	20	—	20	—	25	—	ns	
CAS hold time	t_{CSH}	70	—	80	—	100	—	ns	
CAS to RAS precharge time	t_{CRP}	10	—	10	—	10	—	ns	

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Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters) (cont)

Parameter	Symbol	HM514800-7		HM514800-8		HM514800-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{OE}$ to Din delay time	t_{ODD}	20	—	20	—	25	—	ns	
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{CAS}$ setup time from Din	t_{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7
Refresh period	t_{REF}	—	16	—	16	—	16	ms	
Refresh period (L-version)	t_{REF}	—	128	—	128	—	128	ms	

Read Cycle

Parameter	Symbol	HM514800-7		HM514800-8		HM514800-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	2, 3
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	ns	3, 4, 13
Access time from address	t_{AA}	—	35	—	40	—	45	ns	3, 5, 13
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	
Output buffer turn-off time	t_{OFF1}	0	15	0	15	0	20	ns	6
Output buffer turn-off to $\overline{OE}$	t_{OFF2}	0	15	0	15	0	20	ns	6
$\overline{CAS}$ to Din delay time	t_{CDD}	15	—	15	—	20	—	ns	

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Write Cycle

Parameter	Symbol	HM514800-7 HM514800-8 HM514800-10						Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	10
Write command hold time	t_{WCH}	15	—	15	—	20	—	ns	
Write command pulse width	t_{WPP}	10	—	10	—	20	—	ns	
Write command to RAS lead time	t_{RWL}	20	—	20	—	25	—	ns	
Write command to CAS lead time	t_{CWL}	20	—	20	—	25	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in hold time	t_{DH}	15	—	15	—	20	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM514800-7 HM514800-8 HM514800-10						Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time	t_{RWC}	180	—	200	—	245	—	ns	
RAS to WE delay time	t_{RWD}	95	—	105	—	135	—	ns	10
CAS to WE delay time	t_{CWD}	45	—	45	—	60	—	ns	10
Column address to WE delay time	t_{AWD}	60	—	65	—	80	—	ns	10, 13
OE hold time from WE	t_{OEHL}	20	—	20	—	25	—	ns	

Refresh Cycle

Parameter	Symbol	HM514800-7 HM514800-8 HM514800-10						Unit	Notes
		Min	Max	Min	Max	Min	Max		
CAS setup time (CAS-before-RAS refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	
CAS hold time (CAS-before-RAS refresh cycle)	t_{CHR}	10	—	10	—	10	—	ns	
RAS precharge to CAS hold time	t_{RPC}	10	—	10	—	10	—	ns	
CAS precharge time in normal mode	t_{CPN}	10	—	10	—	10	—	ns	

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Fast Page Mode Cycle

HM514800-7 HM514800-8 HM514800-10

Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode cycle time	t_{PC}	45	—	50	—	55	—	ns	
Fast page mode $\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	40	—	45	—	50	ns	3, 13
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40	—	45	—	50	—	ns	
Fast page mode read-modify-write cycle $\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPW}	65	—	70	—	85	—	ns	
Fast page mode read-modify-write cycle time	t_{PCM}	95	—	100	—	110	—	ns	

Counter Test Cycle

HM514800-7 HM514800-8 HM514800-10

Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ precharge time in counter test cycle	t_{CPT}	50	—	50	—	50	—	ns	

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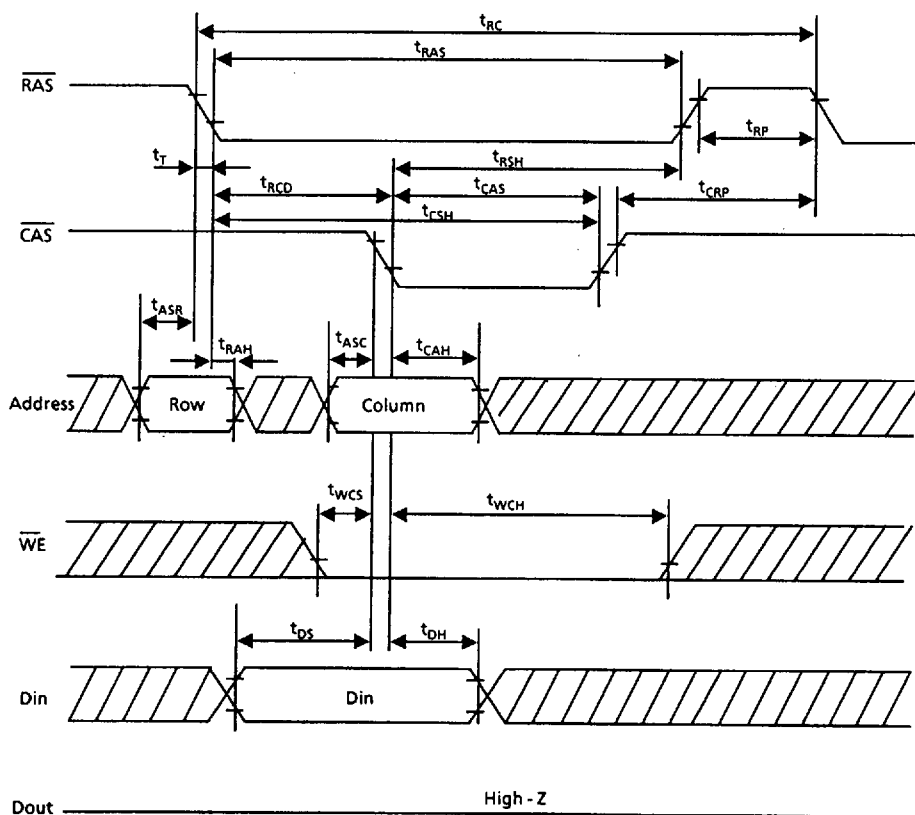
- Notes:
1. AC measurements assume $t_T = 5 \text{ ns}$.
 2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 4. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$.
 5. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \geq t_{RAD}(\text{max})$.
 6. $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
 7. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 8. Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
 9. Operation with the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RAD}(\text{max})$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
 10. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(\text{min})$, $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{AWD} \geq t_{AWD}(\text{min})$ and $t_{CPW} \geq t_{CPW}(\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 11. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in an early write cycle and to $\overline{\text{WE}}$ leading edge in a delayed write or a read-modify-write cycle.
 12. t_{RASC} defines $\overline{\text{RAS}}$ pulse width in fast page mode cycles.
 13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP} .
 14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh cycle or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles is required.
 15. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device.
 16. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 17. The supply voltage with all V_{CC} pins must be on the same level.
The supply voltage with all V_{SS} pins must be on the same level.

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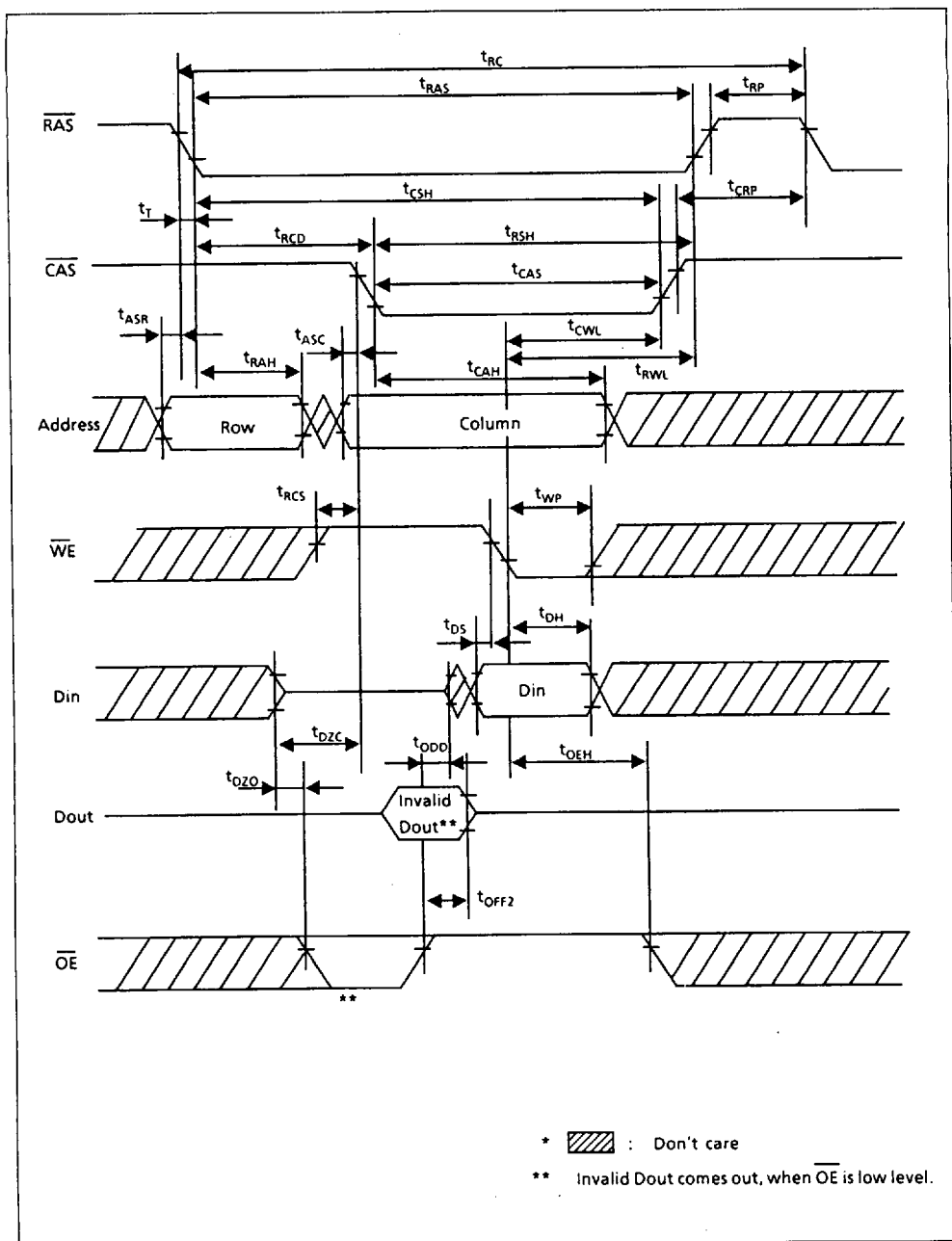
HM514800, HM514800L Series**Early Write Cycle**

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* : Don't care

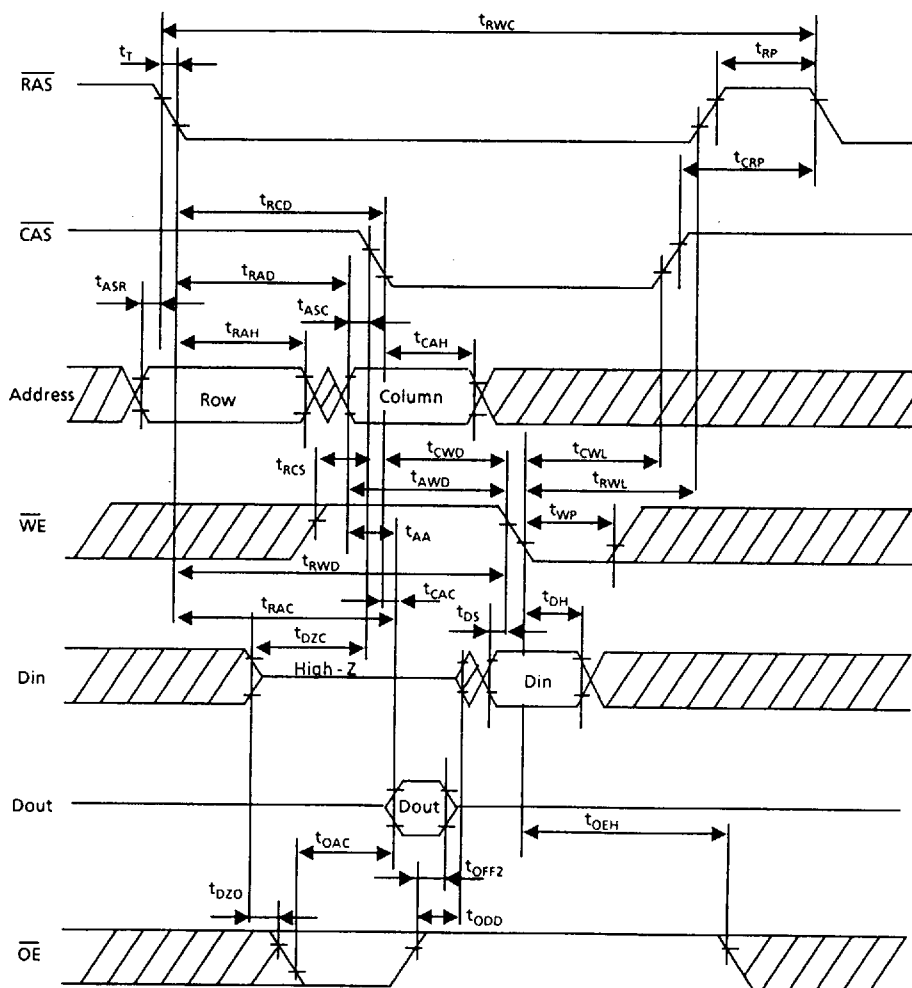
** $\overline{\text{OE}}$: Don't care

HITACHI/ LOGIC/ARRAYS/MEM **HM514800, HM514800L Series****Delayed Write Cycle**

HM514800, HM514800L Series

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Read-Modify-Write Cycle

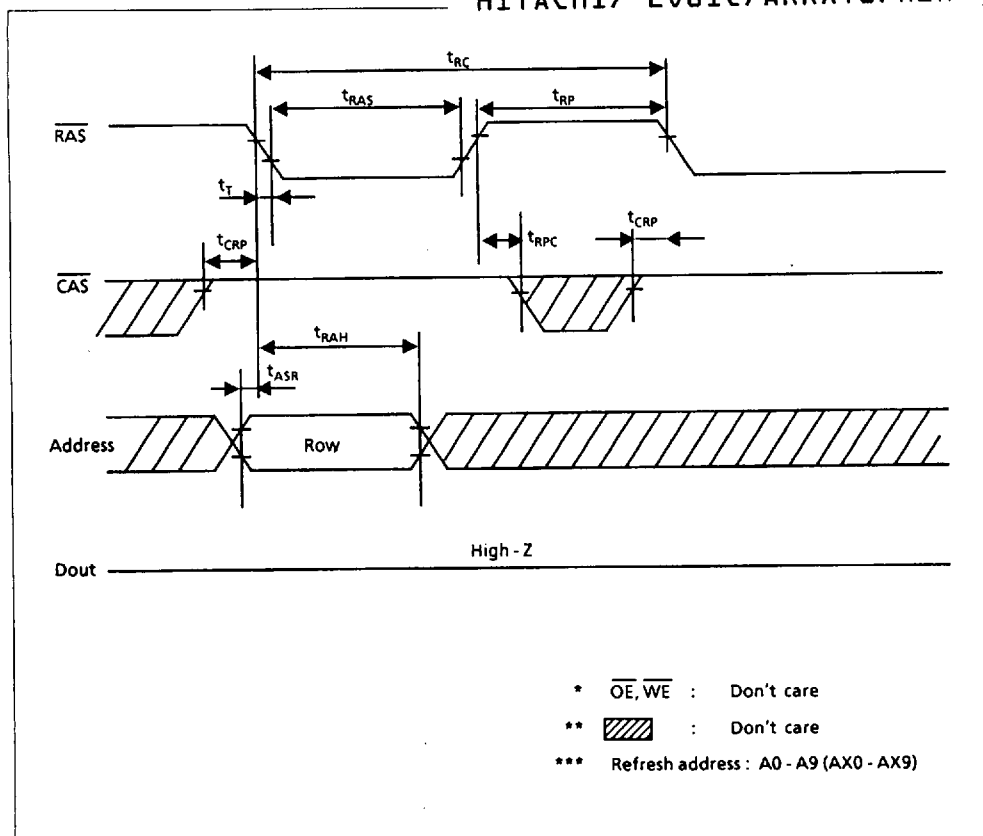


* : Don't care

HM514800, HM514800L Series

RAS-Only Refresh Cycle

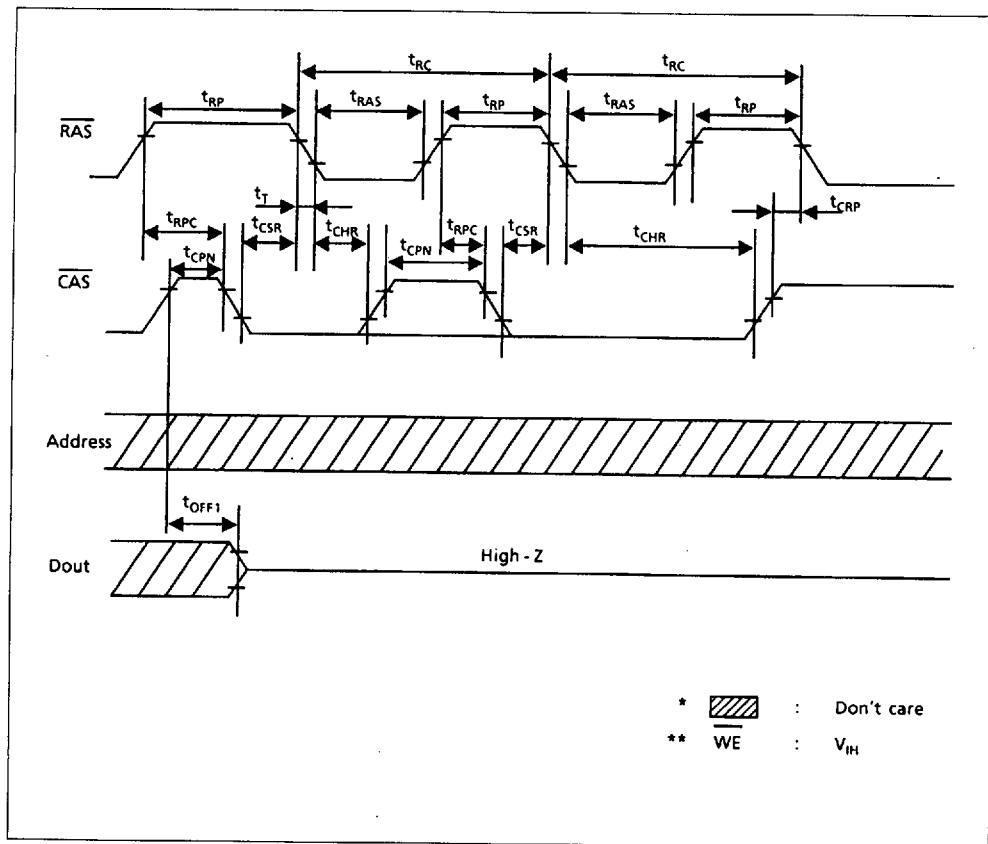
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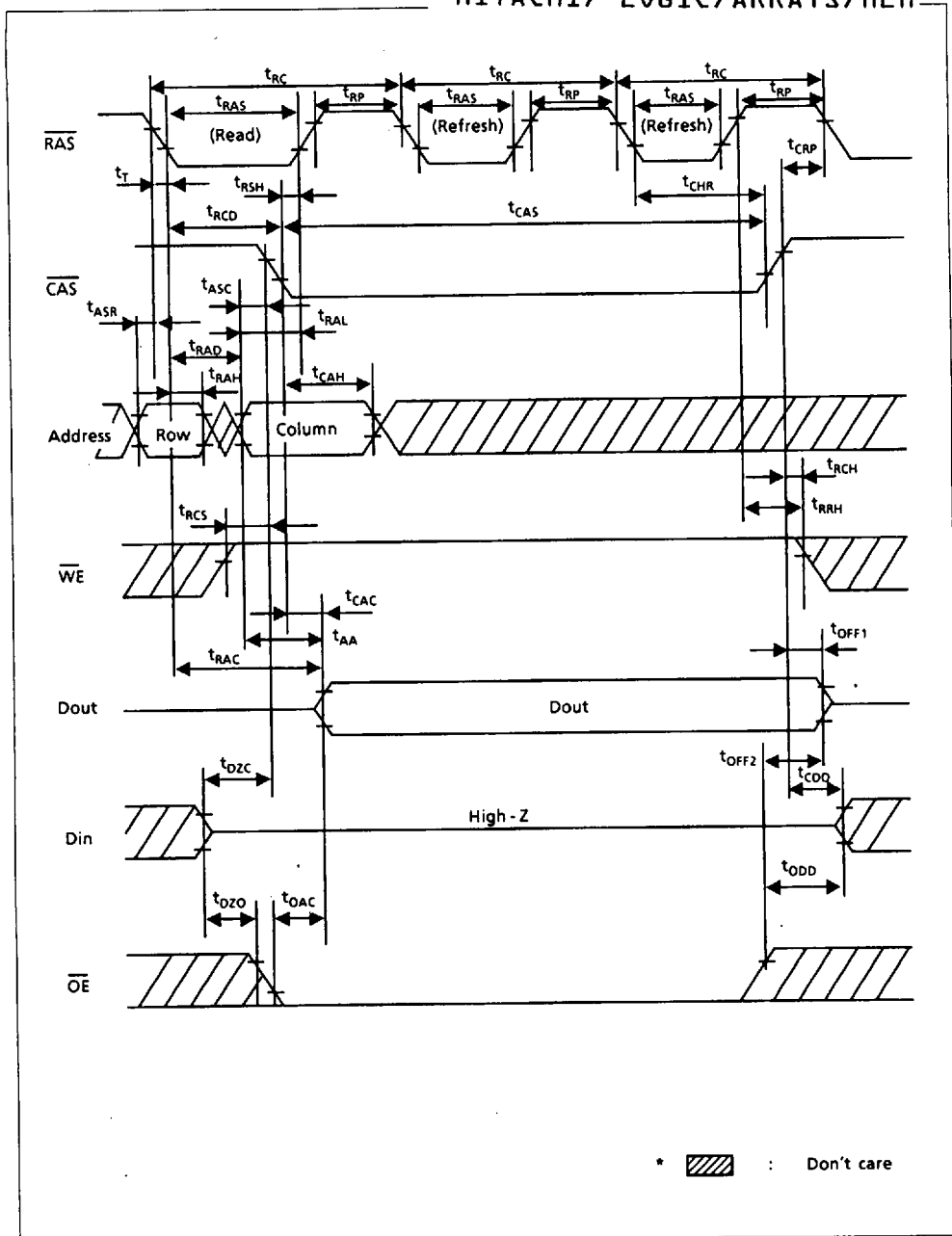
CAS-Before-RAS Refresh Cycle



HM514800, HM514800L Series

Hidden Refresh Cycle

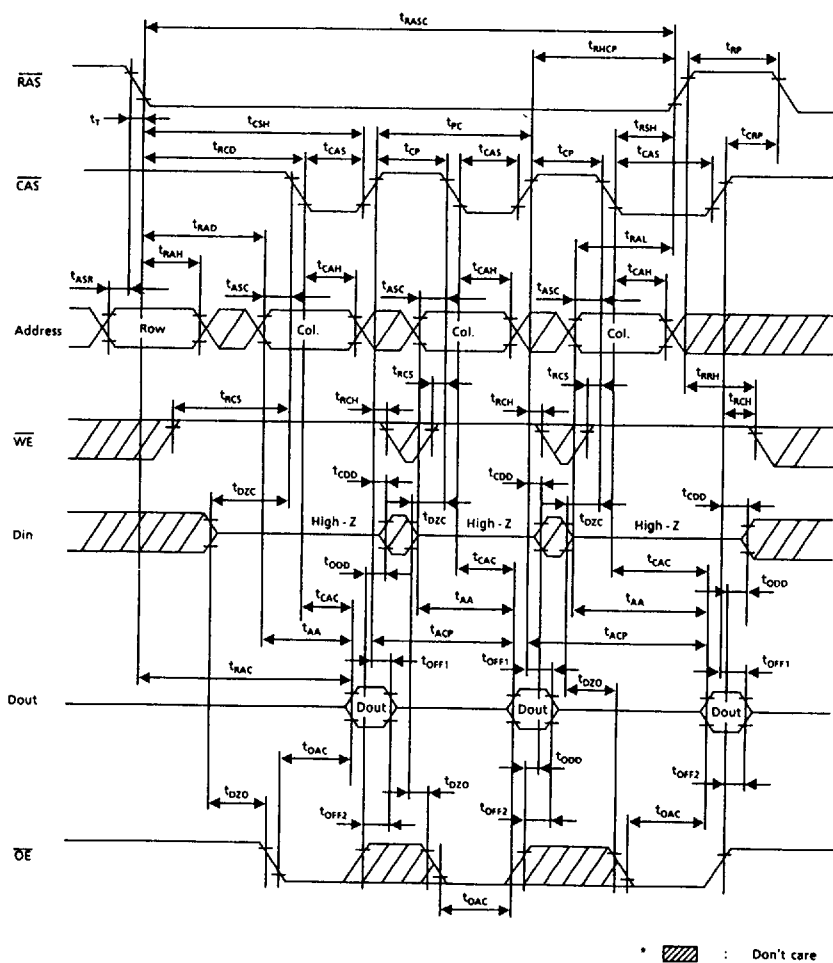
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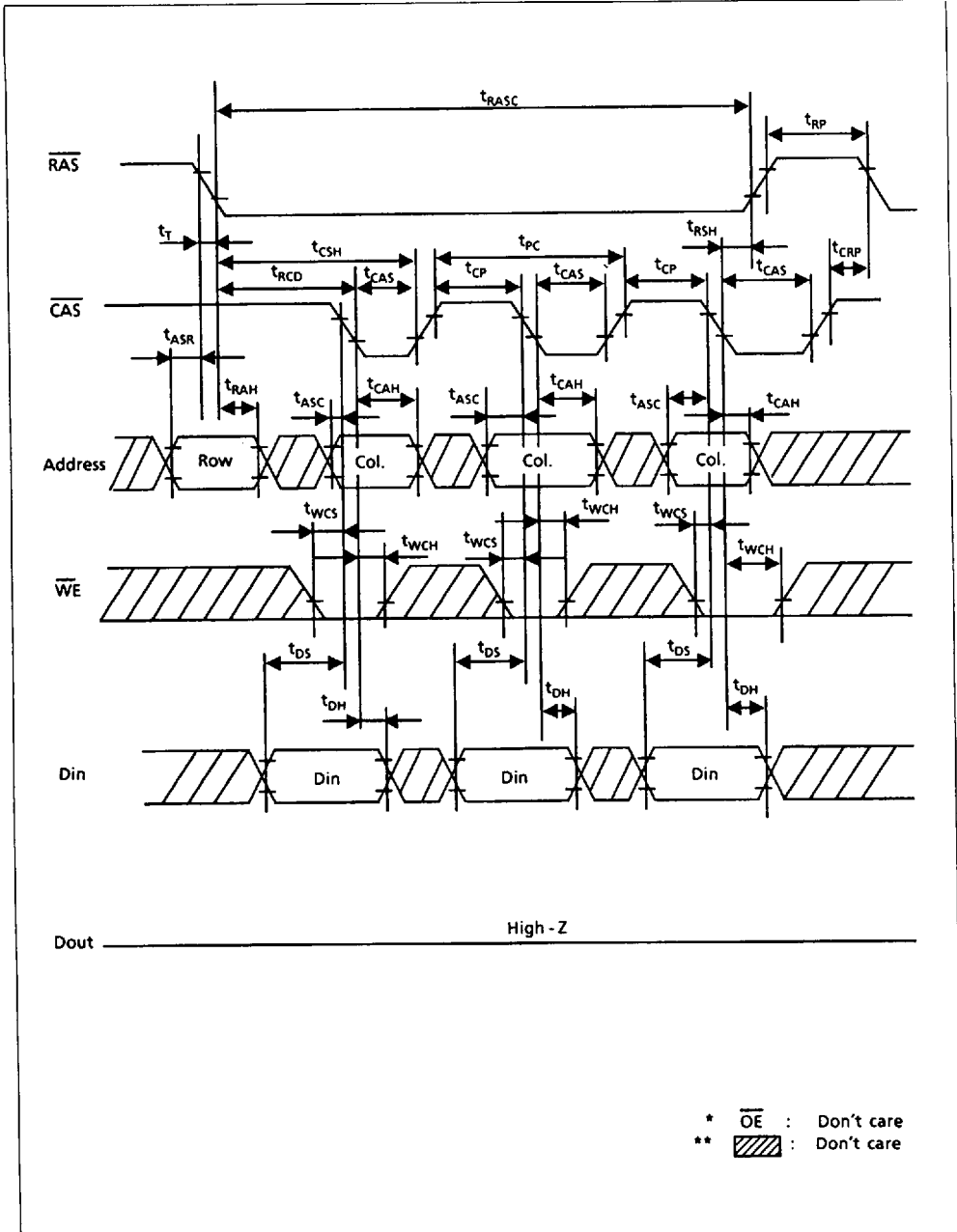
Fast Page Mode Read Cycle



HM514800, HM514800L Series

Fast Page Mode Early Write Cycle

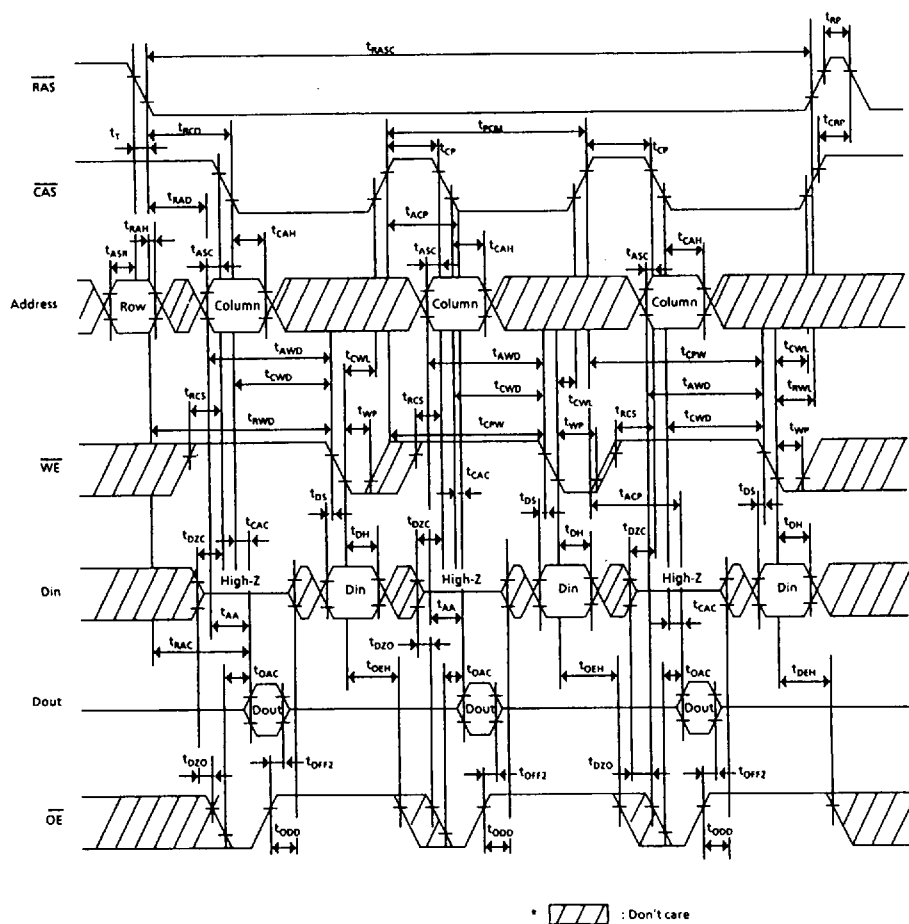
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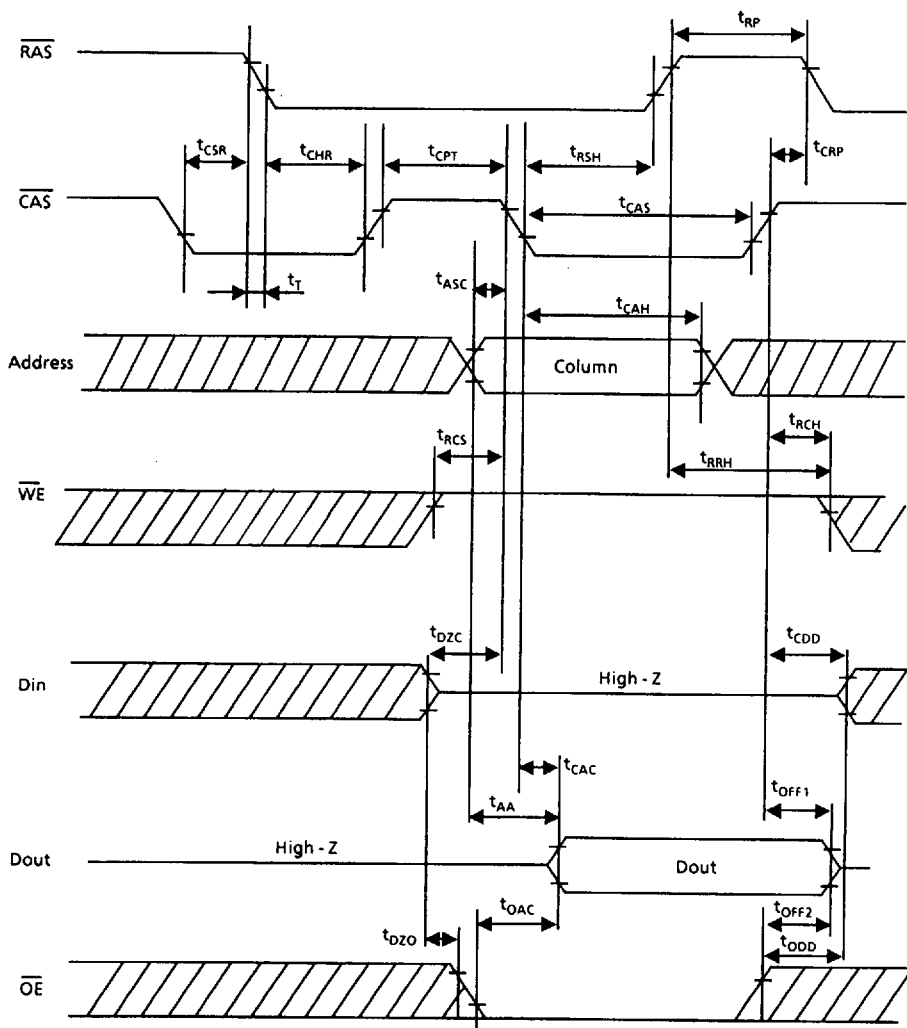


HM514800, HM514800L Series

Fast Page Mode Read-Modify-Write Cycle

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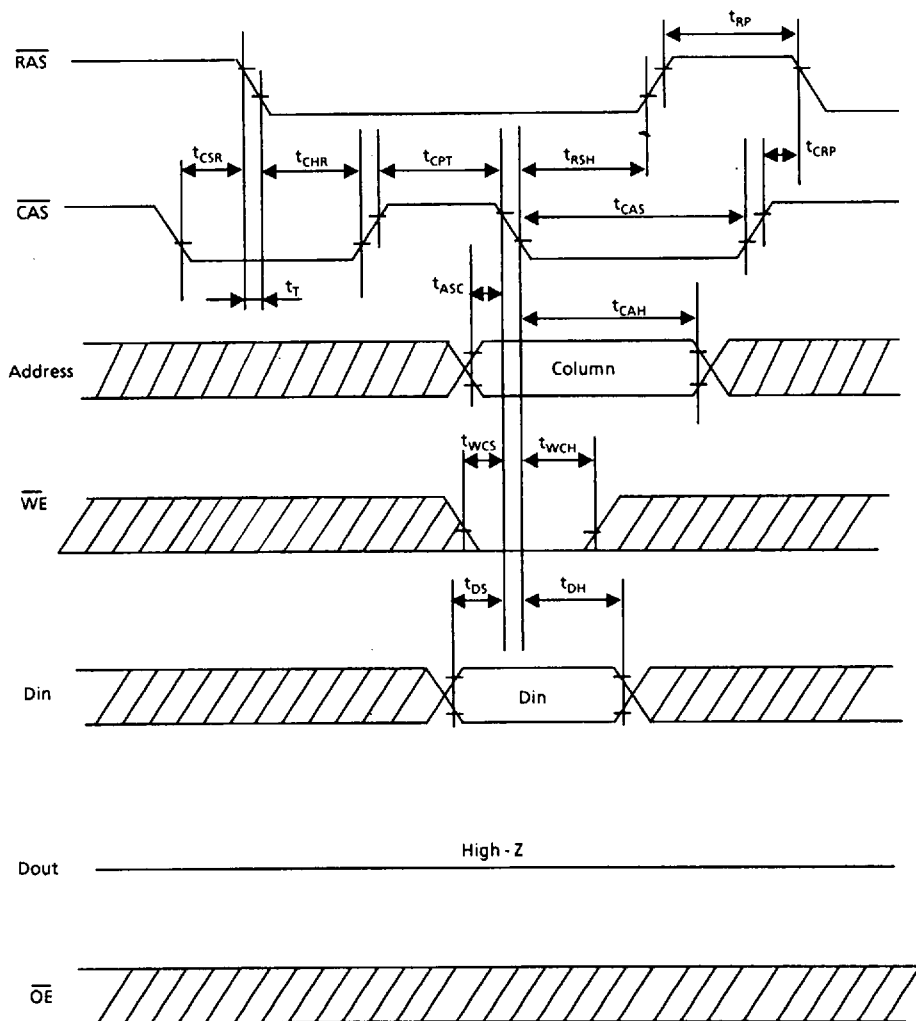


HM514800, HM514800L Series**CAS-Before-RAS Refresh Counter Check Cycle (Read)****HITACHI/ LOGIC/ARRAYS/MEM**

HM514800, HM514800L Series

CAS-Before-RAS Refresh Counter Check Cycle (Write)

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* : Don't care