

HM514800C/CL Series

HM51S4800C/CL Series

524,288-word x 8-bit Dynamic Random Access Memory

HITACHI

Rev. 1
Apr. 20, 1994

The Hitachi HM514800C are CMOS dynamic RAM organized as 524,288-word x 8-bit. HM514800C have realized higher density, higher performance and various functions by employing 0.8 μ m CMOS process technology and some new CMOS circuit design technologies. The HM514800C offer Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514800C to be packaged in standard 400-mil 28-pin plastic SOJ, standard 400-mil 28-pin plastic ZIP and standard 400-mil 28-pin plastic TSOPII.

Internal refresh timer enables HM51S4800C/CL self refresh operation.

Features

- Single 5 V ($\pm 10\%$)
- High speed
 - Access time: 60 ns/70 ns/80 ns (max)
- Low power dissipation
 - Active mode: 605 mW/550 mW/495 mW (max)
 - Standby mode: 11 mW (max)
1.1 mW (max) (L-version)
- Fast page mode capability
- 1,024 refresh cycles: 16 ms
128 ms (L-version)
- 2 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - CAS-before-RAS refresh
- Battery back up operation (L-version)
- Self-refresh operation (HM51S4800C/CL)

ADE-203-242A(Z)

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Ordering Information

Type No.	Access time	Package
HM514800CJ-6	60 ns	400-mil 28-pin
HM514800CJ-7	70 ns	plastic SOJ
HM514800CJ-8	80 ns	(CP-28D)
HM514800CZ-6	60 ns	400-mil 28-pin
HM514800CZ-7	70 ns	plastic ZIP
HM514800CZ-8	80 ns	(ZP-28)
HM514800CLJ-6	60 ns	400-mil 28-pin
HM514800CLJ-7	70 ns	plastic SOJ
HM514800CLJ-8	80 ns	(CP-28D)
HM514800CLZ-6	60 ns	400-mil 28-pin
HM514800CLZ-7	70 ns	plastic ZIP
HM514800CLZ-8	80 ns	(ZP-28)
HM514800CTT-6	60 ns	400-mil 28-pin
HM514800CTT-7	70 ns	plastic TSOPII
HM514800CTT-8	80 ns	(TTP-28D)
HM514800CLTT-6	60 ns	400-mil 28-pin
HM514800CLTT-7	70 ns	plastic TSOPII
HM514800CLTT-8	80 ns	(TTP-28D)

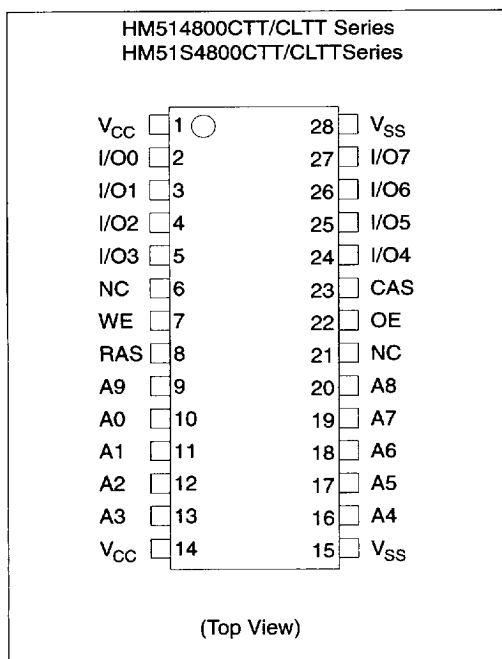
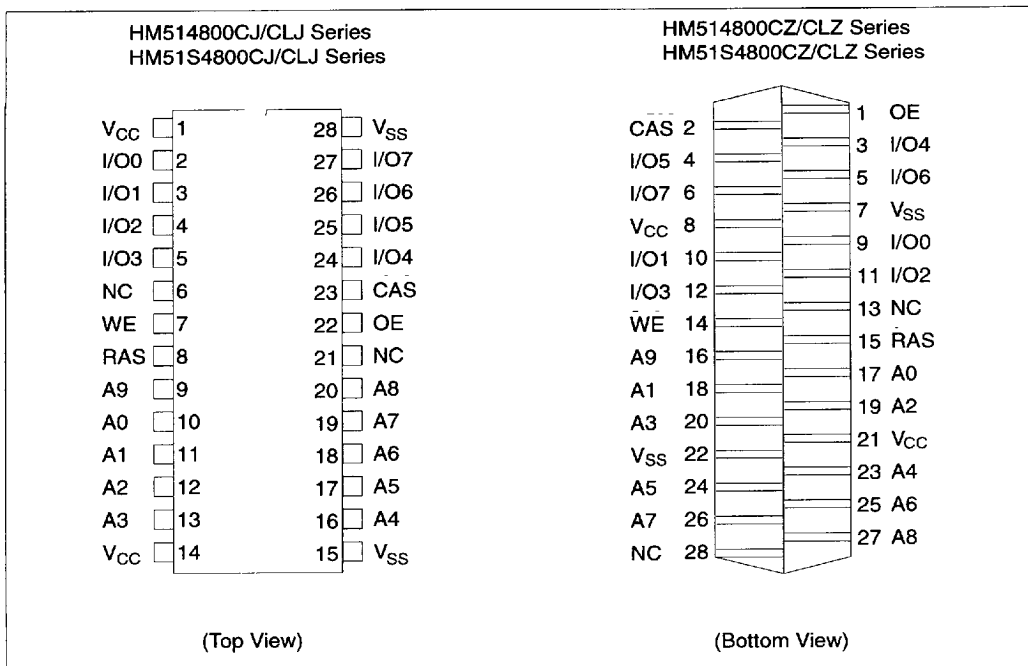
Type No.	Access time	Package
HM51S4800CJ-6	60 ns	400-mil 28-pin
HM51S4800CJ-7	70 ns	plastic SOJ
HM51S4800CJ-8	80 ns	(CP-28D)
HM51S4800CZ-6	60 ns	400-mil 28-pin
HM51S4800CZ-7	70 ns	plastic ZIP
HM51S4800CZ-8	80 ns	(ZP-28)
HM51S4800CLJ-6	60 ns	400-mil 28-pin
HM51S4800CLJ-7	70 ns	plastic SOJ
HM51S4800CLJ-8	80 ns	(CP-28D)
HM51S4800CLZ-6	60 ns	400-mil 28-pin
HM51S4800CLZ-7	70 ns	plastic ZIP
HM51S4800CLZ-8	80 ns	(ZP-28)
HM51S4800CTT-6	60 ns	400-mil 28-pin
HM51S4800CTT-7	70 ns	plastic TSOPII
HM51S4800CTT-8	80 ns	(TTP-28D)
HM51S4800CLTT-6	60 ns	400-mil 28-pin
HM51S4800CLTT-7	70 ns	plastic TSOPII
HM51S4800CLTT-8	80 ns	(TTP-28D)

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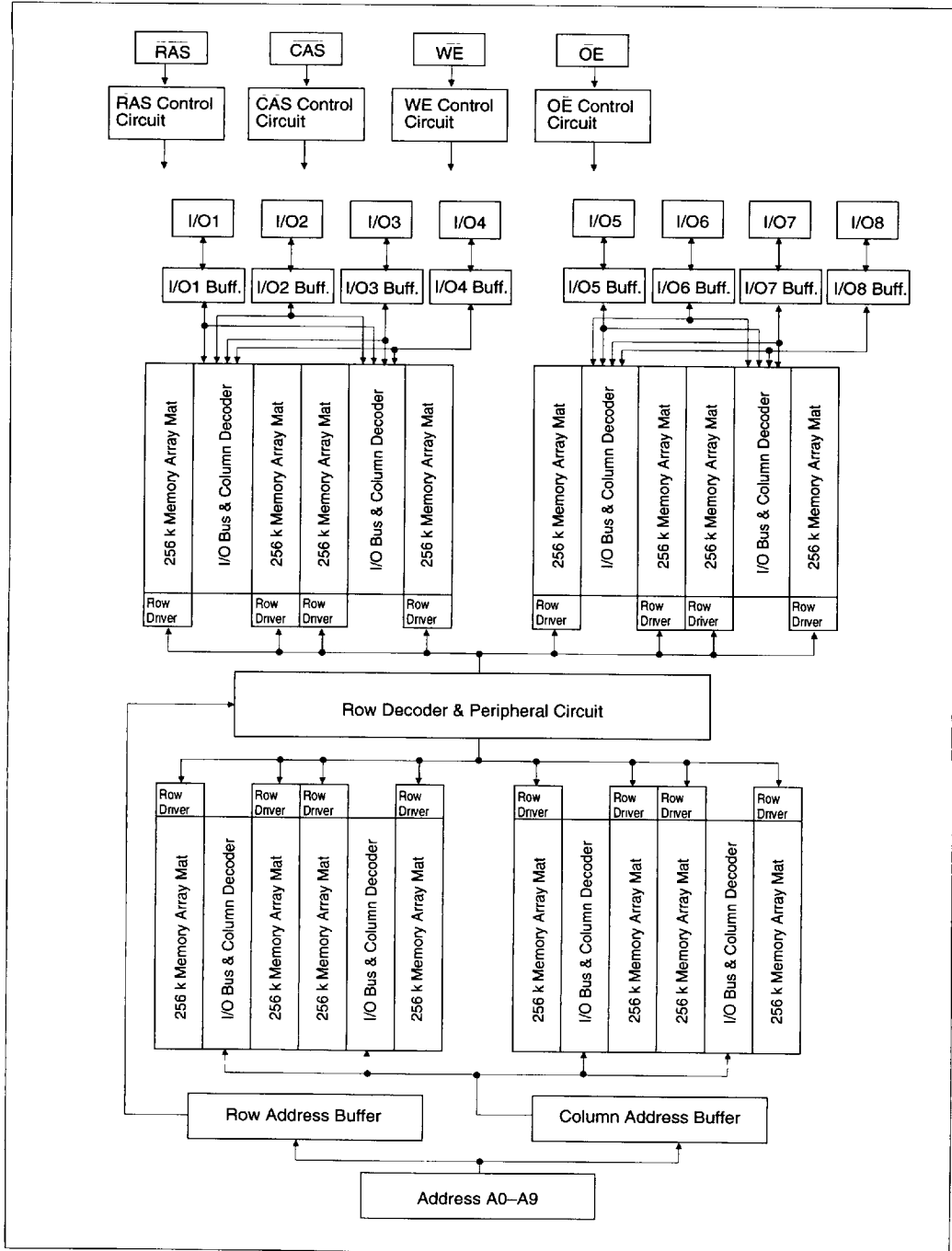
Pin Arrangement



Pin Description

Pin name	Function	
A0 – A9	Address input	
–	Row address	A0 – A9
–	Column address	A0 – A8
–	Refresh address	A0 – A9
I/O0 – I/O8	Data-in/data-out	
RAS	Row address strobe	
CAS	Column address strobe	
WE	Read/write enable	
OE	Output enable	
V _{CC}	Power (+5 V)	
V _{SS}	Ground	

Block Diagram



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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to +70°C) *2

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	2
	V_{CC}	4.5	5.0	5.5	V	1, 2
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	(I/O pin) V_{IL}	-1.0	—	0.8	V	1
	(Others) V_{IL}	-2.0	—	0.8	V	1

Notes: 1. All voltage referred to V_{SS} .
2. The supply voltage with all V_{CC} pins must be on the same level.
The supply voltage with all V_{SS} pins must be on the same level.

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DC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$) *5

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Parameter	Symbol	-6		-7		-8		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Operating current	I_{CC1}	—	120	—	110	—	100	mA	$\overline{\text{RAS}}, \overline{\text{CAS}}$ cycling $t_{RC} = \text{min}$	1, 2
Standby current	I_{CC2}	—	2	—	2	—	2	mA	TTL interface $\overline{\text{RAS}}, \overline{\text{CAS}} = V_{IH}$ Dout = High-Z	
		—	1	—	1	—	1	mA	CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2\text{ V}$ Dout = High-Z	
Standby current (L-version)		—	200	—	200	—	200	μA	CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2\text{ V}$ Dout = High-Z	
$\overline{\text{RAS}}$ -only refresh current	I_{CC3}	—	120	—	110	—	100	mA	$t_{RC} = \text{min}$	2
Standby current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{\text{RAS}} = V_{IH}$ $\overline{\text{CAS}} = V_{IL}$ Dout = enable	1
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh current	I_{CC6}	—	120	—	110	—	100	mA	$t_{RC} = \text{min}$	4
Fast page mode current	I_{CC7}	—	120	—	110	—	100	mA	$t_{PC} = \text{min}$	1, 3
Battery back up current (Standby with CBR refresh) (L-version only)	I_{CC10}	—	300	—	300	—	300	μA	Standby: CMOS interface Dout = High-Z CBR refresh: $t_{RC} = 125\text{ }\mu\text{s}$ $t_{RAS} \leq 1\text{ }\mu\text{s}$, $\overline{\text{CAS}} = V_{IL}$ $\overline{\text{WE}} = V_{IH}$	4
Self-refresh mode current (HM51S4800C)	I_{CC11}	—	1	—	1	—	1	mA	CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}} \leq 0.2\text{ V}$ Dout = High-Z	
Self-refresh mode current (HM51S4800CL)		—	200	—	200	—	200	μA	CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}} \leq 0.2\text{ V}$ Dout = High-Z	
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	μA	$0\text{ V} \leq V_{in} \leq 6.5\text{ V}$	
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	μA	$0\text{ V} \leq V_{out} \leq 6.5\text{ V}$ Dout = disable	

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DC Characteristics (cont.)

HM514800C/CL, HM51S4800C/CL										
		-6		-7		-8				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = -5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.
3. Address can be changed once or less within one page cycle.
4. $V_{IH} \geq V_{CC} - 0.2$ V, $V_{IL} \leq 0.2$ V; Address can be changed once or less while $\overline{CAS} = V_{IL}$.
5. The supply voltage with all V_{CC} pins must be on the same level.
The supply voltage with all V_{SS} pins must be on the same level.

Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS} = V_{IH}$ to disable Dout.

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AC Characteristics ($T_a = 0$ to 70°C , $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$) *1, *14, *15

Test conditions

- Input rise and fall times: 5 ns
- Input timing reference levels: 0.8 V, 2.4 V
- Input levels: 0 V, 3 V
- Output load: 2 TTL gate + C_L (100 pF)
(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

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Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110	—	130	—	150	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	—	50	—	60	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10000	20	10000	20	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	8
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	9
$\overline{RAS}$ hold time	t_{RSH}	20	—	20	—	20	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	ns	
$\overline{OE}$ to Din delay time	t_{ODD}	15	—	20	—	20	—	ns	
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{CAS}$ setup time from Din	t_{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7
Refresh period	t_{REF}	—	16	—	16	—	16	ms	
Refresh period (L-version)	t_{REF}	—	128	—	128	—	128	ms	

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Read Cycle

		HM514800C/CL, HM51S4800C/CL							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	—	80	ns	2, 3
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	15	—	20	—	20	ns	3, 4, 13
Access time from address	t_{AA}	—	30	—	35	—	40	ns	3, 5, 13
Access time from $\overline{\text{OE}}$	t_{OAC}	—	15	—	20	—	20	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	0	—	ns	
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	30	—	35	—	40	—	ns	
Output buffer turn-off time	t_{OFF1}	0	15	0	15	0	15	ns	6
Output buffer turn-off to $\overline{\text{OE}}$	t_{OFF2}	0	15	0	15	0	15	ns	6
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	15	—	15	—	15	—	ns	

Write Cycle

		HM514800C/CL, HM51S4800C/CL							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	10
Write command hold time	t_{WCH}	15	—	15	—	15	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	10	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	15	—	20	—	20	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	15	—	20	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in hold time	t_{DH}	15	—	15	—	15	—	ns	11
$\overline{\text{CAS}}$ to $\overline{\text{OE}}$ delay time	t_{COD}	—	0	—	0	—	0	ns	18

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Read-Modify-Write Cycle

		HM514800C/CL, HM51S4800C/CL							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	150	—	180	—	200	—	ns	
RAS to $\overline{WE}$ delay time	t_{RWD}	80	—	95	—	105	—	ns	10
CAS to $\overline{WE}$ delay time	t_{CWD}	35	—	45	—	45	—	ns	10
Column address to $\overline{WE}$ delay time	t_{AWD}	50	—	60	—	65	—	ns	10, 13
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEh}	15	—	20	—	20	—	ns	

Refresh Cycle

		HM514800C/CL, HM51S4800C/CL							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
CAS setup time ($\overline{CAS}$ -before-RAS refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	
CAS hold time ($\overline{CAS}$ -before-RAS refresh cycle)	t_{CHR}	10	—	10	—	10	—	ns	
RAS precharge to CAS hold time	t_{RPC}	10	—	10	—	10	—	ns	
CAS precharge time in normal mode	t_{CPN}	10	—	10	—	10	—	ns	

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Fast Page Mode Cycle

		HM514800C/CL, HM51S4800C/CL							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode cycle time	t _{PC}	40	—	45	—	50	—	ns	
Fast page mode $\overline{\text{CAS}}$ precharge time	t _{CP}	10	—	10	—	10	—	ns	
Fast page mode $\overline{\text{RAS}}$ pulse width	t _{RASC}	—	100000	—	100000	—	100000	ns	12
Access time from $\overline{\text{CAS}}$ precharge	t _{ACP}	—	35	—	40	—	45	ns	3, 13
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t _{RHCP}	35	—	40	—	45	—	ns	
Fast page mode read-modify-write cycle $\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$ delay time	t _{CPW}	55	—	65	—	70	—	ns	
Fast page mode read-modify-write cycle time	t _{PCM}	80	—	95	—	100	—	ns	

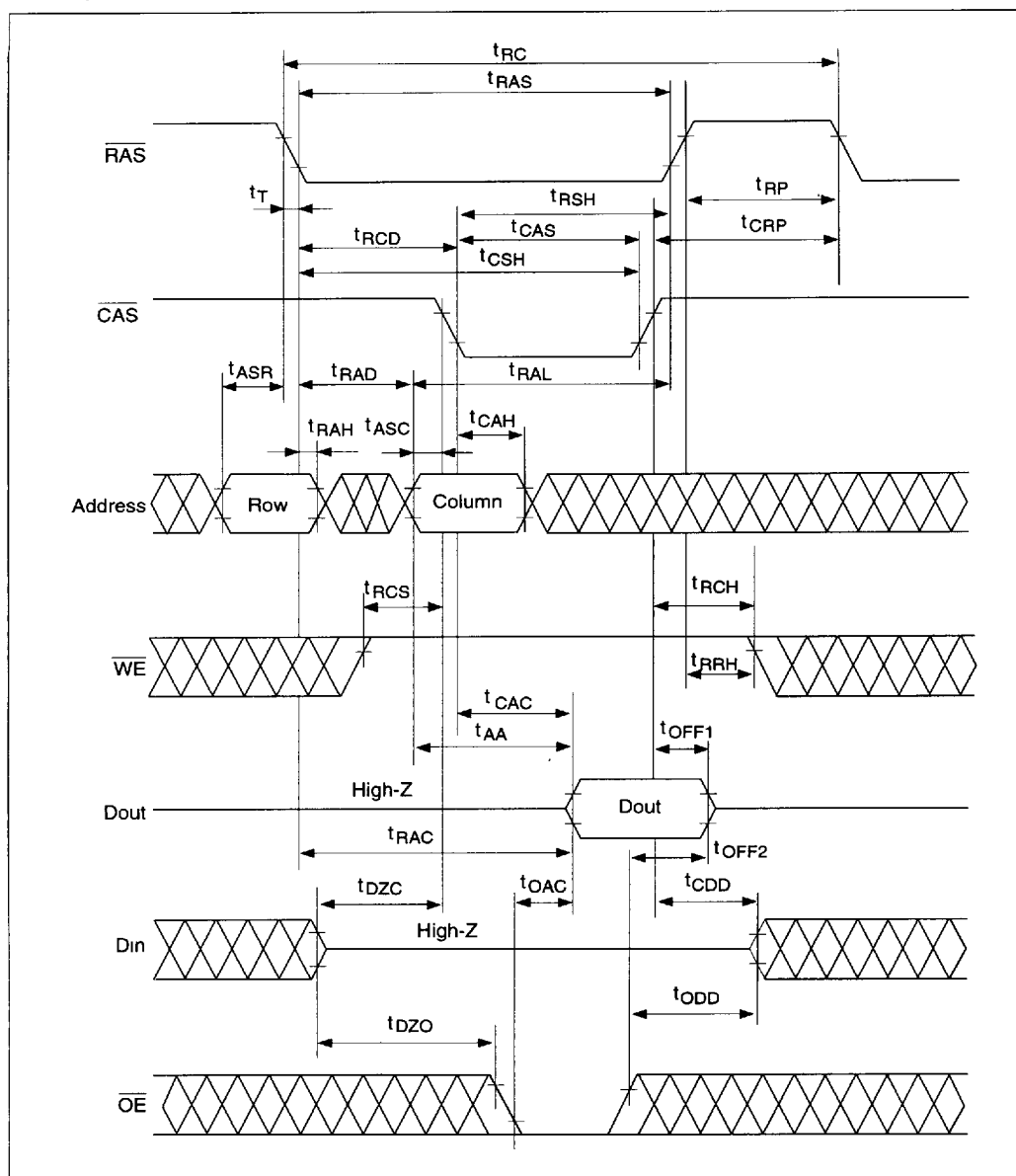
Self-refresh Mode

		HM51S4800C/CL							
		-6		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{\text{RAS}}$ pulse width (self-refresh)	t _{RASS}	100	—	100	—	100	—	μs	
$\overline{\text{RAS}}$ precharge time (self-refresh)	t _{RPS}	110	—	130	—	150	—	ns	
$\overline{\text{CAS}}$ hold time (self-refresh)	t _{CHS}	-50	—	-50	—	-50	—	ns	21

- Notes:
1. AC measurements assume $t_T = 5 \text{ ns}$.
 2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 4. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$.
 5. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \geq t_{RAD}(\text{max})$.
 6. $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
 7. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 8. Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
 9. Operation with the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RAD}(\text{max})$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
 10. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(\text{min})$, $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{AWD} \geq t_{AWD}(\text{min})$ and $t_{CPW} \geq t_{CPW}(\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 11. These parameters are referred to $\overline{\text{CAS}}$ leading edge in an early write cycle and to $\overline{\text{WE}}$ leading edge in a delayed write or a read-modify-write cycle.
 12. t_{RASC} defines $\overline{\text{RAS}}$ pulse width in fast page mode cycles.
 13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP} .
 14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh cycle or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles is required.
 15. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device.
 16. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 17. The supply voltage with all V_{CC} pins must be on the same level.
The supply voltage with all V_{SS} pins must be on the same level.
 18. Do not enable Dout buffer when using delayed write timing.
 19. If you use distributed CBR refresh mode with 15.6 μs interval in normal read/write cycle, CBR refresh should be executed within 15.6 μs immediately after exiting from and before entering into self refresh mode.
 20. If you use $\overline{\text{RAS}}$ only refresh or CBR burst refresh mode in normal read/write cycle, 1024 cycles of distributed CBR refresh with 15.6 μs interval should be executed within 16 ms immediately after exiting from and before entering into the self refresh mode.
 21. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.

Timing Waveforms *22

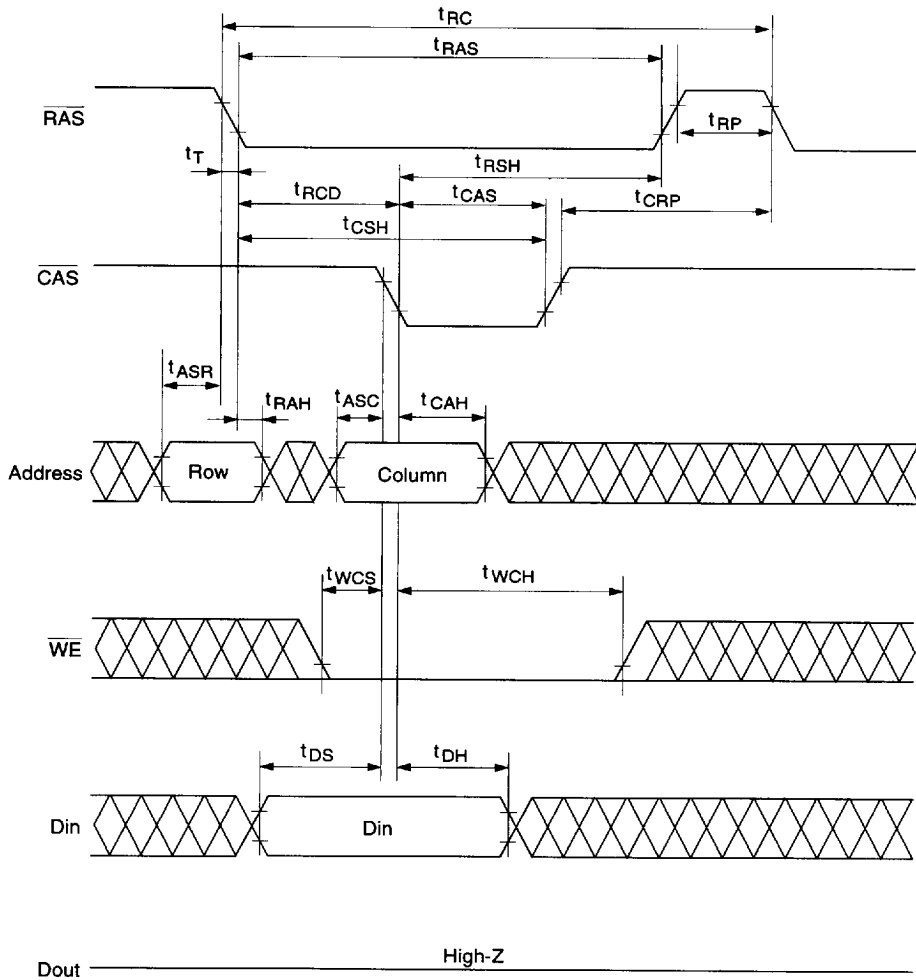
Read Cycle



Note: 22  H or L (H: $V_{\text{IH}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IH}}(\text{max})$, L: $V_{\text{IL}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IL}}(\text{max})$)

 Invalid Dout

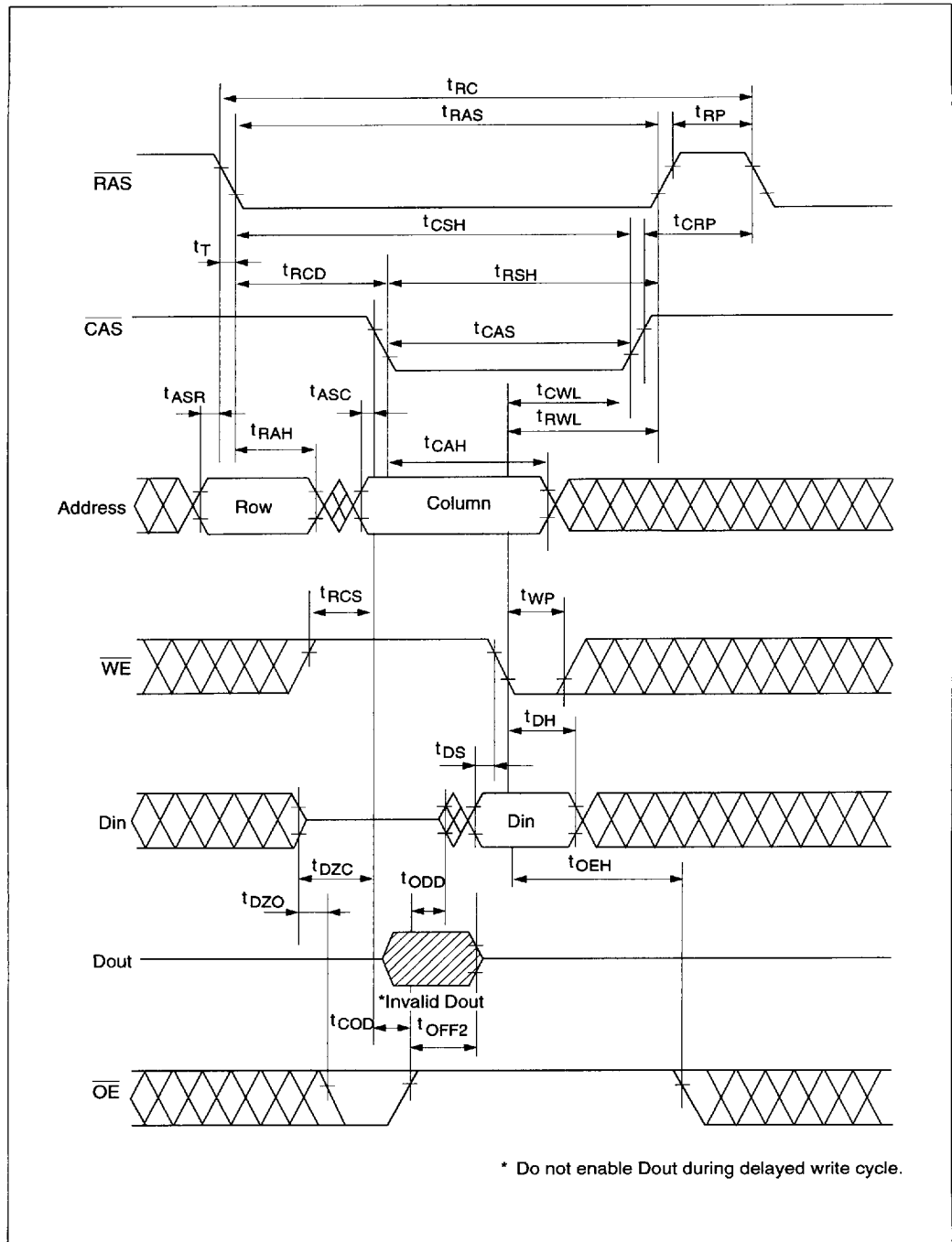
Early Write Cycle



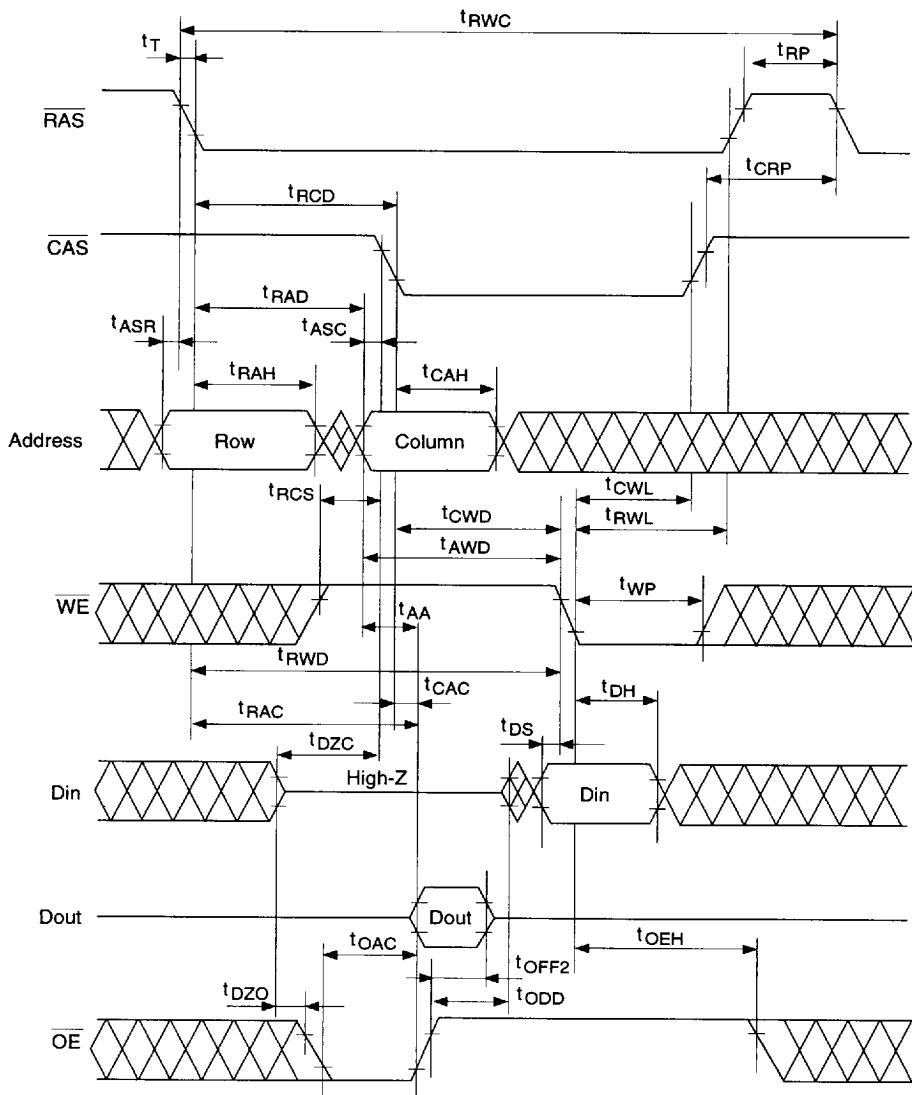
* $\overline{OE}$: V_{IH} or V_{IL}

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Delayed Write Cycle

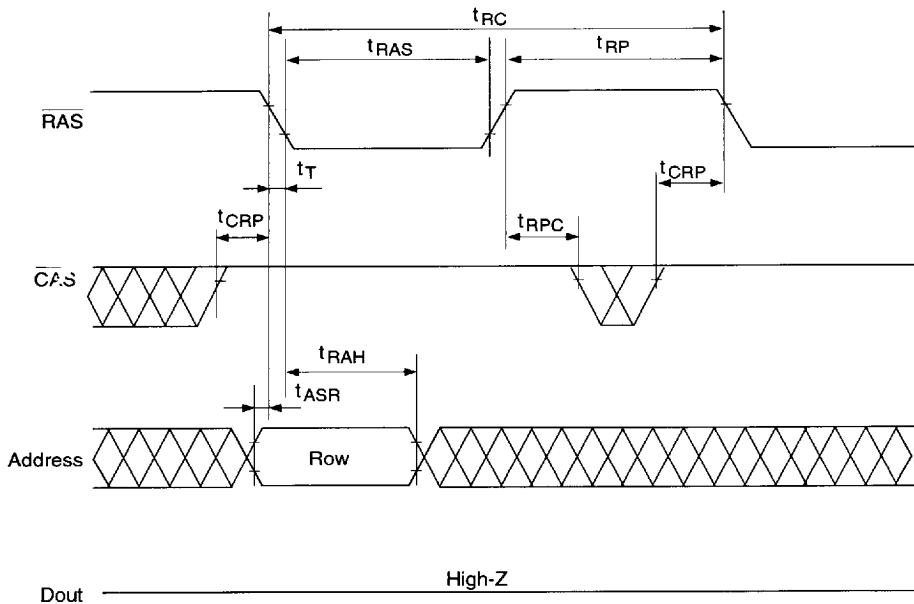


Read-Modify-Write Cycle



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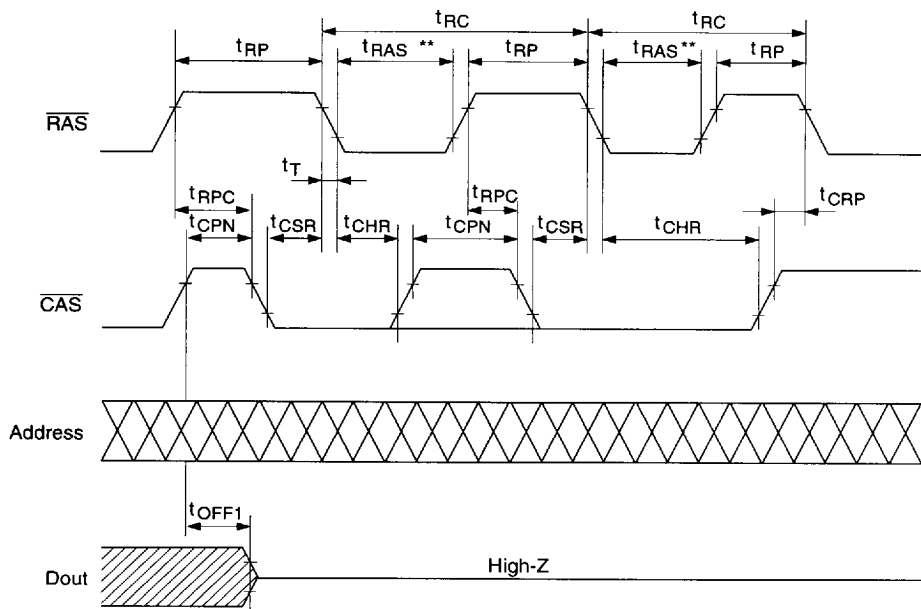
$\overline{\text{RAS}}$ -Only Refresh Cycle



* $\overline{\text{OE}}, \overline{\text{WE}}$: V_{IH} or V_{IL}

** Refresh address : A0 – A9 (AX0 – AX9)

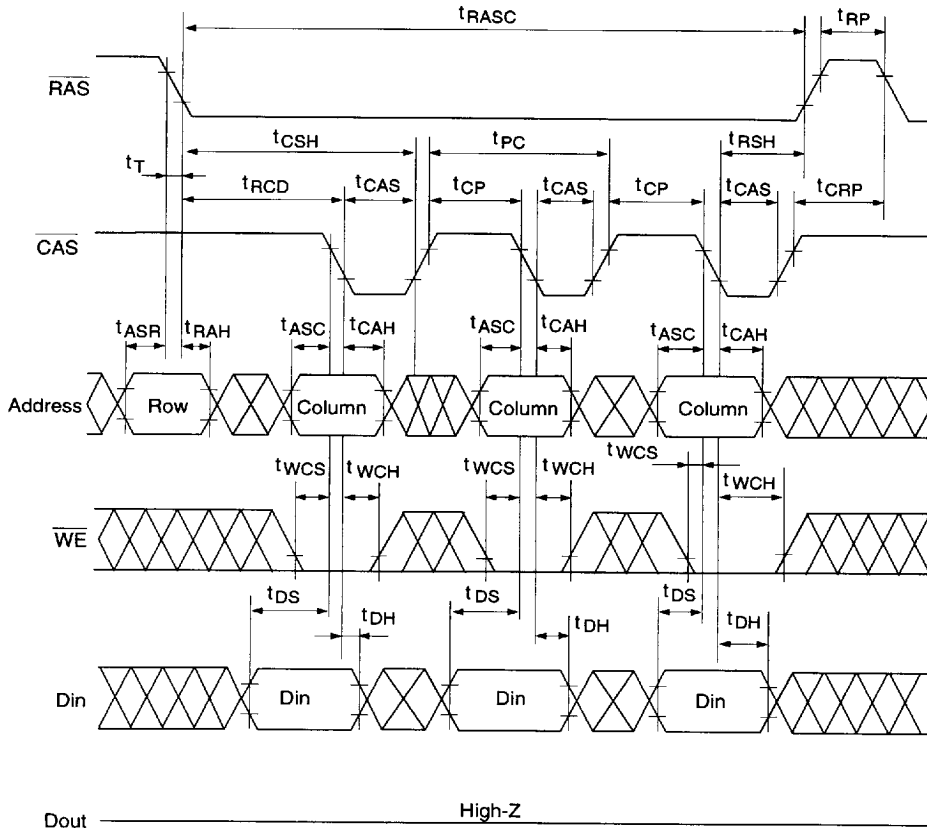
CAS-Before-RAS Refresh Cycle



* $\overline{\text{WE}}$: V_{IH} or V_{IL}

** Do not extend $t_{RAS} \geq t_{RAS}(\text{max})$.
Untested self refresh mode may be
activated and loss of data may be
resulted (HM514800C/CL).

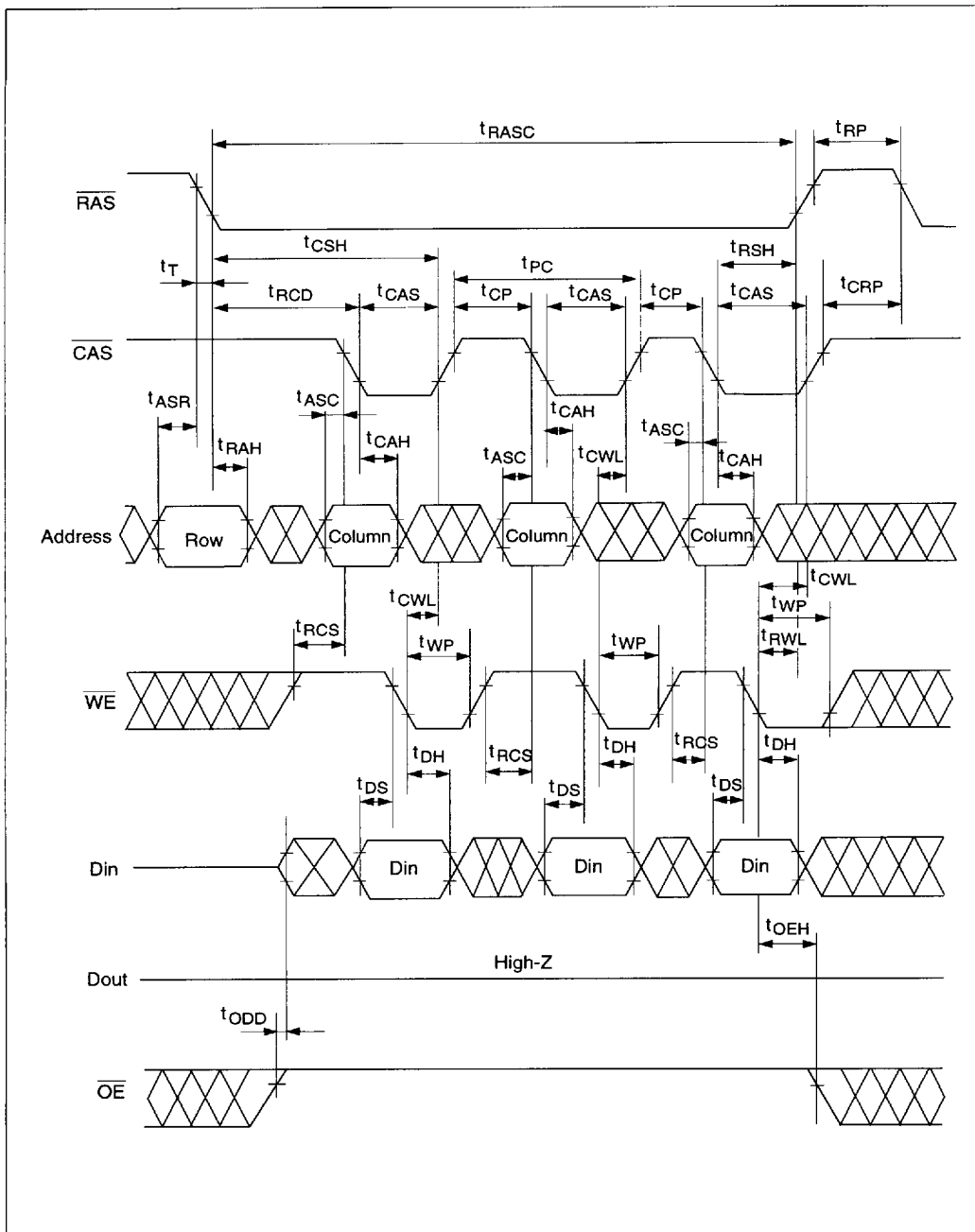
Fast Page Mode Early Write Cycle



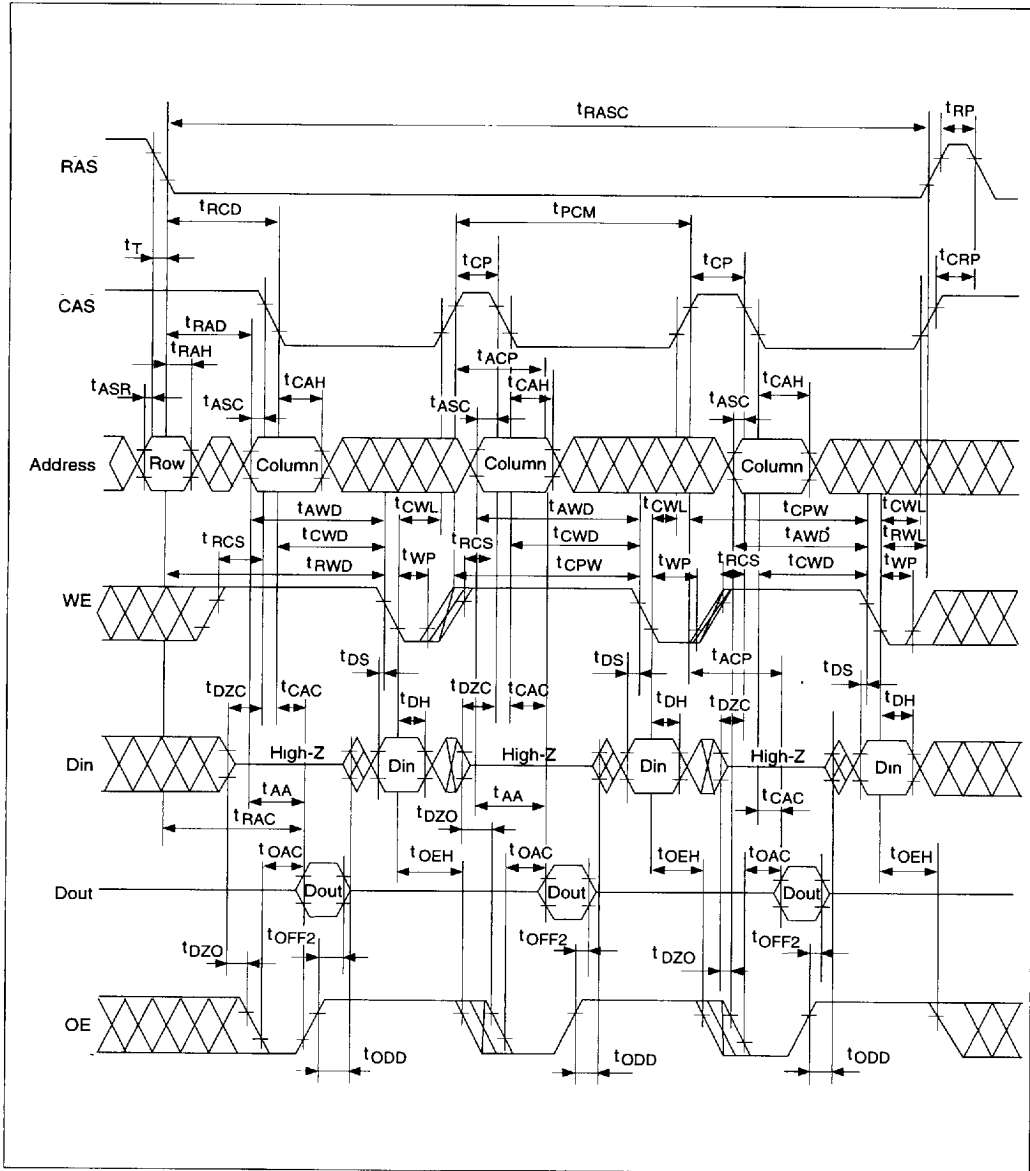
* OE : V_{IH} or V_{IL}

HM514800C/CL, HM51S4800C/CL Series

Fast Page Mode Delayed Write Cycle



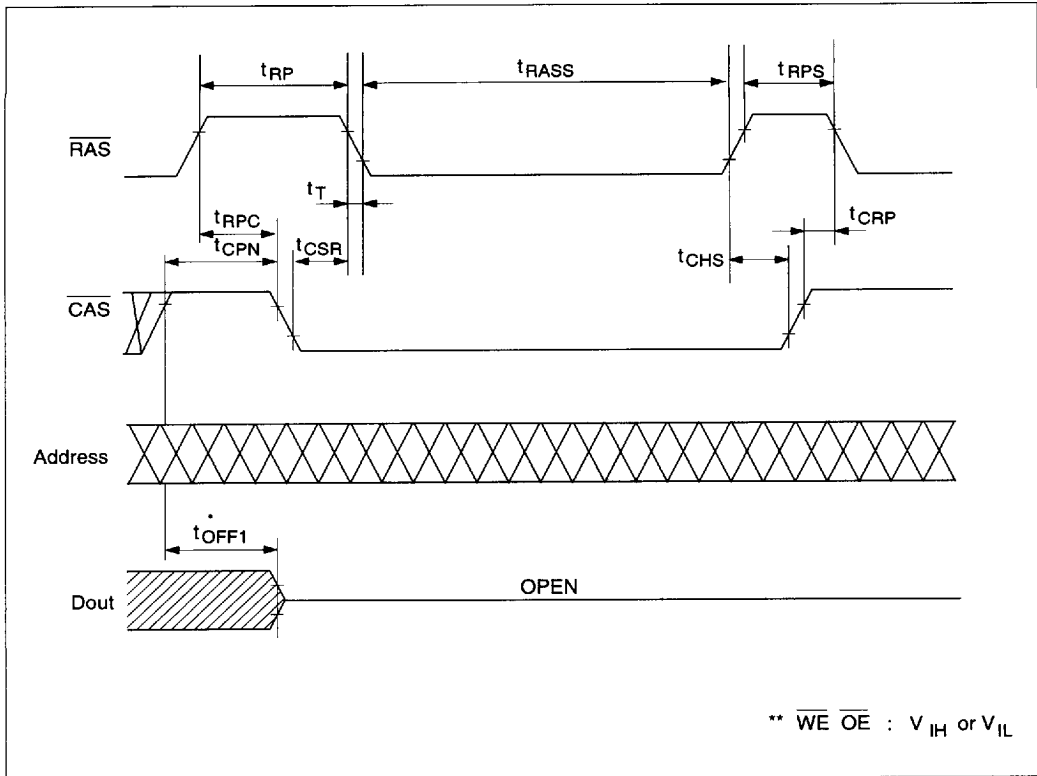
Fast Page Mode Read-Modify-Write Cycle



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Hitachi 287

Self Refresh Cycle



The low self refresh current is achieved by introducing extremely long internal refresh cycle. Therefore some care needs to be taken on the refresh.

1. Please do not use t_{RASS} timing, $10 \mu s \leq t_{RASS} \leq 100 \mu s$. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{RASS} \geq 100 \mu s$, then $\overline{RAS}$ precharge time should use t_{RPS} instead of t_{RP} .
2. If you use $\overline{RAS}$ only refresh or CBR burst refresh mode in normal read/write cycle, 1024 cycles of distributed CBR refresh with $15.6 \mu s$ interval should be executed within 16 ms immediately after exiting from and before entering into the self refresh mode.
3. If you use distributed CBR refresh mode with $15.6 \mu s$ interval in normal read/write cycle, CBR refresh should be executed within $15.6 \mu s$ immediately after exiting from and before entering into self refresh mode.
4. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.