

H7N0602LD, H7N0602LS, H7N0602LM

Silicon N Channel MOS FET
High Speed Power Switching

HITACHI

ADE-208-1526C (Z)

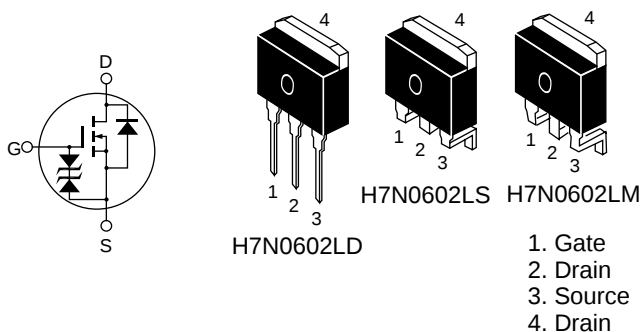
4th. Edition
May 2002

Features

- Low on-resistance
 $R_{DS(on)} = 4.1 \text{ m}\Omega$ typ.
- 4.5 V gate drive devices
- High Speed Switching

Outline

LDPAK



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	85	A
Drain peak current	I_D (pulse) ^{Note1}	340	A
Body-drain diode reverse drain current	I_{DR}	85	A
Avalanche current	I_{AP} ^{Note3}	65	A
Avalanche energy	E_{AR} ^{Note3}	362	mJ
Channel dissipation	Pch ^{Note2}	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$
2. Value at Tc = 25°C
3. Value at Tch = 25°C, Rg $\geq 50 \Omega$

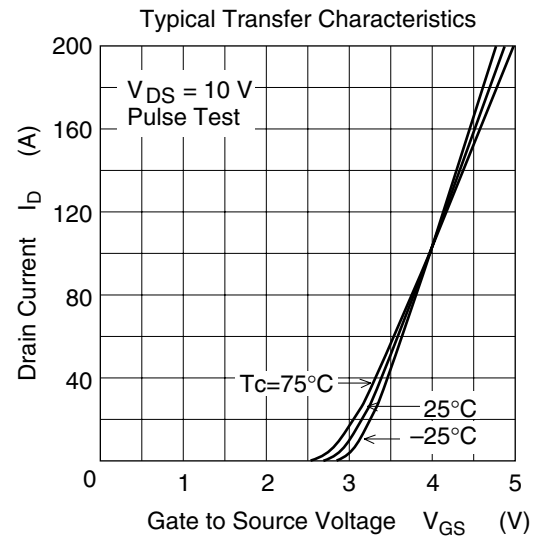
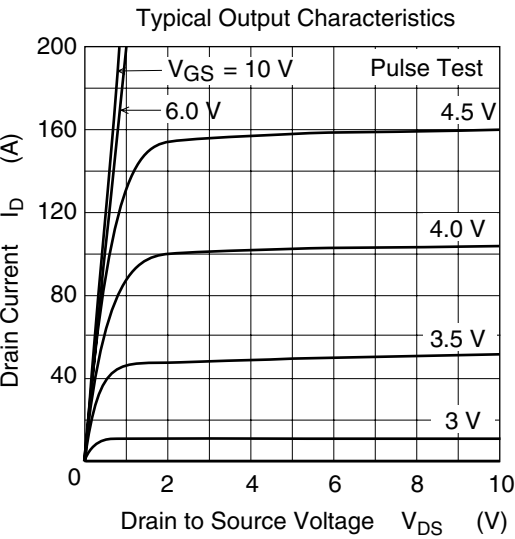
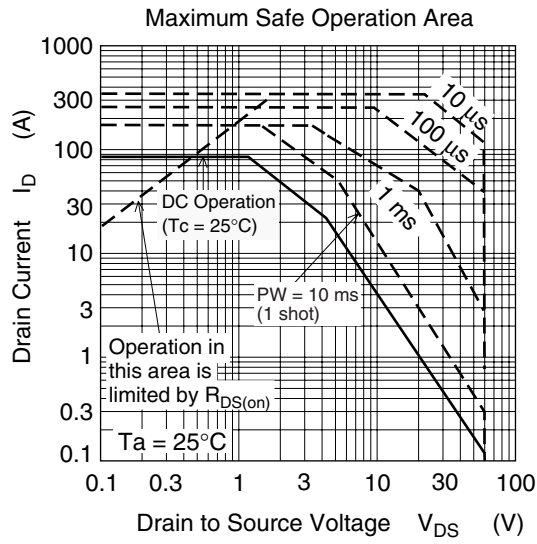
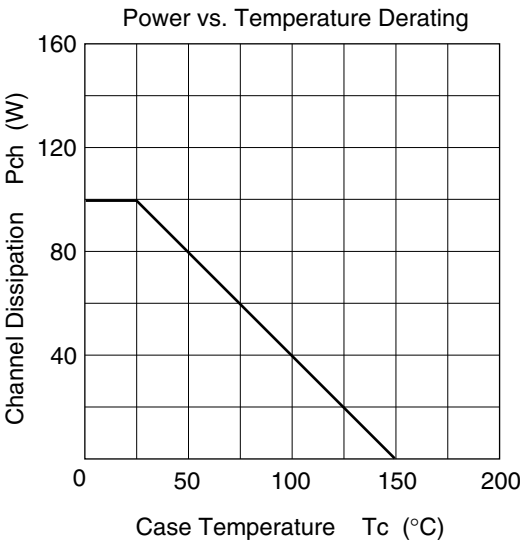
Electrical Characteristics

(Ta = 25°C)

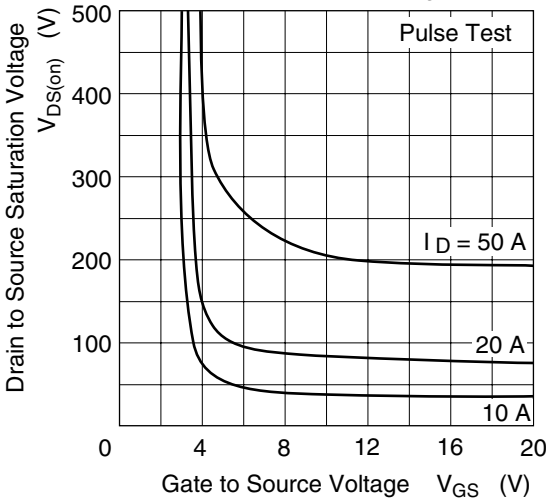
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 60 \text{ V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.5	—	2.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$ ^{Note 1}
Forward transfer admittance	$ y_{fs} $	70	120	—	S	$I_D = 45 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note 1}
Static drain to source on state resistance	$R_{DS(on)}$	—	4.1	5.2	m Ω	$I_D = 45 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note 1}
Static drain to source on state resistance	$R_{DS(on)}$	—	6.2	9.0	m Ω	$I_D = 45 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note 1}
Input capacitance	Ciss	—	9000	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	Coss	—	1000	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	470	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Qg	—	140	—	nc	$V_{DD} = 25 \text{ V}$
Gate to source charge	Qgs	—	30	—	nc	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Qgd	—	30	—	nc	$I_D = 85 \text{ A}$
Turn-on delay time	td(on)	—	55	—	ns	$V_{GS} = 10 \text{ V}$
Rise time	tr	—	290	—	ns	$I_D = 45 \text{ A}$
Turn-off delay time	td(off)	—	140	—	ns	$R_L = 0.67 \text{ }\Omega$
Fall time	tf	—	50	—	ns	$R_g = 4.7 \text{ }\Omega$
Body-drain diode forward voltage	V_{DF}	—	0.95	—	V	$I_F = 85 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	trr	—	45	—	ns	$I_F = 85 \text{ A}$, $V_{GS} = 0$ $diF/dt = 100 \text{ A}/\mu\text{s}$

Notes: 1. Pulse test

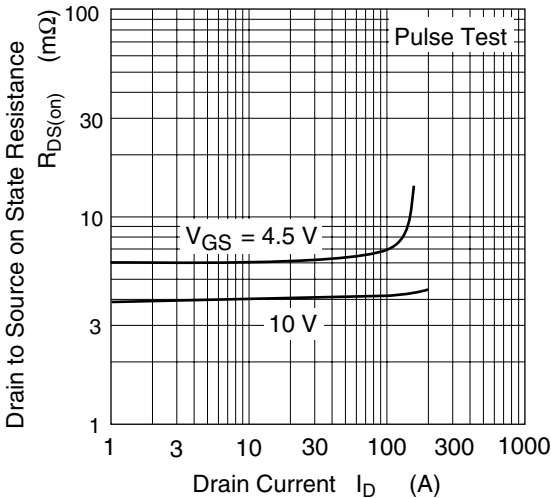
Main Characteristics



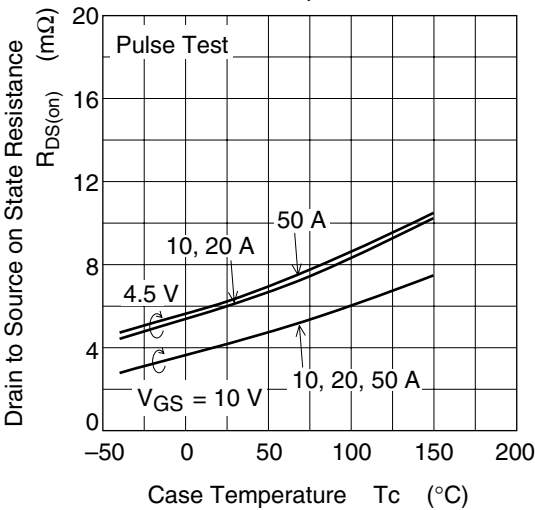
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



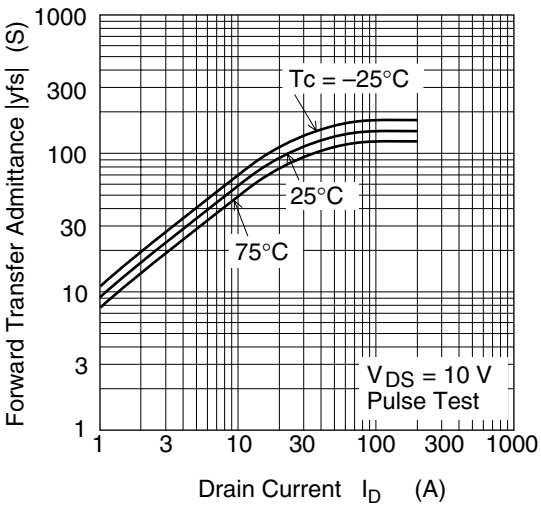
Static Drain to Source on State Resistance
vs. Drain Current

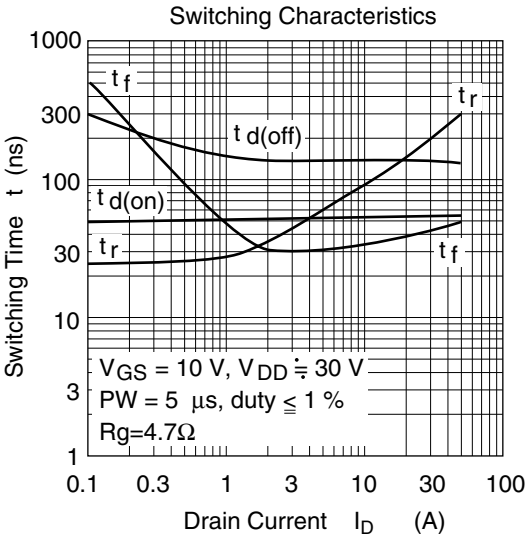
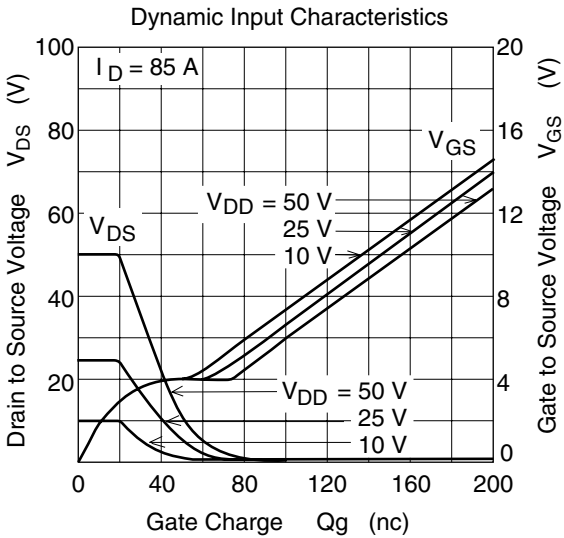
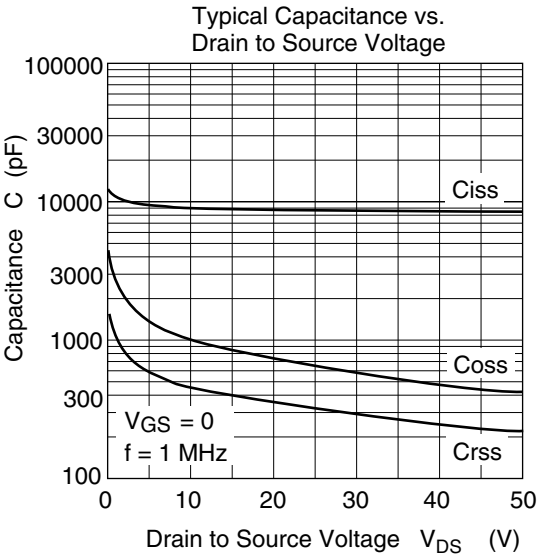
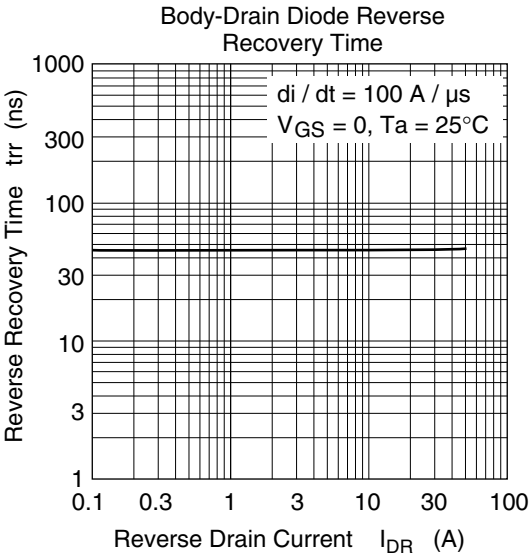


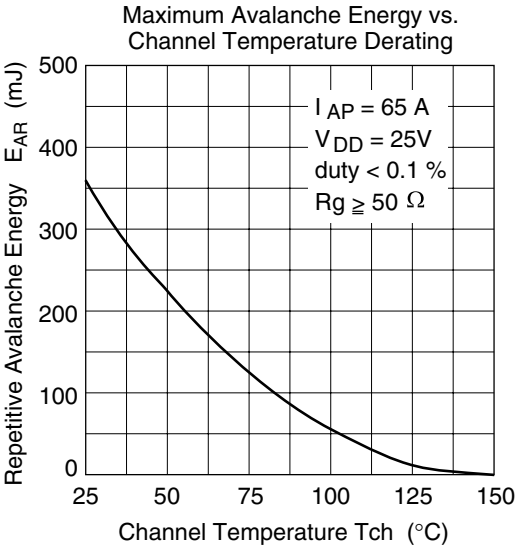
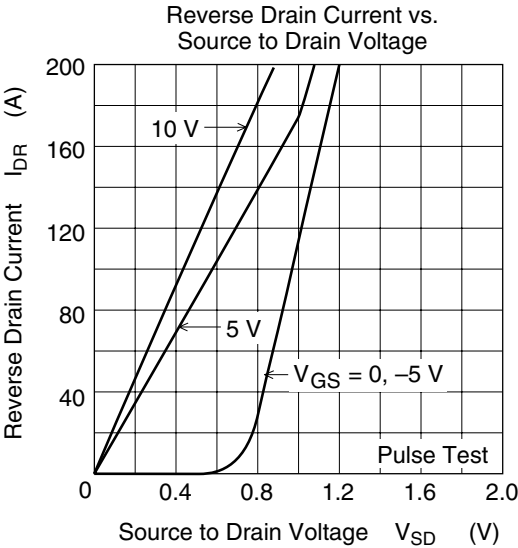
Static Drain to Source on State Resistance
vs. Temperature



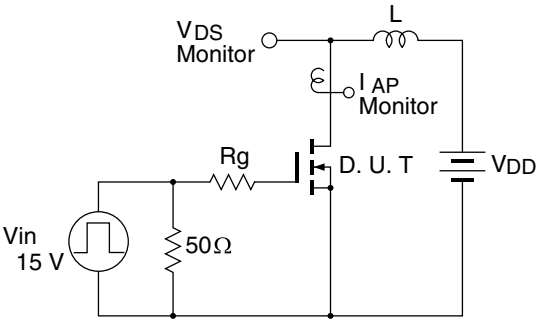
Forward Transfer Admittance vs.
Drain Current





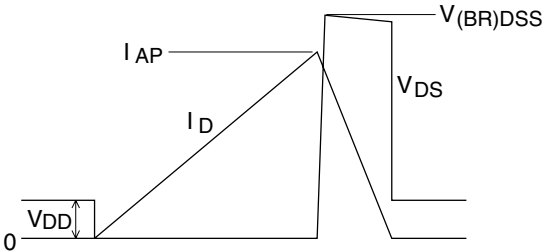


Avalanche Test Circuit

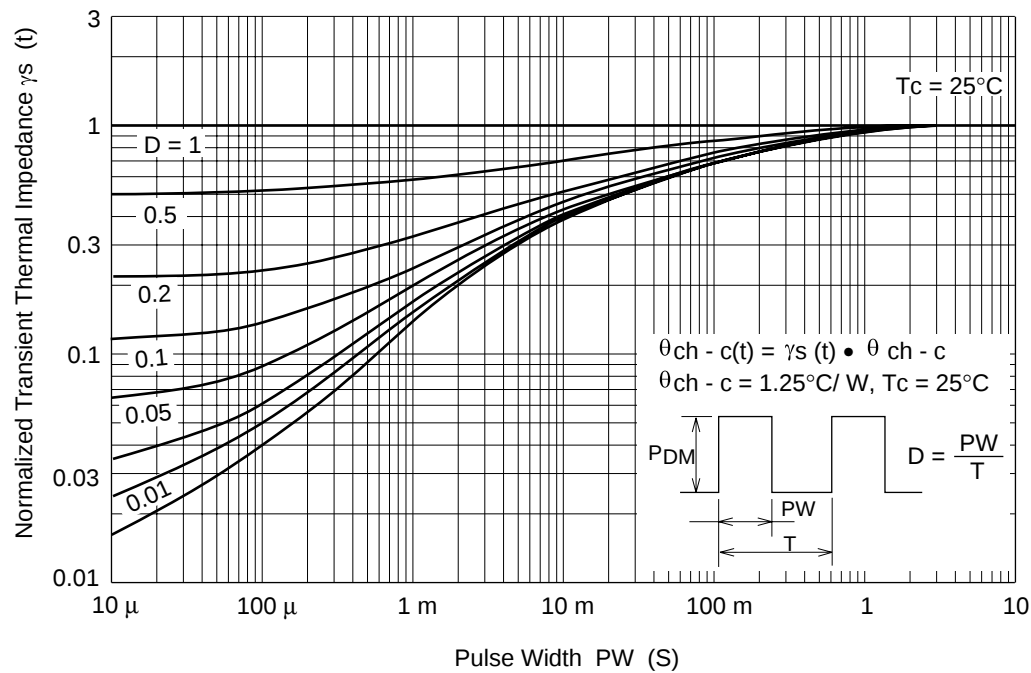


Avalanche Waveform

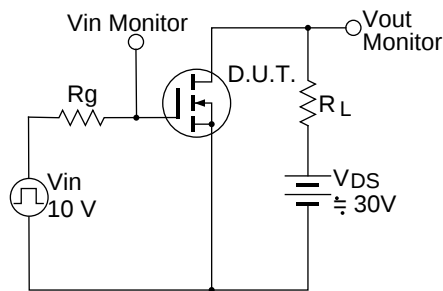
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



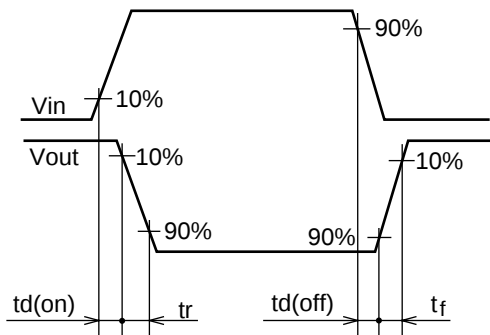
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit

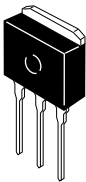
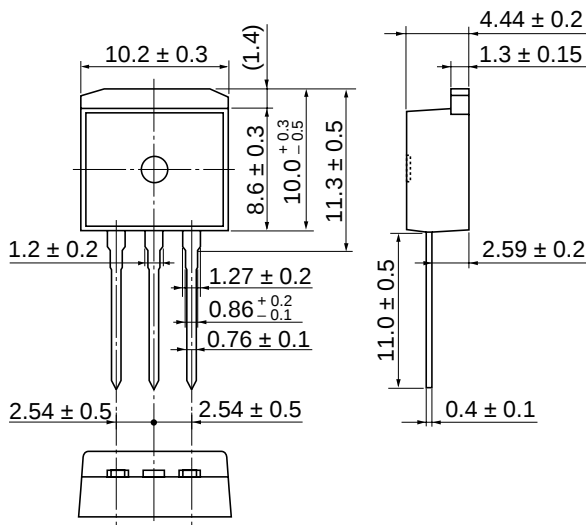


Waveform



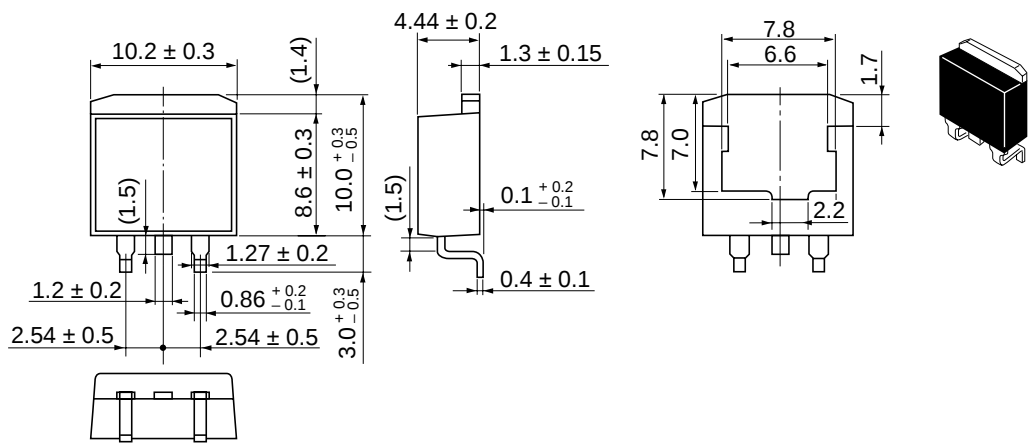
Package Dimensions

As of January, 2002
Unit: mm



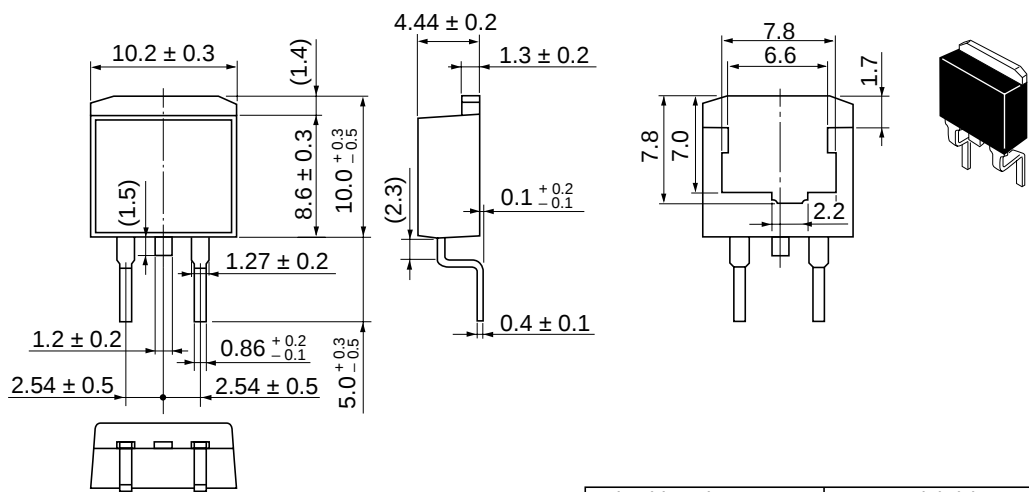
Hitachi Code	LDPAK (L)
JEDEC	—
JEITA	—
Mass (reference value)	1.4 g

As of January, 2002
Unit: mm



Hitachi Code	LDBAK (S)-(1)
JEDEC	—
JEITA	—
Mass (reference value)	1.3 g

As of January, 2002
Unit: mm



Hitachi Code	LDBAK (S)-(2)
JEDEC	—
JEITA	—
Mass (reference value)	1.35 g

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Hitachi, Ltd.

Semiconductor & Integrated Circuits
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 Tel: (03) 3270-2111 Fax: (03) 3270-5109

URL <http://www.hitachisemiconductor.com/>

For further information write to:

Hitachi Semiconductor (America) Inc.
 179 East Tasman Drive
 San Jose, CA 95134
 Tel: <1> (408) 433-1990
 Fax: <1> (408) 433-0223

Hitachi Europe Ltd.
 Electronic Components Group
 Whitebrook Park
 Lower Cookham Road
 Maidenhead
 Berkshire SL6 8YA, United Kingdom
 Tel: <44> (1628) 585000
 Fax: <44> (1628) 585200

Hitachi Europe GmbH
 Electronic Components Group
 Dornacher Straße 3
 D-85622 Feldkirchen
 Postfach 201, D-85619 Feldkirchen
 Germany
 Tel: <49> (89) 9 9180-0
 Fax: <49> (89) 9 29 30 00

Hitachi Asia Ltd.
 Hitachi Tower
 16 Collyer Quay #20-00
 Singapore 049318
 Tel: <65>-6538-6533/6538-8577
 Fax: <65>-6538-6933/6538-3877
 URL: <http://semiconductor.hitachi.com.sg>

Hitachi Asia Ltd.
 (Taipei Branch Office)
 4/F, No. 167, Tun Hwa North Road
 Hung-Kuo Building
 Taipei (105), Taiwan
 Tel: <886>-(2)-2718-3666
 Fax: <886>-(2)-2718-8180
 Telex: 23222 HAS-TP
 URL: <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.
 Group III (Electronic Components)
 7/F., North Tower
 World Finance Centre,
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 Tsim Sha Tsui, Kowloon Hong Kong
 Tel: <852>-2735-9218
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