MICROTECH

T-46-13-01

BS9000 Approved product list

Memory

Part Nº	Package style	BS Spec. Nº	Functional Description
MS6116-2	24 PIN DIL	BS9400 G0085	2k x 8 SRAM
MS29653	18 PIN DIL	BS9400 G0112	2k x 4 Power Switched PROM
MS29673	24 PIN DIL	BS9400 G0084	4k x 8 Power Switched PROM
	or		
MS29683	24 PIN DIL SKINNY	BS9400 G0113	2k x 8 Power Switched PROM
MS27C256	28 PIN DIL	BS9400 G0126	32k x 8 UV Eraseable PROM
	or		
MS28C256	32 PIN LCC	BS9400 G0127	32k x 8 E^2PROM

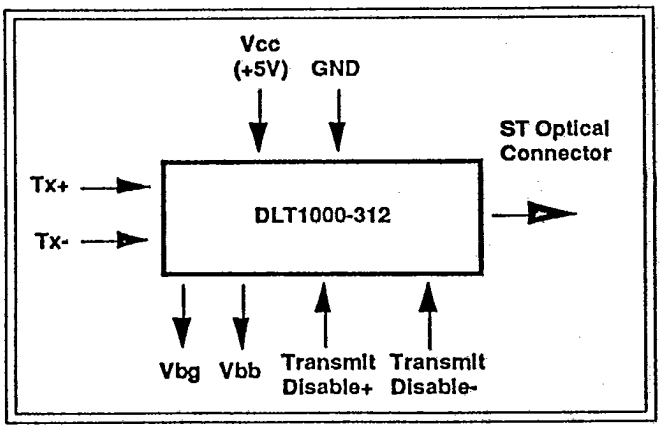
Available end of 1st quarter 1991

µT58128	32 PIN DIL 32 PIN LCC 32 PIN Flat Pack	BS9400 G0179	128k x 8-Bit CMOS SRAM
µT6832	28 PIN DIL 32 PIN LCC	BS9400 G0178	32k x 8-Bit CMOS SRAM
µT8U128	66PGA	BS9400 G0180	32k x 32-Bit UV EPROM module

BS/CECC PRODUCT

T-41-91

DLT1000-312

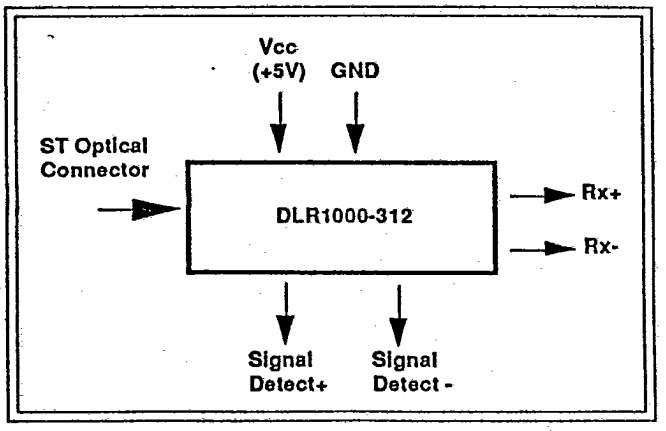


The **DLT1000-312 Data Link Transmitter** converts serial data signals to lightwaves in the 1300 nanometer band. It is capable of data rates from **DC to 312.5 Mbits/sec.** A single nominal +5-volt power supply is required. The DLT1000-312 directly interfaces with pseudo-ECL (Vcc = +5V), TTL, or CMOS. Data and Transmit_Disable signals are received through complementary differential inputs to comparators. Logical 1 to transmit data (Tx+, Tx–) results in high optical output. Logic 1 to Transmit_Disable disables the transmitter.

Output biases Vbb and Vbg are available for setting the Data or Transmit_Disable comparator switching level. For example, to control Transmit_Disable with a TTL signal, connect Transmit_Disable - to Vbg and input the TTL transmit disable signal to Transmit_Disable +. To hardwire enable the DLT1000-312 connect Transmit_Disable- to Vbb, and Transmit_Disable+ to Vbg.

The InGaAsP/InP **very-high-speed ELED** is fabricated by the Metal-Organic Vapor Phase Epitaxy (MOVPE) process for high reliability, performance, and consistency.

DLR1000-312



The **DLR1000-312 Data Link Receiver** converts lightwaves in the 1300 nanometer band to serial pseudo - ECL signals. Data rates from **10 to 312.5 Mbits/second** can be used. A single nominal +5-volt power supply is required.

Data and Signal_Detect signals come from complementary, pseudo - ECL outputs. In the logic 1 state, the positive output is high and the negative output low; in the logic 0 state, the positive output is low and the negative output high.

Signal_Detect is an optical power alarm. The optical signal intensity is sufficient for conversion when Signal_Detect is logic 1; when it is too weak for conversion, Signal_Detect is logic 0. If not used, the Signal_Detect output(s) can be left unconnected.

The InGaAs/InP high-performance **Planar PIN photodiode** is manufactured by the MOVPE process for high reliability and product consistency.

BT&D

T-41-91

DLT1000 - 312 Transmitter

ABSOLUTE LIMITING RATINGS

PARAMETER	MIN	MAX	UNITS
Power Supply Voltage (Vcc or Vee)	0	6	V
Input Voltage	Vee	Vcc	V
Output Current (Vbb and Vbg)	–1	1	mA
Operating Temperature in Free Air	0	+70	°C
Storage Temperature	–20	+85	°C
Relative Humidity	—	non-condensing	%RH
Soldering Temperature	—	240/10	°C/secs

PERFORMANCE SPECIFICATIONS[1]

PARAMETER	MIN	TYP	MAX	UNITS
Center Wavelength	1270	1320	1370	nm
Spectral Width (FWHM)	—	80	110	nm
Optical Output Power (average 50% duty cycle into 62.5 µm core; 0.275 NA fiber)	–19 (12.5)	–16 (25)	–14 (40)	dBm (µW)
Optical Rise and Fall Time (10%-90%/90%-10%)	—	1.5	2.5	ns
Duty Cycle Distortion (peak)[2]	—	—	0.6	ns
Extinguished Optical Output Power[3]	—	<1	—	nW
Differential Input to Switch Optical Output	—	100	—	mV
High Level Input Current	—	50	—	µA
Transmit_Disable Response Time	—	100	—	ns
Output Voltage at Vbb with Respect to Vcc	—	–1.3	—	V
Output Voltage at Vbg with Respect to Vee	—	1.3	—	V
Operating Power Supply Voltage	4.5	5.0	5.7	V
Current Consumption[4]	—	120	170	mA

1. Through specified operating conditions.
2. With 156.25 MHz square wave input.
3. With Logical 0 data input, or Logical 1 Transmit_Disable input
4. Typical consumption figure is at 25°C. Maximum consumption is at 70°C.

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DLR1000-312 Receiver

ABSOLUTE LIMITING RATINGS

PARAMETER	MIN	MAX	UNITS
Power Supply Voltage (Vcc or Vee)	0	6	V
Optical Input Power	—	1	mW
Output Current (any output)	0	30	mA
Operating Temperature in Free Air	0	+70	°C
Storage Temperature	–20	+85	°C
Relative Humidity	—	non-condensing	%RH
Soldering Temperature	—	240/10	°C/secs

PERFORMANCE SPECIFICATIONS[1]

PARAMETER	MIN	TYP	MAX	UNITS
Optical Input Center Wavelength	1270	—	1380	nm
Sensitivity for 2 : 5E -10 BER at 312.5 Mbaud[2,3,7]	—	–28 (1.6)	–26 (2.5)	dBm (µW)
Maximum Operating Optical Input Power[2,7]	–14 (40)	—	—	dBm (µW)
Signal Detect must Assert Input Power	—	—	–31	dBm
Signal_Detect Hysteresis	—	2	—	dB
Signal_Detect Assertion Time	—	70	—	µs
Signal_Detect De-assertion Time	—	300	—	µs
Rx+ and Rx– Output Rise and Fall Times	—	1	1.5	ns
Output High Voltage with Respect to Vcc[4]	–1.0	—	–0.7	V
Output Low Voltage with Respect to Vcc[4]	–2.0	—	–1.6	V
Operating Power Supply Voltage	4.5	5.0	5.7	V
Current Consumption[5,6]	—	80	120	mA

1. Through specified operating conditions.
2. With 2^{15}—1 PRBS Test Pattern, both receiver data outputs PECL terminated.
3. At center of eye.
4. All outputs are 10KH ECL, but with Vee grounded, and Vcc +5V nominal (so called Pseudo-ECL, PECL).
5. Typical consumption figure is at 25°C. Maximum consumption is at 70°C.
6. Excludes current drawn from output loads.
7. Average optical input power from 62.5 µm core; 0.275 NA fiber.

BER = Bit Error Rate In Errors per Bit.
Rx+ and Rx- outputs must be similarly terminated.

T-46-19-13

MICROTECH

Programmable Logic Devices (cont'd)

Part Nº	Package style	BS Spec. Nº	Functional Description
PAL16R4D	20 PIN DIL	BS9493 F0222	Quad 16 Input registered and/or Gate Array
PAL20RS8	24 PIN DIL	BS9493 F0057	Octal 20 Input Registered and/or Gate Array with product term sharing
PAL20L8A	24 PIN DIL	BS9493 F0060	Octal 20 Input and/or-Invert Gate Array
PAL20L8A-2	24 PIN DIL	BS9493 F0058	Octal 20 Input and/or-Invert Gate Array
PAL20L8B	24 PIN DIL	BS9493 F0059	Octal 20 Input and/or-Invert Gate Array
PAL20R8A-2	24 PIN DIL	BS9493 F0048	Octal 20 Input registered and/or Gate Array
PAL20R8B	24 PIN DIL	BS9493 F0049	Octal 20 Input registered and/or Gate Array
PAL20R6A-2	24 PIN DIL	BS9493 F0227	Hex 20 Input registered and/or Gate Array
PAL20R6B	24 PIN DIL	BS9493 F0228	Hex 20 Input registered and/or Gate Array
PAL20R4A	24 PIN DIL	BS9493 F0063	Quad 20 Input registered and/or Gate Array
PAL20R4A-2	24 PIN DIL	BS9493 F0061	Quad 20 Input registered and/or Gate Array
PAL20R4B	24 PIN DIL	BS9493 F0062	Quad 20 Input registered and/or Gate Array
PAL20L10	24 PIN DIL	BS9493 F0262	Deca 20 Input and/or-Invert Gate Array
PAL20RA10	24 PIN DIL	BS9493 F0263	Deca 20 Input registered Async and/or gate array
PAL20S10	24 PIN DIL	BS9493 F0264	Deca 20 Input and/or Gate Array with Product term sharing
PAL20X4	24 PIN DIL	BS9493 F0265	Quad 20 Input registered and-or -xor Gate Array
PAL20X8	24 PIN DIL	BS9493 F0266	Octal 20 Input registered and-or -xor Gate Array
PAL20X10	24 PIN DIL	BS9493 F0267	Deca 20 Input registered and-or -xor Gate Array
PAL22V10	24 PIN DIL	BS9493 F0268	Deca Macrocell 22 Input and-or Gate Array

BS/CECC PRODUCT

T-41-91

Ordering Information:

Please order part number **DLT1000-312/DLR1000-312.**
To place an order or obtain more information, contact:

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Handling Precautions:

Normal handling precautions for electrostatic-sensitive devices should be taken.