T-46-23-14

CYM1836

CYPRESS SEMICONDUCTOR

128K x 32 Static RAM Module

Features

- High-density 4-megabit SRAM module
- High-speed CMOS SRAMs
  - Access time of 20 ns
- Low active power
  - 2.6W (max.) at 20 ns
- SMD technology
- TTL-compatible inputs and outputs
- Low profile
  - Max. height of .57 in.
- JEDEC-compatible pinout
- Small PCB footprint
  - 0.78 sq. in.
- Available in SIMM, ZIP, or PLCC format

Functional Description

The CYM1836 is a high-performance 4-megabit static RAM module organized as 128K words by 32 bits. This module is constructed from four 128K x 8 SRAMs in SOJ packages mounted on an epoxy laminate board with pins. Four chip selects ($\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$, $\overline{CS}_4$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

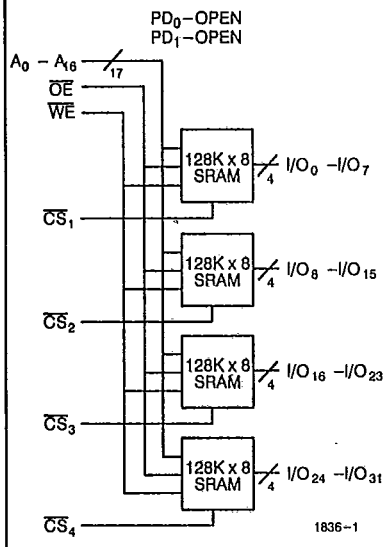
Writing to each byte is accomplished when the appropriate chip select ($\overline{CS}_N$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O_X) is written into the memory location specified on the address pins (A_0 through A_{16}).

Reading the device is accomplished by taking the chip select ($\overline{CS}_N$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O_X).

The data input/output pins stay at the high-impedance state when write enable is LOW or the appropriate chip selects are HIGH.

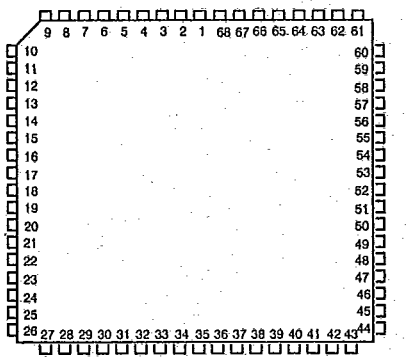
Two pins (PD_0 and PD_1) are used to identify module memory density in applications where alternate versions of the JEDEC-standard modules can be interchanged.

Logic Block Diagram

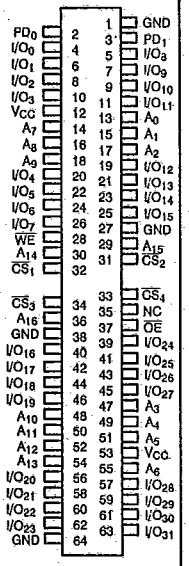


Pin Configurations

PLCC
Top View



ZIP/SIMM
Top View



Selection Guide

	1836–20	1836–25	1836–30	1836–35	1836–45
Maximum Access Time (ns)	20	25	30	35	45
Maximum Operating Current (mA)	480	480	480	480	480
Maximum Standby Current (mA)	100	100	100	100	100

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... −10°C to +85°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM1836		Units
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		−0.5	0.8	V
I_{IX}	Input Load Current	$GND \le V_I \le V_{CC}$	−20	+20	µA
I_{OZ}	Output Leakage Current	$GND \le V_O \le V_{CC}$, Output Disabled	−20	+20	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = mA, $\overline{CS}_N \le V_{IL}$		480	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}_N \ge V_{IH}$, Min. Duty Cycle = 100%		100	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}_N \ge V_{CC}$ − 0.2V, $V_{IN} \ge V_{CC}$ − 0.2V, or $V_{IN} \le 0.2V$		28	mA

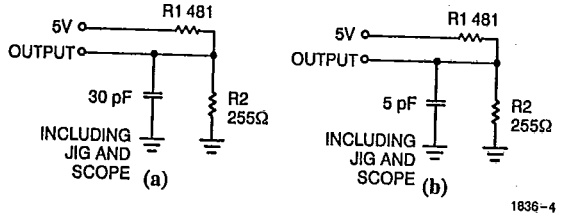
Capacitance[2]

Parameters	Description	Test Conditions	Typ.	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	33	40	pF
C_{OUT}	Output Capacitance		12	15	pF

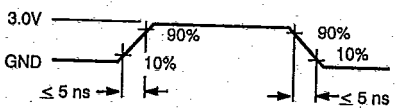
Notes:

1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

AC Test Loads and Waveforms

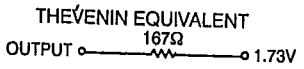


1836-4



1836-5

Equivalent to: THEVENIN EQUIVALENT



MODULES

Switching Characteristics Over the Operating Range[3]

Parameters	Description	1836–20		1836–25		1836–30		1836–35		1836–45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	20		25		30		35		45		ns
t_{AA}	Address to Data Valid		20		25		30		35		45	ns
t_{OHA}	Output Hold from Address Change	5		5		5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		20		25		30		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		8		8		10		12		15	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		8		10		11		12		15	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	3		3		3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		10		10		13		15		18	ns
WRITE CYCLE[6]												
t_{WC}	Write Cycle Time	20		25		30		35		45		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	15		15		18		20		25		ns
t_{AW}	Address Set-Up to Write End	15		15		18		20		25		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		15		18		20		25		ns
t_{SD}	Data Set-Up to Write End	10		10		13		15		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[4]	0		0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4, 5]	0	8	0	10	0	15	0	15	0	18	ns

Shaded areas contain preliminary information.

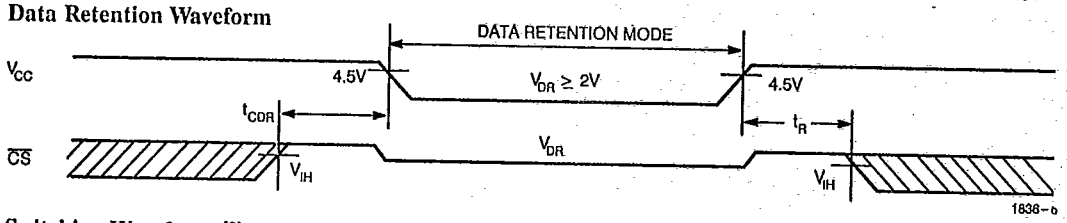
Data Retention Characteristics Over the Operating Range (L Version Only)

Parameters	Description	Test Conditions	1836		Units
			Min.	Max.	
V_{DR}	V_{CC} for Retention Data	$V_{CC} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$, or $V_{IN} \leq 0.2V$	2.0		V
I_{CCDR}	Data Retention Current			2	mA
t_{CDR}[7]	Chip Deselect to Data Retention Time		0		ns
t_R[7]	Operation Recovery Time		t_{RC}		ns

Notes:

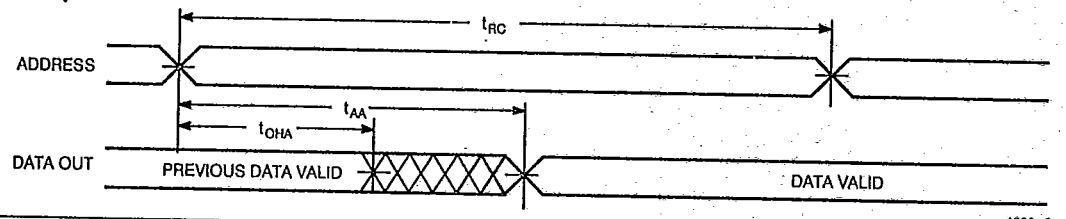
3. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
7. Guaranteed, not tested.

Data Retention Waveform

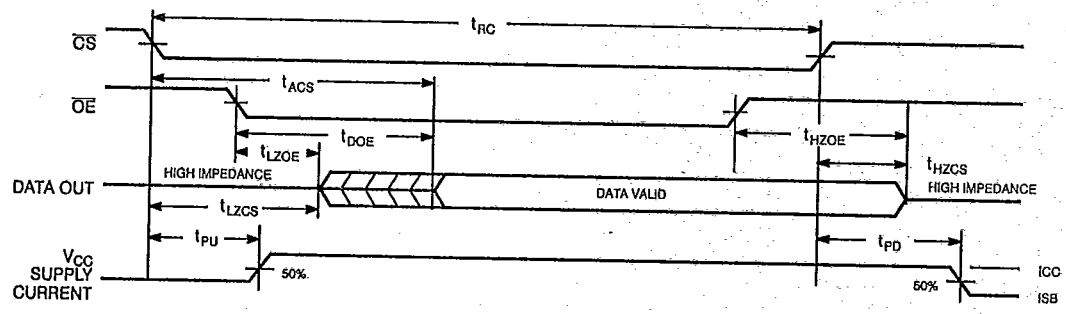


Switching Waveforms[8]

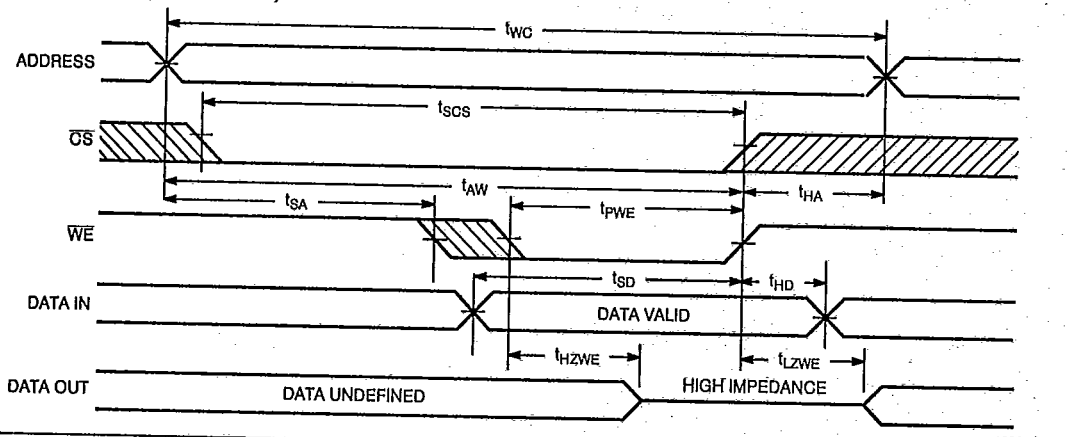
Read Cycle No. 1[9, 10]



Read Cycle No. 2[9, 11]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[6]



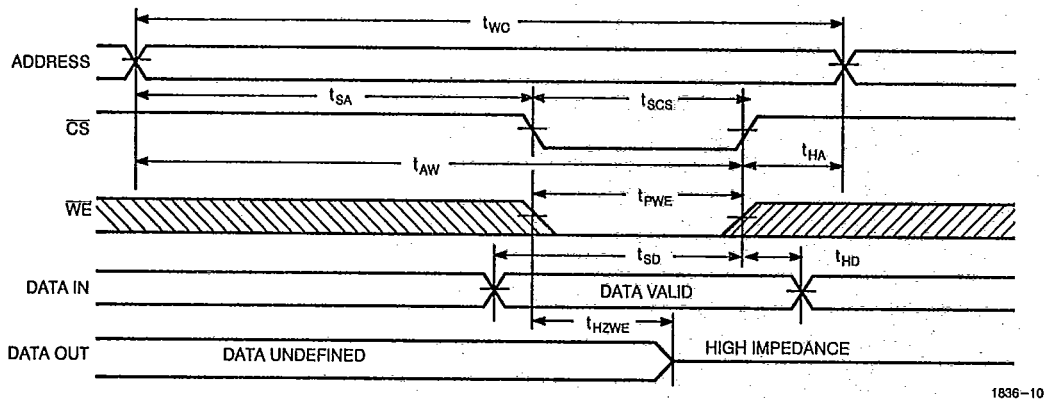
Notes:

8. $\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$, and $\overline{CS}_4$ are represented by $\overline{CS}$ in the Switching Characteristics and Switching Waveforms sections.
9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.
11. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

MODULES

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[6, 12]



Notes:
12. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}_N$	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CYM1836PJ–20C	PJ02	Commercial
	CYM1836PM–20C	PM03	
	CYM1836PZ–20C	PZ08	
25	CYM1836PJ–25C	PJ02	Commercial
	CYM1836PM–25C	PM03	
	CYM1836PZ–25C	PZ08	
30	CYM1836PJ–30C	PJ02	Commercial
	CYM1836LPJ–30C	PJ02	
	CYM1836PM–30C	PM03	
	CYM1836LPM–30C	PM03	
	CYM1836PZ–30C	PZ08	
	CYM1836LPZ–30C	PZ08	

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CYM1836PM–35C	PM03	Commercial
	CYM1836LPM–35C	PM03	
	CYM1836PZ–35C	PZ08	
	CYM1836LPZ–35C	PZ08	
45	CYM1836PM–45C	PM03	Commercial
	CYM1836LPM–45C	PM03	
	CYM1836PZ–45C	PZ08	
	CYM1836LPZ–45C	PZ08	

Shaded areas contain preliminary information

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