LH53515

CMOS 512K (64K × 8) Mask-Programmable ROM

FEATURES

- 65,536 × 8 bit organization
- Access time: 150 ns (MAX.)
- Low power consumption:
  Operating: 195 mW (MAX.)
  Standby: 550 µW (MAX.)
- Programmable output enable
- Static operation (Internal sync. system)
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  28-pin, 600-mil DIP
  28-pin, 450-mil SOP
  32-pin, 525-mil SOP
  44-pin, 10 × 10 mm^2 QFP
- JEDEC standard EPROM pinout (DIP)

PIN CONNECTIONS

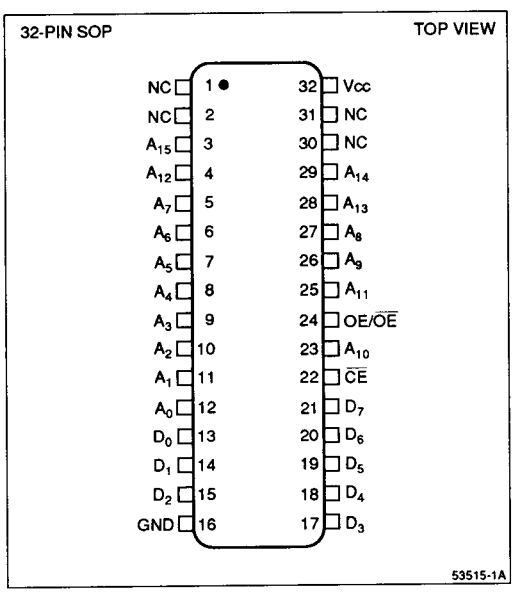


Figure 1. Pin Connections for SOP Package

DESCRIPTION

The LH53515 is a mask-programmable ROM organized as 65,536 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

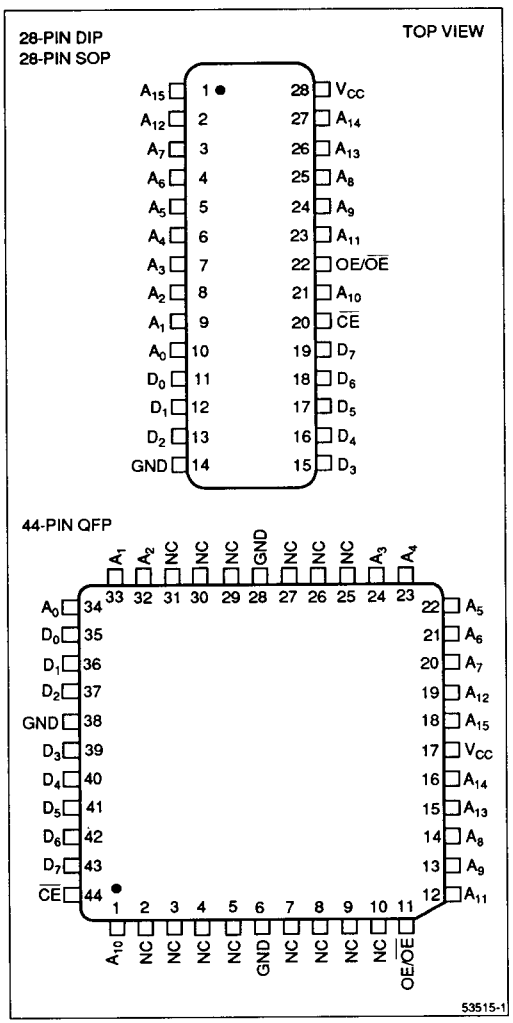


Figure 2. Pin Connections for DIP, SOP, and QFP Packages

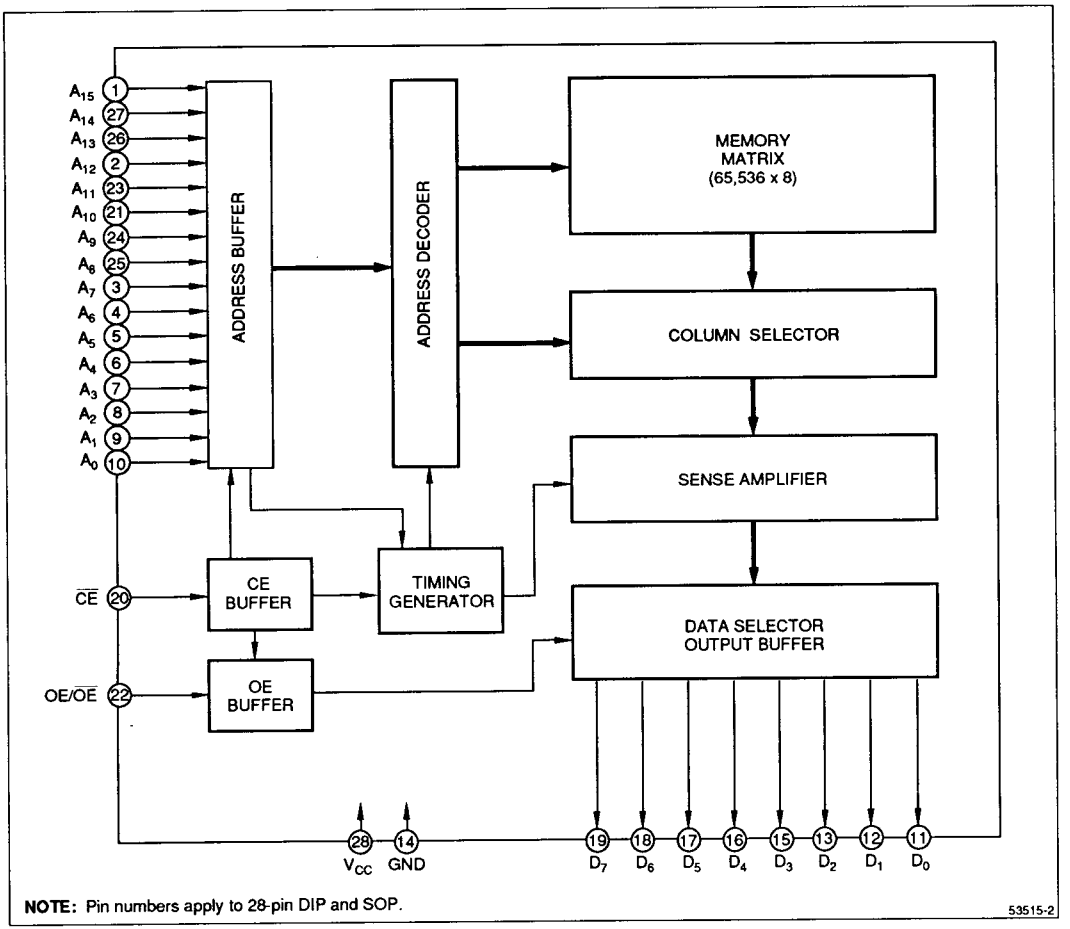


Figure 3. LH53515 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{15}	Address input	
D_0 - D_7	Data output	
$\overline{CE}$	Chip enable input	

SIGNAL	PIN NAME	NOTE
OE/$\overline{OE}$	Output enable input	1
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:
1. Active level of OE/$\overline{OE}$ is mask-programmable.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	MODE	D_0 - D_7	CURRENT CONSUMPTION	NOTE
H	X	Non selected	High-Z	Standby(I_{SB})	1
L	L/H			Operating(I_{CC})	
	H/L	Selected	D_{OUT}		

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	1
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	1
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			35	mA	2
	I_{CC2}	t_{RC} = 1 µs			25		
	I_{CC3}	t_{RC} = 150 ns			30	mA	3
	I_{CC4}	t_{RC} = 1 µs			20		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			2	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	

NOTES:
1. OE = V_{IL} or $\overline{CE}/\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}		150			ns	
Address access time	t_{AA}				150	ns	
Chip enable access time	t_{ACE}				150	ns	
Output enable time	t_{OE}		10		80	ns	
Output hold time	t_{OH}		5			ns	
$\overline{CE}$ to output in High-Z	t_{CHZ}				70	ns	1
OE to output in High-Z	t_{OHZ}				70	ns	1

NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

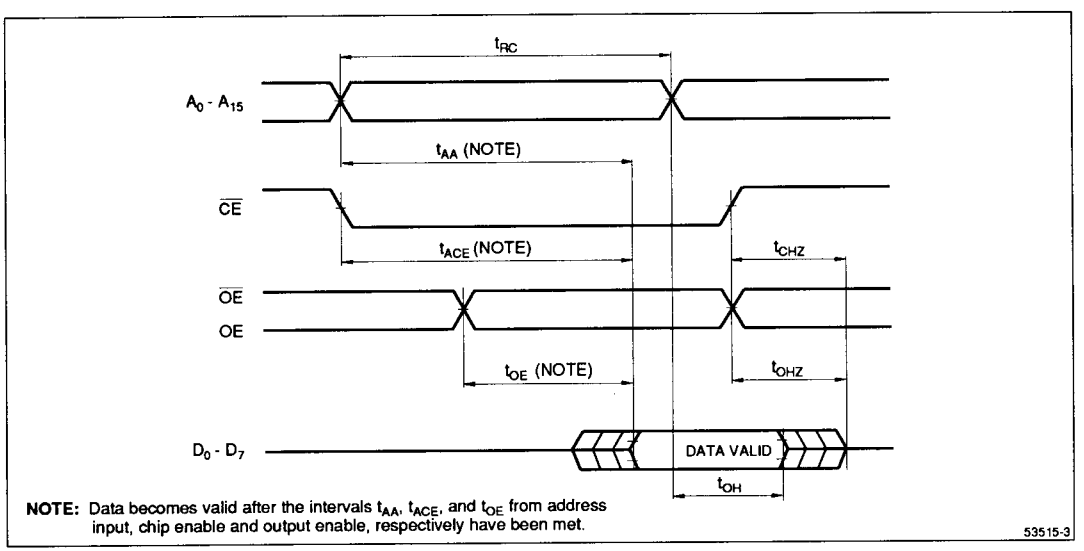


Figure 4. Timing Diagram

OPERATION IMMEDIATELY AFTER POWER UP

To ensure valid data immediately after power up and once the supply is stable, perform one of the following operations:

1. If the Chip Enable ($\overline{CE}$) was high during power up, switch the $\overline{CE}$ input from HIGH to LOW. (t_{ACE}) or
2. Change one or more addresses A_2 - A_{15} if the $\overline{CE}$ input was LOW at power up. (t_{AA})

The valid data will be output at t_{ACE} or t_{AA} following a transition from the above operations (1) or (2).

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and GND.

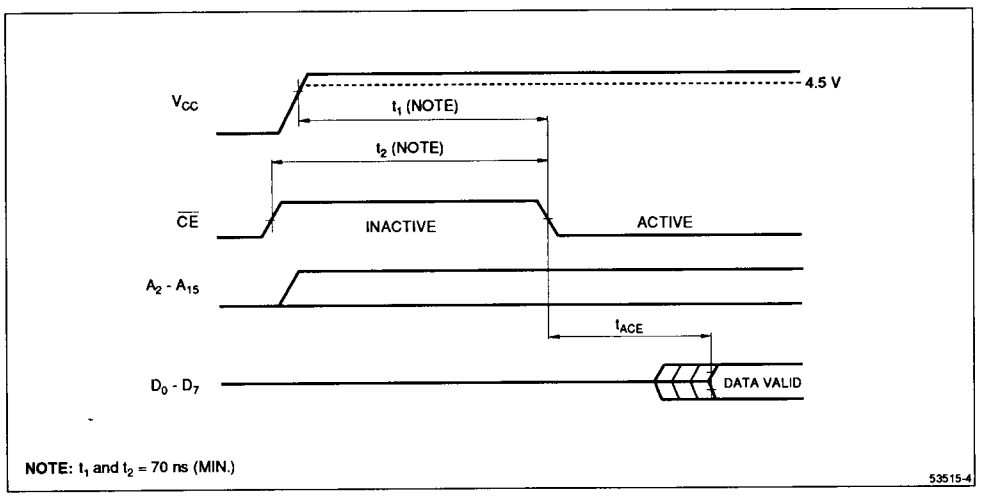


Figure 5. Power On With $\overline{CE}$ Inactive

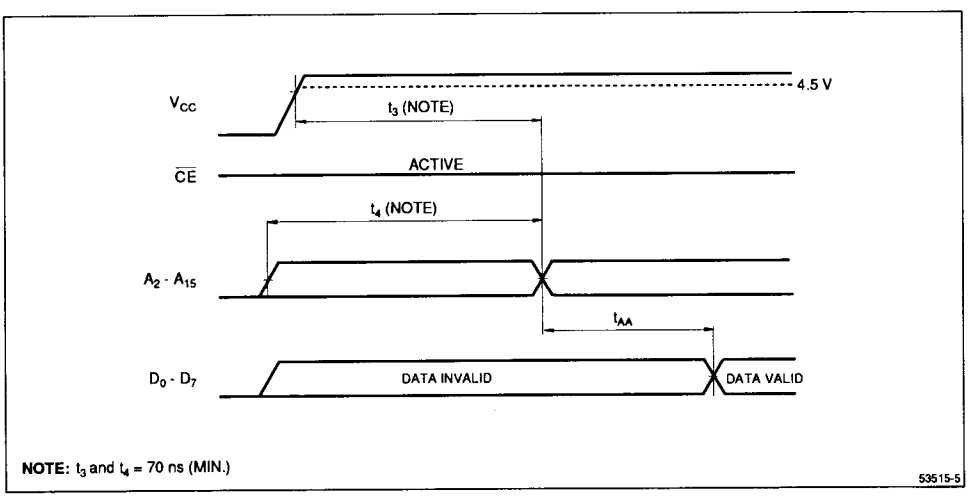
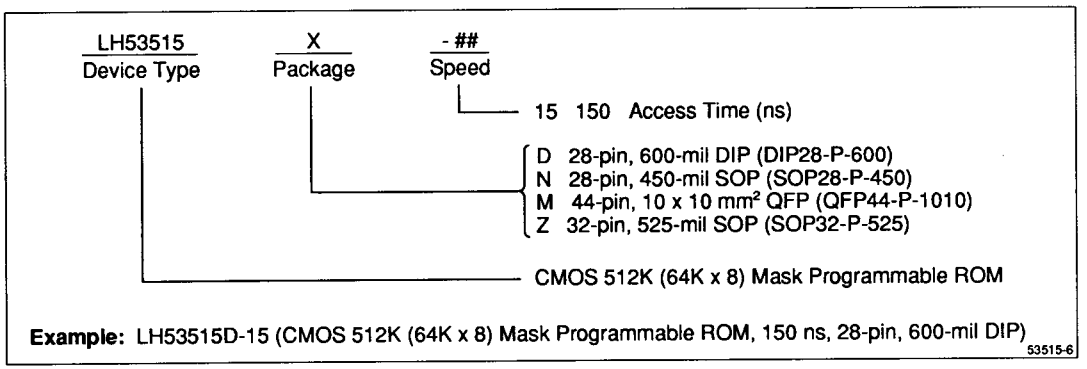


Figure 6. Power On With $\overline{CE}$ Active

ORDERING INFORMATION



Example: LH53515D-15 (CMOS 512K (64K x 8) Mask Programmable ROM, 150 ns, 28-pin, 600-mil DIP)