

DESCRIPTION

The HY51V18165B is the new generation and fast dynamic RAM organized 1,048,576 x 16-bit. The HY51V18165B utilized Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to prove wide operating margin to the users. This device can be packaged in industry-standard 42/42 plastic SOJ, 44/50 TSOP-II and Reverse TSOP-II.

The HY51V18165B is a burst access DRAM in which all READ and WRITE cycles occur in bursts of four. The burst wrap around on a eight byte boundary. This means only the two least significant bits of the CAS address are modified internally to produce each address of the burst sequence.

The burst type, interleave or linear, is determined by executing a WCBR cycle with address A0 set to either HIGH or LOW. A0 LOW will program the device to execute linear bursts, A0 HIGH will program the bursts to be interleaved. For future compatibility it is strongly recommended that the information 0010 000X (where x=A0) is supplied on addresses A7-A0 during the WCBR cycle. The WCBR cycle must be followed by a RAS-only or CBR to exit programming mode.

FEATURES

- Low power dissipation
Max. CMOS standby 0.83mW
Max. TTL standby 0.33mW
Max. operating

Speed	Power1	Power2
50	576mW	648mW
60	540mW	612mW
70	504mW	576mW

NOTE

Power1: Closed Row Burst Read/Write
Power2: Open Row Burst Read/Write

- Single power supply of 3.3V±5%
- All inputs and outputs are LVTTTL compatible with 5V input/output tolerance
- Fast access and cycle time

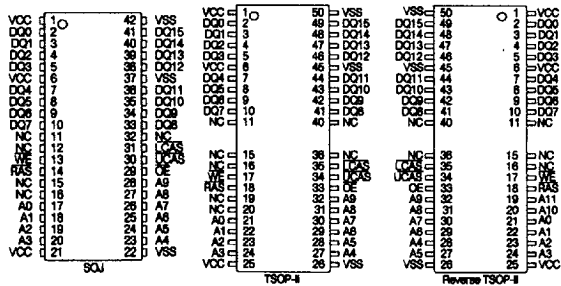
Speed	tRAC	tCAC	tPC
50	52ns	10ns	15ns
60	60ns	11.6ns	16.6ns
70	70ns	15ns	20ns

- Burst EDO mode operation
- Burst order, interleave or linear, programmed by executing WCBR cycle after initialization
- Industry-standard x 16 pinout and package
- CAS-before-RAS, RAS-only refresh capability
- 1024 refresh cycles /16ms
- Four cycle EDO burst access

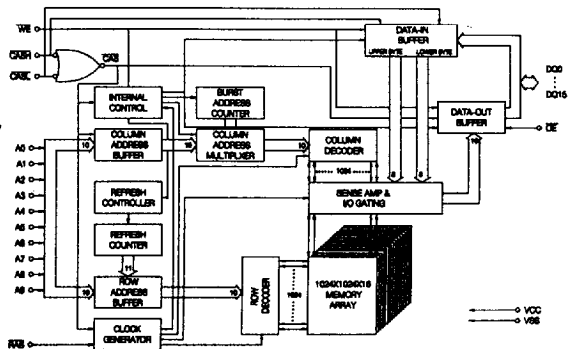
PIN DESCRIPTION

RAS	Row Address Strobe
LCAS, UCAS	Column Address Strobe
WE	Write Enable
OE	Output Enable
A0 - A9	Address Input
DQ0-DQ15	Data Input/Output
Vcc	Power (+3.3V)
Vss	Ground

PIN CONNECTION



BLOCK DIAGRAM



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EDO BURST MODE TRUTH TABLE

PRESENT-STATE	RESULTING STATE	RAS	CAS	WE	OE	ADDRESS		DATA
						Row	Column	DQ
Any	Idle	L → H	H	X	X	X	X	High-Z
Idle	Row Open	H → L	H	X	X	Row	X	High-Z
Idle	CBR REFRESH	H → L	L	H	X	X	X	High-Z
Row Open	RAS-only REFRESH	H→L→H	H	X	X	Row	X	High-Z
Row Open	READ burst	L	H→L	H	L	X	Col	Data-Out
Row Open	WRITE burst	L	H→L	L	X	X	Col	Data-In
READ burst	TERMINATE READ burst	L	H	H→L	X	X	X	High-Z
WRITE burst	TERMINATE WRITE burst	L	H	L→H	X	X	X	High-Z
Idle	PROGRAM burst type	H → L	L	L	X	A0	X	High-Z
PROGRAM	EXIT PROGRAM MODE	H → L	L	H	X	X	X	High-Z
PROGRAM	EXIT PROGRAM MODE	H→L→H	H	X	X	Row	X	High-Z

Note:

1. A WCBR cycle determines the burst sequence. A0=LOW sets burst sequence to linear, A0=HIGH set the burst sequence to interleave, A8 through A9 are don't care. A7-A0 should contain the sequence (0010 000X where X=A0) to ensure future compatability. A refresh cycle (RAS-only or CBR) must follow WCBR cycle to exit the programming mode.

INTERLEAVE BURST SEQUENCE TABLE

OPERATION	ADDRESSES USED		
	A9 - A2	A1	A0
First access, register external CAS address	A9 - A2	A1	A0
Second access (first burst address)	registered A9 - A2	registered A1	registered A0
Third access (second burst address)	registered A9 - A2	registered A1	registered A0
Fourth access (third burst address)	registered A9 - A2	registered A1	registered A0

INTERLEAVE BURST ADDRESS TABLE

FIRST ADDRESS	SECOND ADDRESS	THIRD ADDRESS	FOURTH ADDRESS
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

LINEAR BURST ADDRESS TABLE

FIRST ADDRESS	SECOND ADDRESS	THIRD ADDRESS	FOURTH ADDRESS
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

ABSOLUTE MAXIMUM RATING

SYMBOL	PARAMETER	RATING	UNIT
T _A	Ambient Temperature	0 to 70	°C
T _{STG}	Storage Temperature	-55 to 150	°C
V _{IN} , V _{OUT}	Voltage on Any Pin Relative to V _{SS}	-0.1 to 5.5	V
I _{OS}	Short Circuit Output Current	50	mA
P _D	Power Dissipation	1.1	W

NOTE: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTE
V _{CC}	Power Supply Voltage	3.13	3.47	V	
V _{IH}	Input High Voltage	2.0	5.5	V	2
V _{IL}	Input Low Voltage	-1.0	0.8	V	2

NOTE: All Voltage are referenced to V_{SS}.

DC CHARACTERISTICS

(TA=0°C to 70°C, Vcc=3.3V±10%, Vss=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
I _{LI}	Input Leakage Current (Any Input Pins)	0V ≤ V _{IN} ≤ 5.5V All other pins not under test = 0V		-2	2	μA	
I _{LO}	Output Leakage Current (High impedance State)	0V ≤ V _{OUT} ≤ 5.5V RAS & CAS at V _{IH}		-10	10	μA	
I _{CC1}	Vcc Supply Current, TTL Standby	RAS & CAS at V _{IH} (min.), other inputs ≥ Vss		-	2	mA	
I _{CC2}	Vcc Supply Current, CMOS Standby	RAS & CAS ≥ Vcc-0.2V		-	0.5	mA	
I _{CC3}	Vcc Supply Current, Operating ; Closed Row Burst Read / Write	tpc = tpc (min): 50% duty cycle on RAS: Open Row, 4 Cycle Burst, Close Row	50	-	160	mA	5
			60	-	150		
			70	-	140		
I _{CC4}	Vcc Supply Current, Operating : Open Row Burst Read / Write	tpc = tpc (min): Alternating 4 cycles inactivity	50	-	180	mA	5
			60	-	170		
			70	-	160		
I _{CC5}	Vcc Supply Current, RAS-only refresh	tpc = tpc (min.)	50	-	200	mA	4
			60	-	190		
			70	-	180		
I _{CC6}	Vcc Supply Current, CAS-before- RAS refresh	trc = trc (min.)	50	-	200	mA	4,6
			60	-	190		
			70	-	180		
V _{OL}	Output Low Voltage	I _{OL} = 2mA		-	0.4	V	
V _{OH}	Output High Voltage	I _{OH} = -2mA		2.4	-	V	

CAPACITANCE

(TA=25°C, Vcc=3.3V±10%, Vss=0V, f=1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTE
C _{I1}	Input Capacitance : Address		5	pF	3
C _{I2}	Input Capacitance : RAS		6	pF	3
C _{I3}	Input Capacitance : CAS, WE, OE		5	pF	3
C _{I0}	Data Input/Output Capacitance : DQ		7	pF	3

AC CHARACTERISTICS

(TA=0°C to 70°C, Vcc=3.3V ± 5%, VSS=0V, unless otherwise noted.) NOTE: 7, 8, 9, 10, 11

#	SYMBOL	PARAMETER	HY51V18165BJC/TC/RC						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tPC	Burst EDO Cycle Time	15	-	16.6	-	20	-	ns	
2	tRAC	Access Time from RAS	-	50	-	60	-	70	ns	
3	tCAC	Access Time from CAS	-	10	-	11.6	-	15	ns	
4	tAA	Access Time from Column-Address	-	25	-	28.2	-	35	ns	12
5	tOEA	Output Enable Access Time	-	10	-	12	-	15	ns	
6	tCOH	Data Hold Time from CAS Low	3	-	3	-	3	-	ns	
7	tRAS	RAS Pulse Width	50	125K	60	125K	70	125K	ns	
8	tRP	RAS Precharge Time	30	-	40	-	50	-	ns	
9	tRSH	RAS Hold Time	0	-	0	-	0	-	ns	
10	tCAS	CAS Pulse Width	5	10K	5	10K	5	10K	ns	
11	tCP	CAS Precharge Time	5	-	5	-	5	-	ns	
12	tRCD1	RAS to CAS Delay Time	20	-	16.6	-	20	-	ns	
13	tRCD2	RAS to CAS Delay Time	40	-	46.6	-	55	-	ns	
14	tCRP	CAS to RAS Precharge Time	10	-	10	-	10	-	ns	
15	tASR	Row-Address Set-up Time	1.5	-	1.5	-	1.5	-	ns	
16	tRAH	Row-Address Hold Time	8.5	-	8.5	-	8.5	-	ns	
17	tASC	Column-Address Set-Up Time	1.5	-	1.5	-	1.5	-	ns	
18	tCAH	Column-Address Hold Time	8.5	-	8.5	-	8.5	-	ns	
19	tRCS	Read Command Set-Up Time	3	-	4	-	5	-	ns	
20	tRCH	Read Command Hold Time	5	-	5	-	5	-	ns	
21	tOEP	OE High Pulse Width	10	-	10	-	10	-	ns	
22	tOELZ	OE to Output Low-Z	3	-	3	-	3	-	ns	13
23	tOD	Output Disable	4	10	4	10	4	15	ns	13
24	tOES	Output Enable Set-Up (Only near CAS)	3	-	3	-	3	-	ns	
25	tOEH	Output Enable Hold (Only near CAS)	5	-	5	-	5	-	ns	
26	tCLZ	CAS to Output in Low-Z	3	-	3	-	3	-	ns	13
27	tOFF	Output Buffer Turn-Off Delay	4	10	4	10	4	15	ns	13
28	tBTH	Burst Terminate Hold Time	3	-	3	-	3	-	ns	
29	tBTHZ	Output disable from burst Terminate	7	13	7	13	7	13	ns	13,16
30	tWCS	WE Command Set-Up Time	3	-	4	-	5	-	ns	
31	tWCH	Write Command Hold Time	5	-	5	-	5	-	ns	
32	tWHZ	WE to Output High-Z	4	10	4	10	4	15	ns	13,16
33	tTP	Burst Terminate Pulse Width	6	-	6	-	8	-	ns	14
34	tCRW	CAS Low to RAS High (Required Only for WRITE Only)	15	-	16.6	-	20	-	ns	
35	tDS	Data-in Set-Up Time	0	-	0	-	0	-	ns	
36	tDH	Data-in Hold Time	5	-	5	-	5	-	ns	
37	tT	Transition Time (rise or fall)	1.5	50	1.5	50	1.5	50	ns	
38	tREF	Refresh Period (1024 Cycle)	-	16	-	16	-	16	ms	
39	tRPC	RAS to CAS Precharge Time	5	-	5	-	5	-	ns	
40	tRC	Random Read or Write cycle Time	90	-	110	-	130	-	ns	
41	tWRP	WE Set-Up Time (CBR or WCBR)	10	-	10	-	10	-	ns	
42	tWRH	WE Hold Time (CBR or WCBR)	10	-	10	-	10	-	ns	
43	tCPN	CAS Precharge Time (CBR or WCBR)	10	-	10	-	10	-	ns	
44	tCSR	CAS Set-Up Time (CBR or WCBR)	10	-	10	-	10	-	ns	6
45	tCHR	CAS Hold Time (CBR or WCBR)	15	-	15	-	15	-	ns	6

NOTE:

1. All voltage referenced to Vss.
2. Input Power-up : $V_{IH} \leq +5.5V$ and $V_{CC} \leq +3.13V$
for $t \leq 200msec$.
3. This parameter is sampled. $V_{CC}=3.3V \pm 5\%$: $f=1$ MHz
4. I_{CC} is dependent on cycle rates.
5. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum tPC and 50 percents duty cycle. The outputs are open.
6. Enables on-chip refresh and address counters.
7. Initialization consists of an initial pause of $100\mu s$ after power-up followed by eight \overline{RAS} refresh cycles (\overline{RAS} -only or CBR with \overline{WE} HIGH). This sequence must be executed before proper device operation is assured. The eight \overline{RAS} cycle wake-ups should be repeated any time the tREF refresh requirement is exceeded. A WCBR cycle must be executed to initialize the burst type, interleave or linear followed by a \overline{RAS} -only or CBR refresh cycle.
8. AC characteristics assume $t_T=1.5ns$.
9. All output timings are referenced to 1.5V and all input timings are referenced to 1.5V, unless otherwise specified. Inputs must be driven to the appropriate voltage levels indicated by the corresponding timing diagrams when A.C. specifications are measured, as shown in Figure 1.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. NC pins are assumed to be left floating and are not tested for leakage.
12. t_{AA} is a calculated specification which is the sum of tPC and tCAC.
13. Output loading is specified with $C_L=5pF$ as Figure 2. Transition is measured $\pm 200mV$ from steady state voltage. These parameters are sampled.
14. Applies only during burst termination operation.
15. AC output loading is specified with $C_L=50pF$ as in Figure 3. Figure 4. is shown for reference. Transition is measured at the 1.5V referenced level.
16. The latter of tWHZ or tBTHZ satisfied will place the DQ pins in the High-Z state.

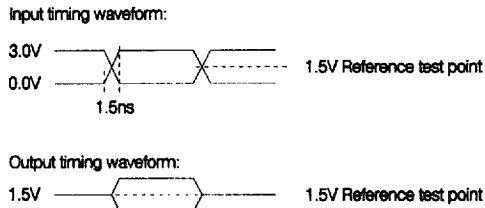


Fig. 1 TIMING SPECIFICATIONS

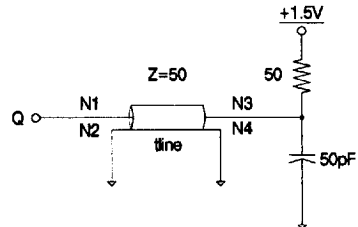


Fig. 3 AC TIMING OUTPUT LOAD EQUIVALENT

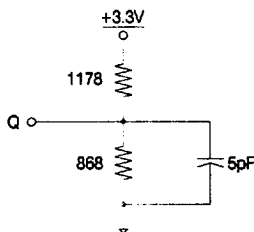


Fig. 2 HIGH-Z OUTPUT LOAD

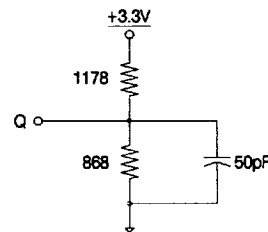
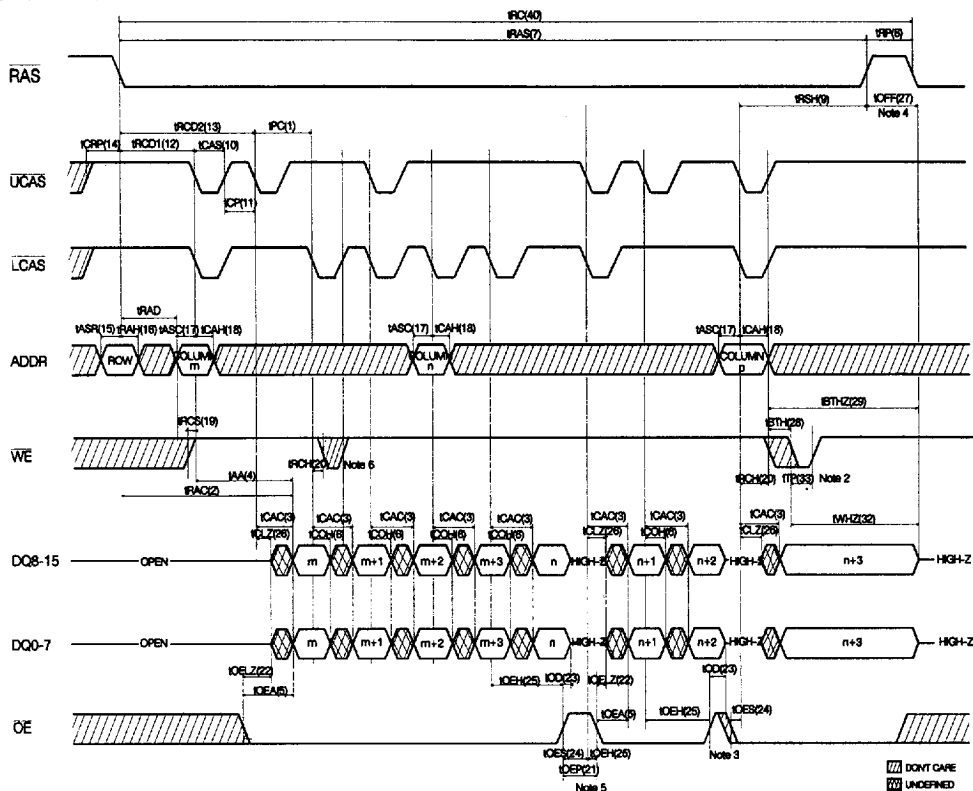


Fig. 4 OUTPUT LOAD EQUIVALENT

BURST EDO READ CYCLE



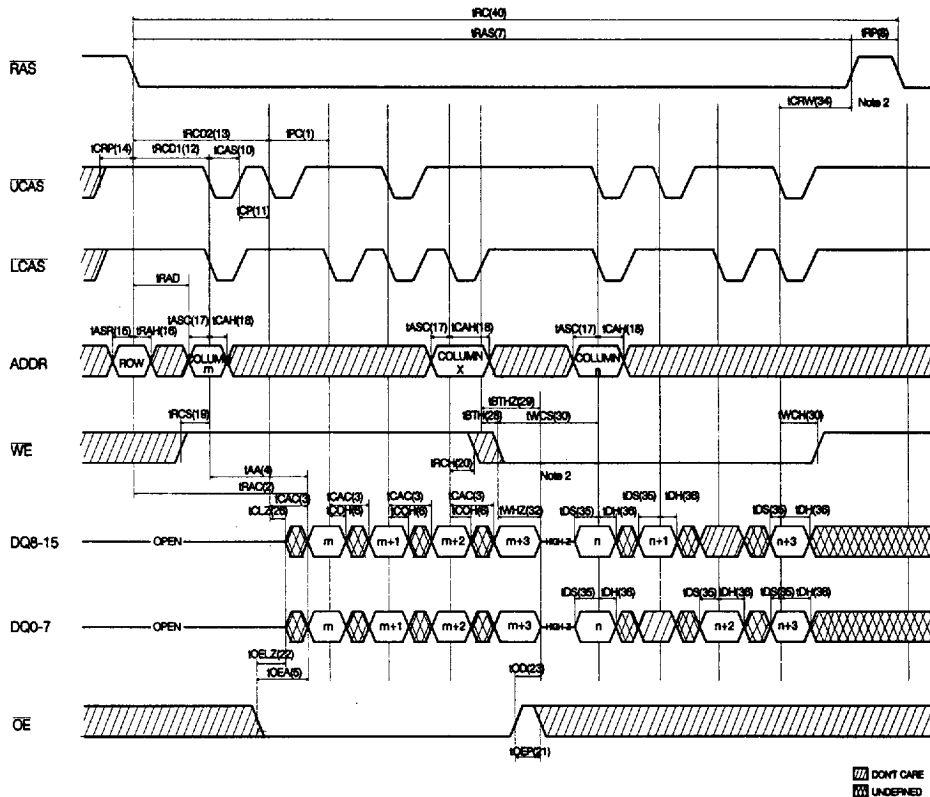
The timing diagram illustrates the operational timing for the 74VHC163 counter. Key signals and their timing relationships are as follows:

- RAS(7):** The master clock signal. Setup time $t_{SU}(7)$ and hold time $t_{HD}(7)$ are specified relative to the ICP(8) signal.
- ICP(8):** The clock input. Its setup and hold times are defined relative to RAS(7).
- ICPM(34):** The master clock input to the counter.
- UCAS and LCAS:** The user clock and load clock signals, respectively.
- ADDR:** The address bus, which includes ROW, COLUMN, and data bus signals (n, p). Timing parameters $t_{ASQ}(15)$, $t_{ASQ}(17)$, and $t_{ASQ}(18)$ are shown for the address signals.
- WE:** The write enable signal. Timing parameters $t_{WCH}(31)$ and $t_{WCH}(33)$ are indicated.
- DQ8-15 and DQ0-7:** The data bus signals. Timing parameters $t_{DS}(35)$ and $t_{DH}(36)$ are shown for the data signals.
- OE:** The output enable signal.

The diagram is divided into two sections: HIGH-Z and LOW-Z. The legend indicates that hatched areas represent 'DONT CARE' and white areas represent 'UNDEFINED'.

1. **LCAS** and **UCAS** each control their respective bytes on **WRITES**. Each must transition to write their respective byte. **UCAS** and **LCAS** must be **HIGH** coincident for 5ns. All setup and hold times are measured from the first **CAS** transitioning from **HIGH** to **LOW** on each **WRITE** cycle within the burst. The skew between **UCAS** and **LCAS** must not exceed 2ns.
2. **WE** transitioning **HIGH** will terminate the burst and reset the burst counter provided **tTP** and **tBTH** are satisfied.
3. **WE** transitioning **HIGH** and returning **LOW** prior to **CAS** going **HIGH** will not terminate the burst.

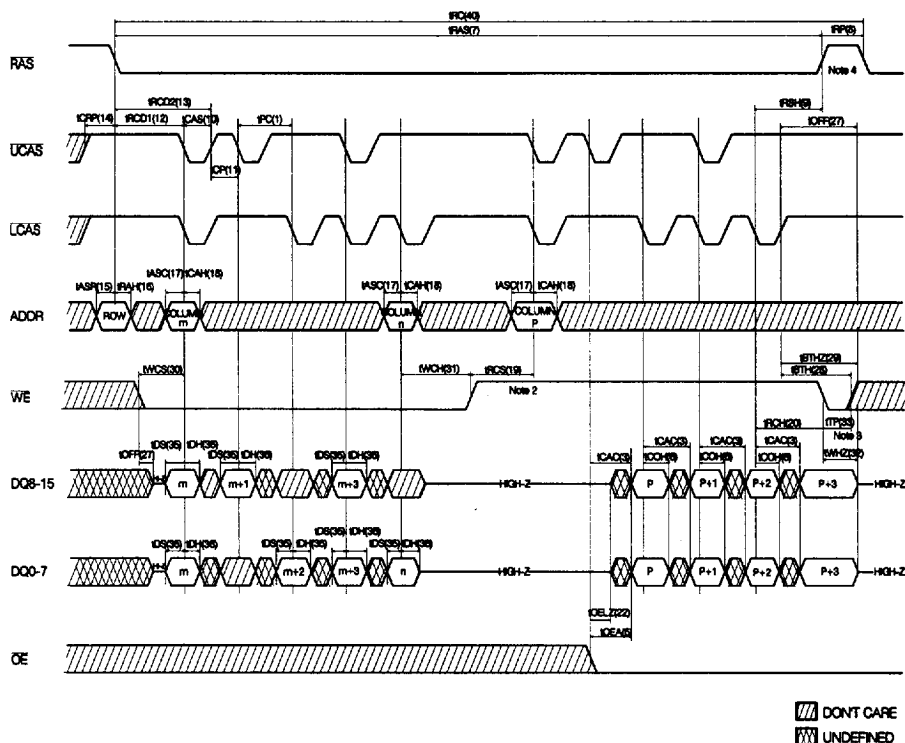
BURST EDO READ / WRITE CYCLE



NOTE:

- Both bytes are always output during READ operations.
 \overline{UCAS} and/or \overline{LCAS} control both bytes on READs \overline{UCAS} and \overline{LCAS} must transition within 2ns of each other.
 \overline{UCAS} and \overline{LCAS} must be HIGH coincident for 5ns.
 All setup, hold, and access times are measured from the first \overline{CAS} transitioning from HIGH to LOW on each LOW on each cycle within the burst.
 \overline{LCAS} and \overline{UCAS} each control their respective bytes on WRITES.
 Each must transition to write their respective byte.
 \overline{UCAS} and \overline{LCAS} must be HIGH coincident for 5ns.
 All setup and hold times are measured from the first \overline{CAS} transitioning from HIGH to LOW on each WRITE cycle within the burst. The skew between \overline{UCAS} and \overline{LCAS} must not exceed 2ns.
- \overline{WE} transitioning LOW will terminate the burst and reset the burst counter provided t_{TP} and t_{BTH} are satisfied.
 t_{TP} is met by the READ burst being terminated by a WRITE burst. The DQs will be placed in the High-Z state once the latter of the t_{WHZ} or t_{BTHZ} is satisfied.
- The combination of \overline{RAS} and \overline{CAS} HIGH close the row and place the DQs pins in the High-Z state.

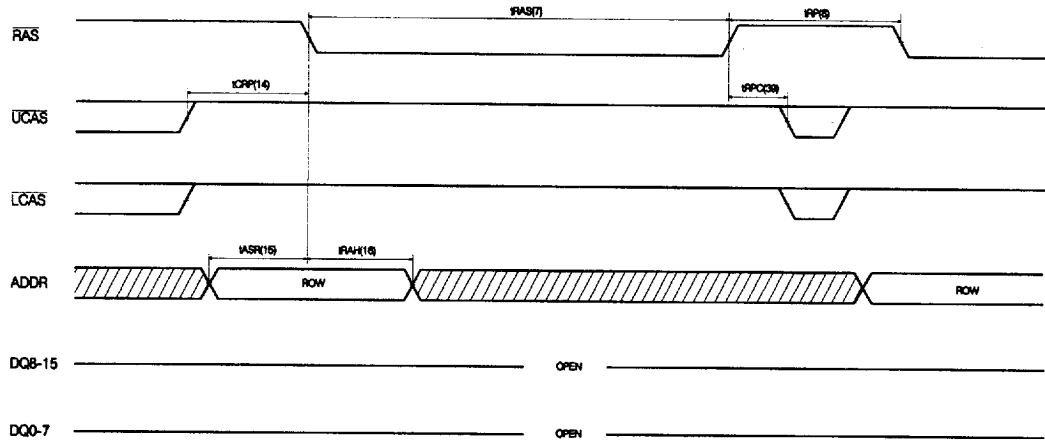
BURST EDO WRITE / READ CYCLE



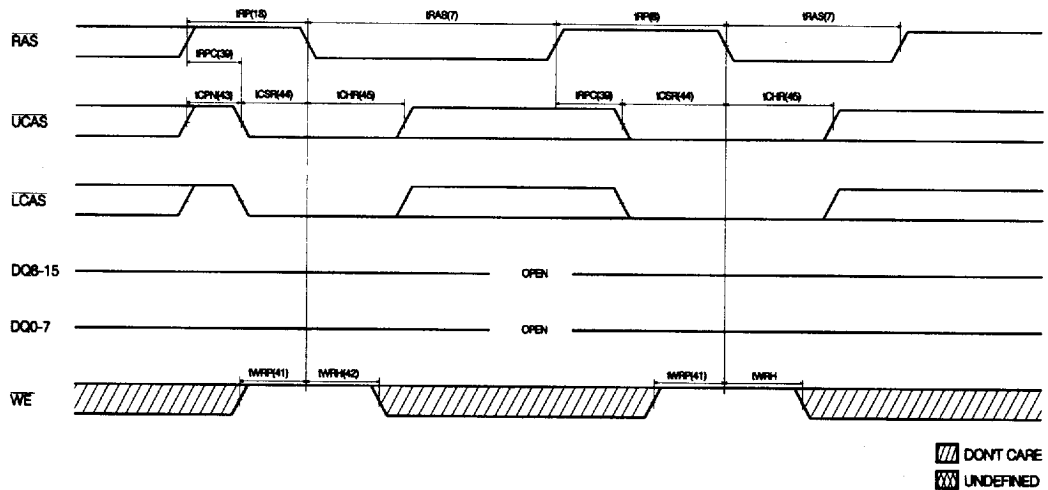
NOTE:

1. **LCAS** and **UCAS** each control their respective bytes on **WRITES**. Each must transition to write their respective byte. **UCAS** and **LCAS** must be **HIGH** coincident for 5ns. All setup and hold times are measured from the first **CAS** transitioning from **HIGH** to **LOW** on each **WRITE** cycle within the burst. The skew between **UCAS** and **LCAS** must not exceed 2ns. Both bytes are always output during **READ** operations. **UCAS** and/or **LCAS** control both bytes on **READS**. **UCAS** and **LCAS** must transition within 2ns of each other. **UCAS** and **LCAS** must be **HIGH** coincident for 5ns. All setup, hold, and access times are measured from the first **CAS** transitioning from **HIGH** to **LOW** on each **READ** cycle within the burst.
2. **WE** transitioning **HIGH** will terminate the burst and reset the burst counter. The **tBTH** time is not required as it is satisfied by **TRCS**: **tTP** is met by the **WRITE** burst being terminated by a **READ** burst.
3. **WE** transitioning **LOW** will terminate the burst and reset the burst counter provided **tTP** and **tBTH** are satisfied. The **DQs** will be placed in the **High-Z** state once the latter of **tWHZ** or **tBTHZ** is satisfied.
4. The combination of **RAS** and **CAS** **HIGH** close the row and place the **DQ** pins in the **High-Z** state. **tOFF** is measured from the last signal (**RAS** or **CAS**) that transitions **HIGH**.

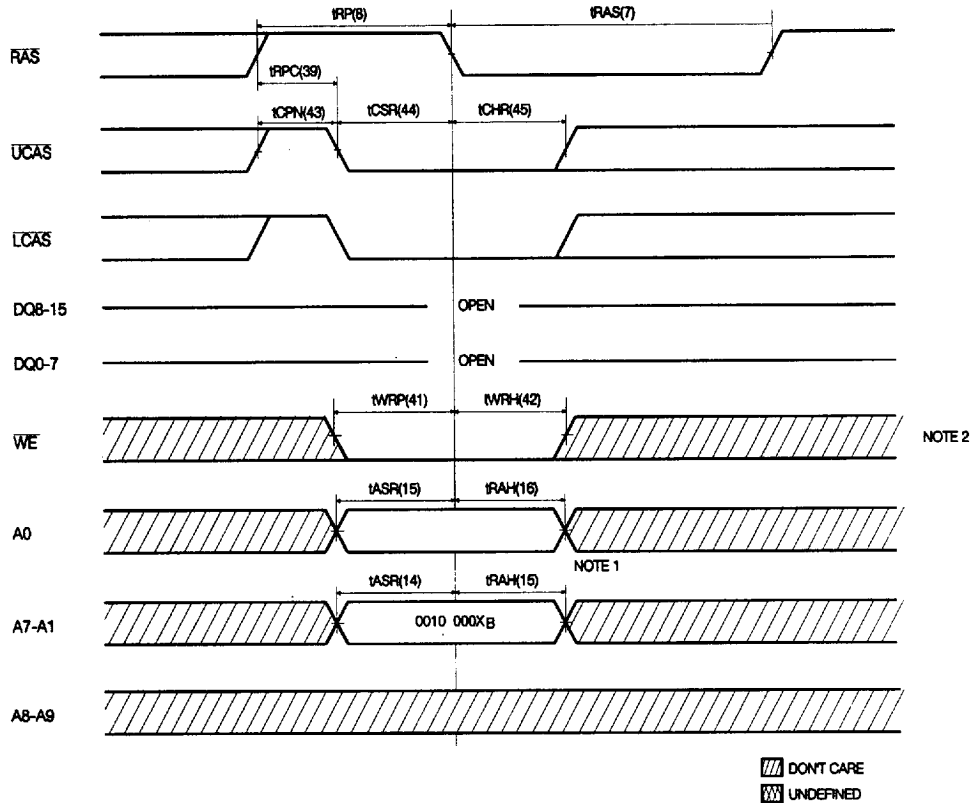
RAS-ONLY REFRESH CYCLE



CBR REFRESH CYCLE



WCBR PROGRAM CYCLE

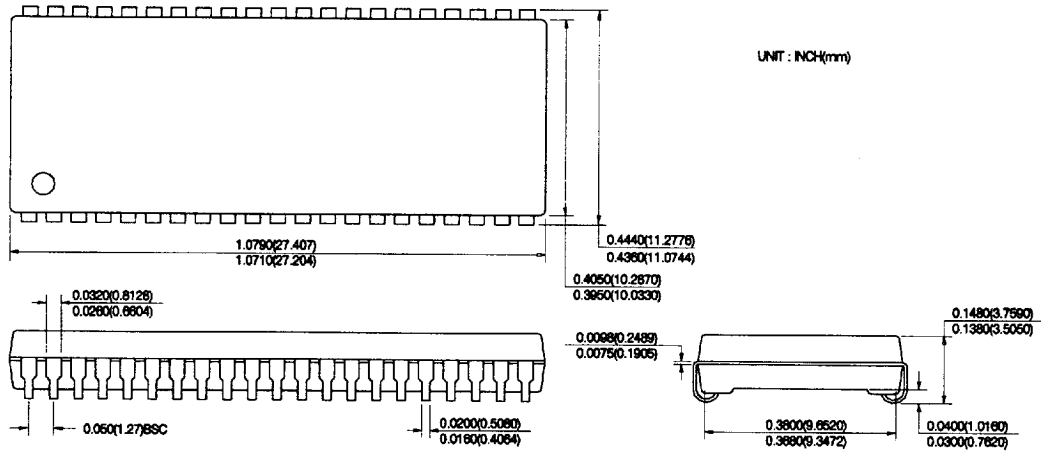


NOTE:

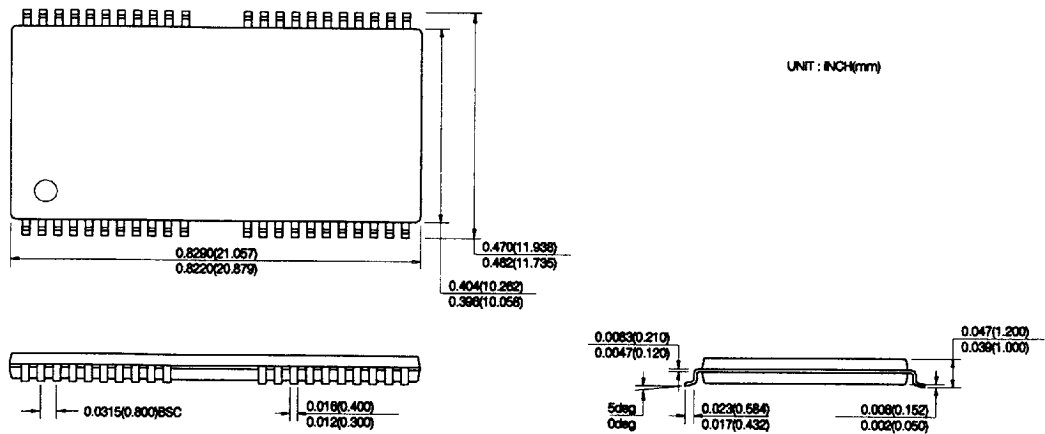
1. A0 LOW sets the burst sequence to linear bursts. A0 HIGH sets the burst sequence to interleave bursts. Addresses A8 through A9 are don't cares. Address A7-A1 should contain the state of (0010 000X_B where x=A0) to ensure future compatability. The burst sequence will remain set until the device power is interrupted or another WCBR cycle is executed.
2. A RAS-only or CBR refresh cycle must be executed after the WCBR cycle to exit the programming mode.

PACKAGE INFORMATION

400 mil 42 pin Small Outline J-form Package (JC)



400 mil 44/50 pin Thin Small Outline Package (TC) (RC)



ORDERING INFORMATION

PART NO	SPEED	POWER	PACKAGE
HY51V18165BJC	50/60/70		SOJ
HY51V18165BTC	50/60/70		TSOP-II
HY51V18165BRC	50/60/70		TSOP-II(R)