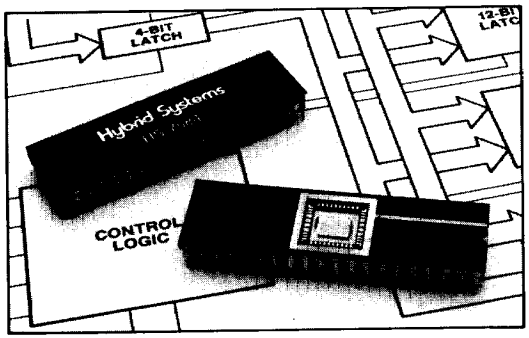
HS 7584

Quad 12-Bit MDAC

FEATURES

- Four 12-Bit DACs on a Single Monolithic Chip
- Independent V_{REF} Input For Each DAC
- Low Power CMOS (5 mW)
- Single +5V Operation
- Double Buffered Input Structure for μP Interface
- Available in 40-Pin DIP or 44-Pin LCC/PLCC



DESCRIPTION

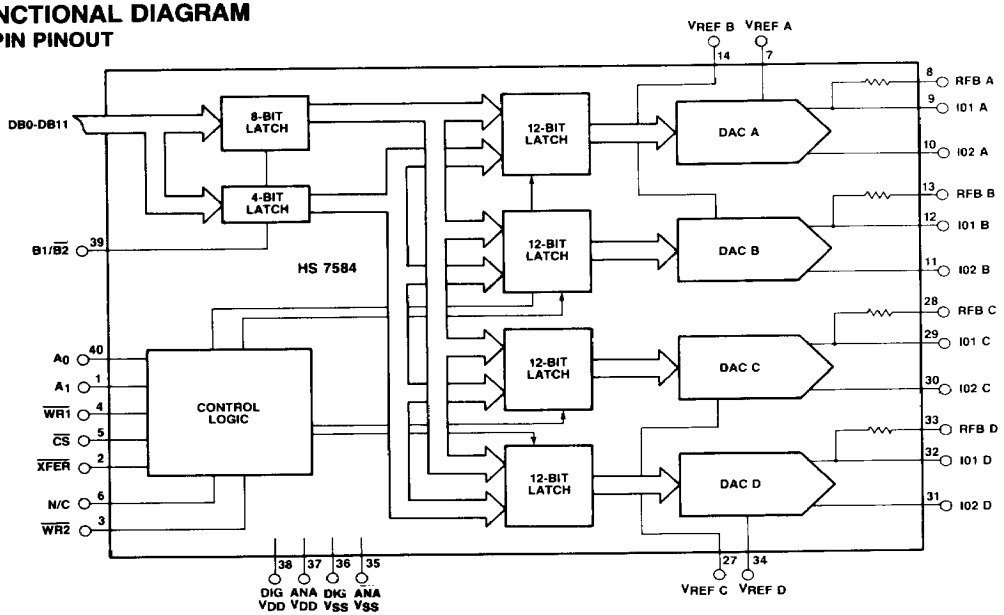
The HS 7584 contains four CMOS current output D/A converters on a single monolithic chip. All four DACs provide 4-quadrant multiplication with a separate reference input and feedback resistor for each DAC. Monolithic construction ensures excellent matching and tracking between all four DACs.

The double buffered input structure is designed to accept 12-Bit parallel data or 8-Bit/4-Bit data allowing easy microprocessor interface. All four DACs may be simultaneoulsy updated using a single $\overline{XFER}$ command.

The HS 7584 is packaged in a 40-Pin DIP as well as a 44-Pin LCC and PLCC and operates from a +5V power supply. Processing to MIL-STD-883B, Rev C is available.

7

FUNCTIONAL DIAGRAM
40-PIN PINOUT



SPECIFICATIONS

(Typical @25°C with $V_{DD} = V_{SS} = +5V$, $V_{REF} = +10V$ unless otherwise noted.)

MODEL	HS 7584	
PACKAGE	**DIP/LCC**	**PDIP/PLCC**
DIGITAL INPUTS		
Resolution	12-Bits	*
V_{IH} Logic Level	2.4V min	*
V_{IL} Logic Level	0.8V max	*
I_{IN} Input Current	1μA typ, 4μA max	*
2 Quad, Unipolar Coding	Straight Binary	*
4 Quad, Bipolar Coding	Offset Binary	
REFERENCE INPUT		
Input Resistance	5kΩmin, 10kΩtyp, 15kΩmax	*
STATIC PERFORMANCE		
Integral Linearity	0.006% FSR typ, 0.012% FSR max	*
Differential Linearity	0.006% FSR typ, 0.024% FSR max	*
Monotonicity	12-Bits	*
DYNAMIC PERFORMANCE		
Output Current Settling Time	2μ sec typ, 3μ sec max	*
Data Set-Up Time	100 nsec min	*
Data Hold Time	0 nsec min	*
Write Pulse Width	100 nsec min	*
ANALOG OUTPUT		
Scale Factor	$100\mu A/V_{REF}$	*
Scale Factor Accuracy	±0.0488% typ, 0.0976% max	±0.15% max
I_O Leakage	1 nA typ, 10 nA max	*
Output Capacitance	80 pF typ	*
STABILITY		
Scale Factor	1 ppm/°C typ, 2 ppm/°C max	10 ppm/°C
Integral Linearity	0.5 ppm/°C typ, 1 ppm/°C max	*
Differential Linearity	0.5 ppm/°C typ, 1 ppm/°C max	*
Input Impedance	−400 ppm/°C typ	*
I_{OUT} Leakage (T_{MIN}-T_{MAX})	100 nA typ, 200 nA max	*
Scale Factor Tracking (DAC to DAC)	2 ppm/°C typ, 4 ppm/°C max	*
POWER REQUIREMENTS		
Operating Voltage	+5V ±5%	*
Supply Current		
V_{IN} = 0 or 5V	0.5 mA typ, 1 mA max	*
V_{IN} = 0.8V or 2.0V	5 mA typ, 10 mA max	*
Power Supply Rejection Ratio	0.0005%/%typ, .002%/% max	0.0025%/%
Power Dissipation		
V_{IN} = 0 or 5V	2.5 mW typ, 5.0 mW max	*
V_{IN} = 0.8V or 2.0V	25 mW typ, 50 mW max	*

*Specifcations same as HS 7584-DIP/LCC

ABSOLUTE MAXIMUM RATINGS

V_{DD} 7V
V_{SS} . . . . . ±0.4V
V_{REF} A,B,C,D . . . . . ±20V
RFB A,B,C,D . . . . . ±20V
Digital Input Voltage . . . . . −0.3V to 5.5V
V_{PIN} 9,10,11,12,29,30,31,32 . . . . . ±0.4V
ANGND to DGND . . . . . ±0.4V
Power Dissipation (Any Package)
To +75°C . . . . . 450 mW
Derates above +75°C . . . . . 6 mW/°C
Operating Temperature Range
Commercial . . . . . 0 to +70°C
Extended . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C

PIN ASSIGNMENTS (DIP, PDIP)

PIN	FUNCTION	DESCRIPTION
1	A1	Address Line 1
2	$\overline{XFER}$	Transfer. Updates all DAC's
3	$\overline{WR2}$	Write Input. Active Low. Gates Transfer Fuction
4	$\overline{WR1}$	Write Input. Active Low. Gates DAC Selection
5	$\overline{CS}$	Chip Select Input. Active Low
6	N/C	No Connection
7	V_{REF} A	Voltage Reference Input to DAC A
8	RFB A	Reference Feedback Resistor of DAC A
9	IO1 A	Current Output to Virtual Ground
10	IO2 A	Current Output – Complement of IO1 A
11	IO2 B	Current Output – Complement of IO2 B
12	IO1 B	Current Output to Virtual Ground
13	RFB B	Reference Feedback Resistor of DAC B
14	V_{REF} B	Voltage Reference Input to DAC B
15	DB11	Data Bit 11 (MSB)
16	DB10	Data Bit 10
17	DB9	Data Bit 9
18	DB8	Data Bit 8
19	DB7	Data Bit 7
20	DB6	Data Bit 6
21	DB5	Data Bit 5
22	DB4	Data Bit 4
23	DB3	Data Bit 3
24	DB2	Data Bit 2
25	DB1	Data Bit 1
26	DB0	Data Bit 0 (LSB)
27	V_{REF} C	Voltage Reference Input to DAC C
28	RFB C	Reference Feedback Resistor of DAC C
29	IO1 C	Current Output to Virtual Ground
30	IO2 C	Current Output – Complement of IO1 C
31	IO2 D	Current Output - Complement of IO1 D
32	IO1 D	Current Output to Virtual Ground
33	RFB D	Reference Feedback Resistor of DAC D
34	V_{REF} D	Voltage Reference Input to DAC D
35	AV_{SS}	Analog Ground
36	DV_{SS}	Digital Ground
37	AV_{DD}	Analog Supply
38	DV_{DD}	Digital Supply
39	B1/$\overline{B2}$	Byte 1/Byte 2. Selects Data Input Format 8-Bit/4-Bit or 12-Bit Parallel
40	A0	Address Line 2

PIN ASSIGNMENTS (LCC, PLCC)

PIN	FUNCTION	DESCRIPTION
1	A1	Address Line 1
2	$\overline{XFER}$	Transfer. Updates all DAC's
3	$\overline{WR2}$	Write Input. Active Low. Gates Transfer Fuction
4	$\overline{WR1}$	Write Input. Active Low. Gates DAC Selection
5	$\overline{CS}$	Chip Select Input. Active Low
6	N/C	No Connection
7	V_{REF} A	Voltage Reference Input to DAC A
8	RFB A	Reference Feedback Resistor of DAC A
9	IO1 A	Current Output to Virtual Ground
10	IO2 AF	Current Output (Forcing) } Complement of IO1 A
11	IO2 AS	Current Output (Sensing) }
12	IO2 BS	Current Output (Sensing) } Complement of IO2 B
13	IO2 BF	Current Output (Forcing) }
14	IO1 B	Current Output to Virtual Ground
15	RFB B	Reference Feedback Resistor of DAC B
16	V_{REF} B	Voltage Reference Input to DAC B
17	DB11	Data Bit 11 (MSB)
18	DB10	Data Bit 10
19	DB9	Data Bit 9
20	DB8	Data Bit 8
21	DB7	Data Bit 7
22	DB6	Data Bit 6
23	DB5	Data Bit 5
24	DB4	Data Bit 4
25	DB3	Data Bit 3
26	DB2	Data Bit 2
27	DB1	Data Bit 1
28	DB0	Data Bit 0 (LSB)
29	V_{REF} C	Voltage Reference Input to DAC C
30	RFB C	Reference Feedback Resistor of DAC C
31	IO1 C	Current Output to Virtual Ground
32	IO2 CF	Current Output (Forcing) } Complement of IO1 C
33	IO2 CS	Current Output (Sensing) }
34	IO2 DS	Current Output (Sensing) } Complement of IO1 D
35	IO2 DF	Current Output (Forcing) }
36	IO1 D	Current Output to Virtual Ground
37	RFB D	Reference Feedback Resistor of DAC D
38	V_{REF} D	Voltage Reference Input to DAC D
39	AV_{SS}	Analog Ground
40	DV_{SS}	Digital Ground
41	AV_{DD}	Analog Supply
42	DV_{DD}	Digital Supply
43	B1/$\overline{B2}$	Byte 1/Byte 2. Selects Data Input Format 8-Bit/4-Bit or 12-Bit Parallel
44	A0	Address Line 2

APPLICATIONS INFORMATION

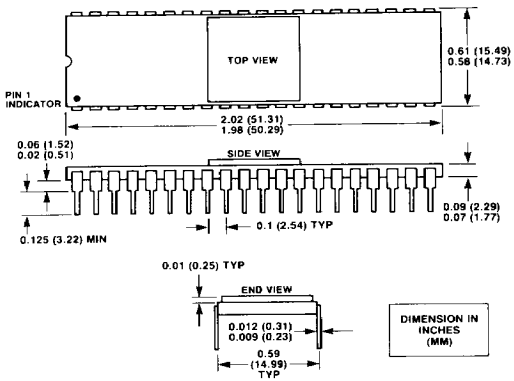
THEORY OF OPERATION

The HS 7584 is a quad MDAC designed to provide maximum flexibility. Each current output DAC provides 4-quadrant multiplication for unipolar and bipolar output and has an individual reference input and feedback resistor. The monolithic HS 7584 gives a designer four DAC's with excellent matching and tracking which accept separate AC or DC signals. The quad MDAC is therefore ideal for those applications where multiple digital to analog conversion roles are required in a small package with optimum thermal and gain error matching characteristics.

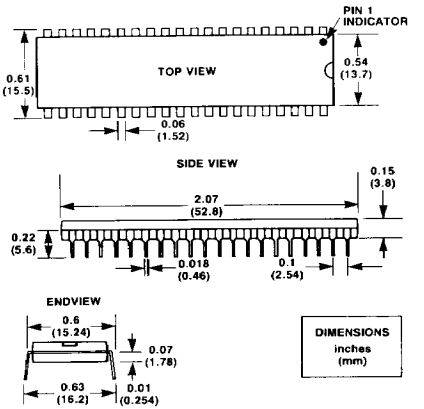
Maximum flexibility has also been applied to the microprocessor compatible control inputs. A double buffered input structure allows simple interface to many microprocessors without the need for external latches. The first buffer has been split to accept 12-Bit parallel data or 8-Bit/4-Bit data allowing direct interface to 8- or 12-Bit bus structures. A separate control line "B1/B2" allows the four MDAC's to be selectively connected to an 8- and a 12-Bit bus without the need for rewiring.

The monolithic CMOS construction results in very low system level power requirements with a total dissipation of 2mW. The very low power requirement contributes to the excellent thermal and gain error matching between the four DAC's.

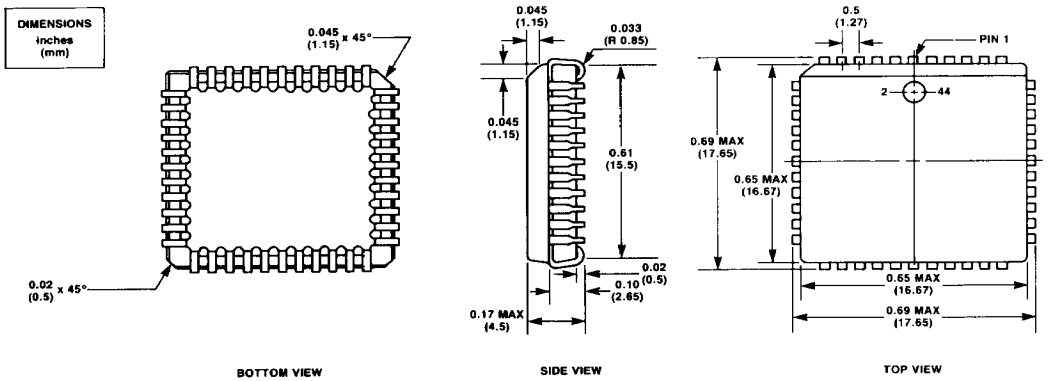
PACKAGE OUTLINE (DIP)



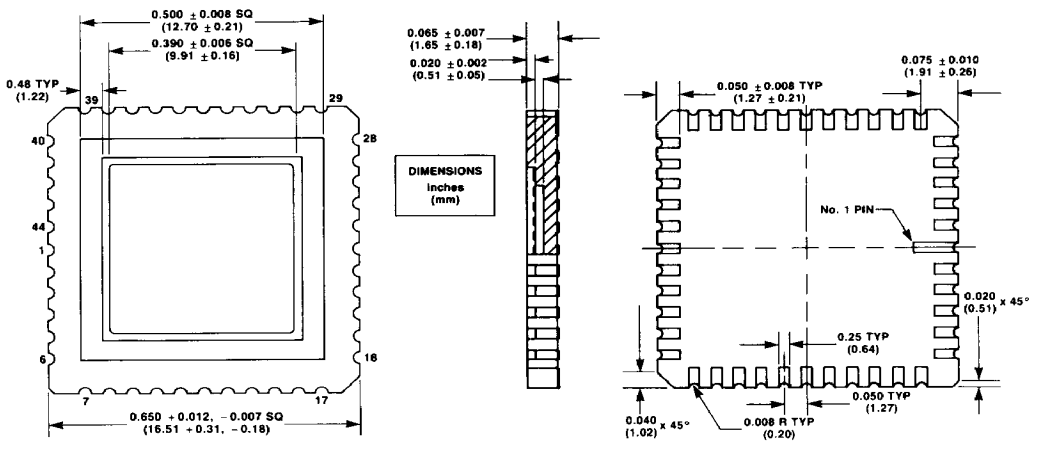
PACKAGE OUTLINE (PDIP)



PACKAGE OUTLINE (PLCC)



PACKAGE OUTLINE (LCC)



HS 7584 CONTROL INPUTS

A_0	A_1	$\overline{CS}$	$\overline{WR1}$	B1/$\overline{B2}$	$\overline{WR2}$	$\overline{XFER}$	HS 7584 OPERATION DESCRIPTION
0	0	0	0	1	1	1	Address DAC A register and loads data (register only)
1	0	0	0	1	1	1	Address DAC B register and loads data (register only)
0	1	0	0	1	1	1	Address DAC C register and loads data (register only)
1	1	0	0	1	1	1	Address DAC D register and loads data (register only)
X	X	X	X	X	0	0	Transfers data from first registers to all DAC's
X	X	1	X	X	X	X	No updated information
X	X	X	1	X	X	X	No updated information

HS 7584 Truth Table 12-Bit Parallel Load

HS 7584 CONTROL INPUTS

A_0	A_1	$\overline{CS}$	$\overline{WR1}$	B1/$\overline{B2}$	$\overline{WR2}$	$\overline{XFER}$	HS 7584 OPERATION DESCRIPTION
0	0	0	0	1	1	1	Address DAC A register and loads data (register only)
0	0	0	0	0	1	1	Address DAC A register and updates lower 4 Bits
1	0	0	0	1	1	1	Address DAC B register and loads data (register only)
1	0	0	0	0	1	1	Address DAC B register and updates lower 4 Bits
0	1	0	0	1	1	1	Address DAC C register and loads data (register only)
0	1	0	0	0	1	1	Address DAC C register and updates lower 4 Bits
1	1	0	0	1	1	1	Address DAC D register and loads data (register only)
1	1	0	0	0	1	1	Address DAC D register and updates lower 4 Bits
X	X	X	X	X	0	0	Transfers data from first registers to all DAC's
X	X	1	X	X	X	X	No updated information
X	X	X	1	X	X	X	No updated information

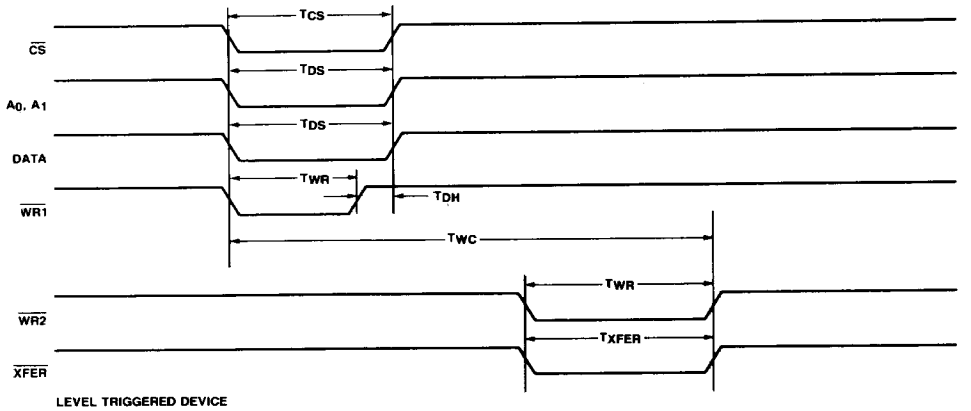
HS 7584 Truth Table 12-Bit Parallel Load

CONTROL FUNCTIONS

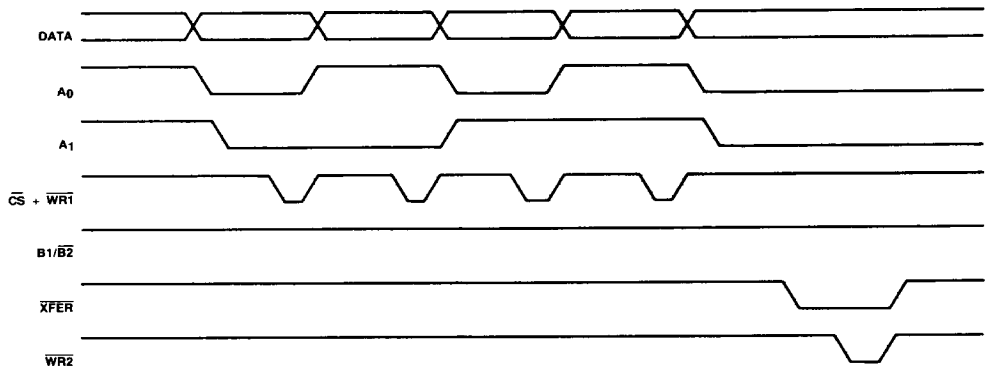
PIN	FUNCTION
A_0	Address 0 for DAC selection
A_1	Address 1 for DAC selection
$\overline{CS}$	Enables DAC input and A_0, A_1 (along with $\overline{WR1}$) for writing (Active low)
$\overline{WR1}$	Enables A_0, A_1 (along with $\overline{CS}$), active low, gated with $\overline{CS}$
B1/$\overline{B2}$	Selects high and low bytes. In 12-Bit mode, B1/$\overline{B2}$ tied high; In 8-Bit mode, a 12-Bit word is loaded into first register when B1/$\overline{B2}$ is high, and a 4-Bit word is updated to the lower bits when B1/$\overline{B2}$ is low.
$\overline{WR2}$	Gated with $\overline{XFER}$, used to load all DAC's simultaneously (Active low)
$\overline{XFER}$	Gated with $\overline{WR2}$, used to load all DAC's simultaneously (Active low)

TIMING CHARACTERISTICS

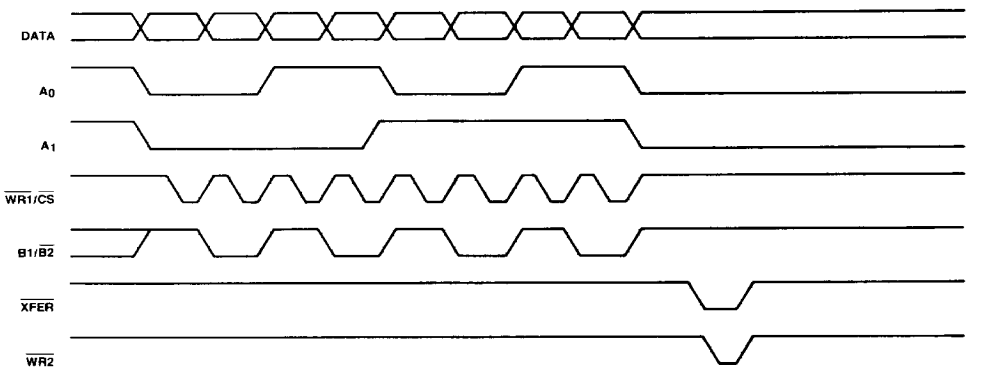
PARAMETER	LIMIT AT T_A = +25°C	LIMIT AT −55°C to +125°C	UNITS	
T_{DS}	100 min	125 min	ns	Data Set Up Time (To rising edge of $\overline{WR1}$ command)
T_{DH}	0 min	0 min	ns	Data Hold Time
T_{WR}	100 min	120 min	ns	Write Pulse Width
T_{CS}	100 min	125 min	ns	Chip Select Width
T_{XFER}	100 min	120 min	ns	Transfer Pulse Width
T_{WC}	200 min	245 min	ns	Total Write Command



Write Cycle Timing Diagram

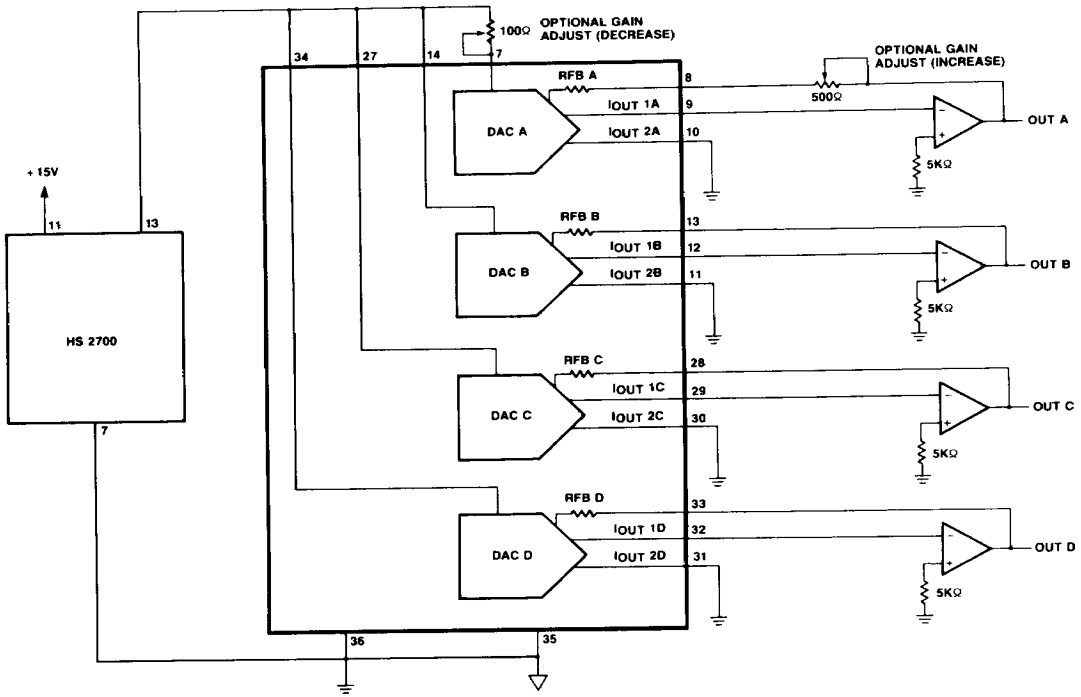


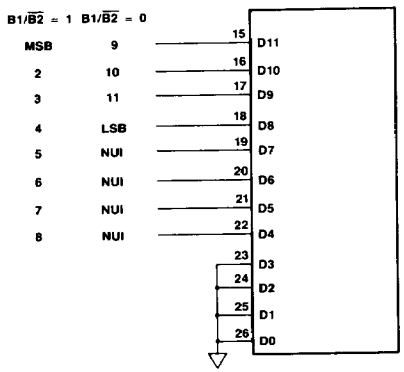
Typical Interface with a 12-Bit Data Bus



Typical Interface with an 8-Bit Data Bus

UNIPOLAR OPERATION





NUI = No Updated information. During the second load cycle, the information on pins 15 thru 18 will be loaded into the lower bits of the first register; information on pins 19 through 22 will not be recognized. Note: Upper 8 bits should be loaded first, then lower bits.

8-Bit Bus Configuration

OFFSET AND GAIN ADJUSTMENT

Offset Adjust. Since the maximum output leakage is 200nA (over temperature range) the offset voltage, due to the DAC, would be ±1.4mV. This, plus any offset's due to the op-amp, could be nulled out by the offset adjust circuit given by the op-amp manufacturer. The 5KΩ resistor, from the positive summing junction to ground, reduces offset voltages due to bias currents of the op-amp. They may be eliminated if cost factors out ways offset demands.

Gain Adjust. The circuit may be modified which would lead the user to adjusting gain. A 100 Ohm trimpot in series between the reference and reference input would allow for a 0 to −1.4% adjustment range in gain. A 500 Ohm trimpot in series with the feedback resistor to output of the op-amp would allow for a 0 to +7% adjustment range.

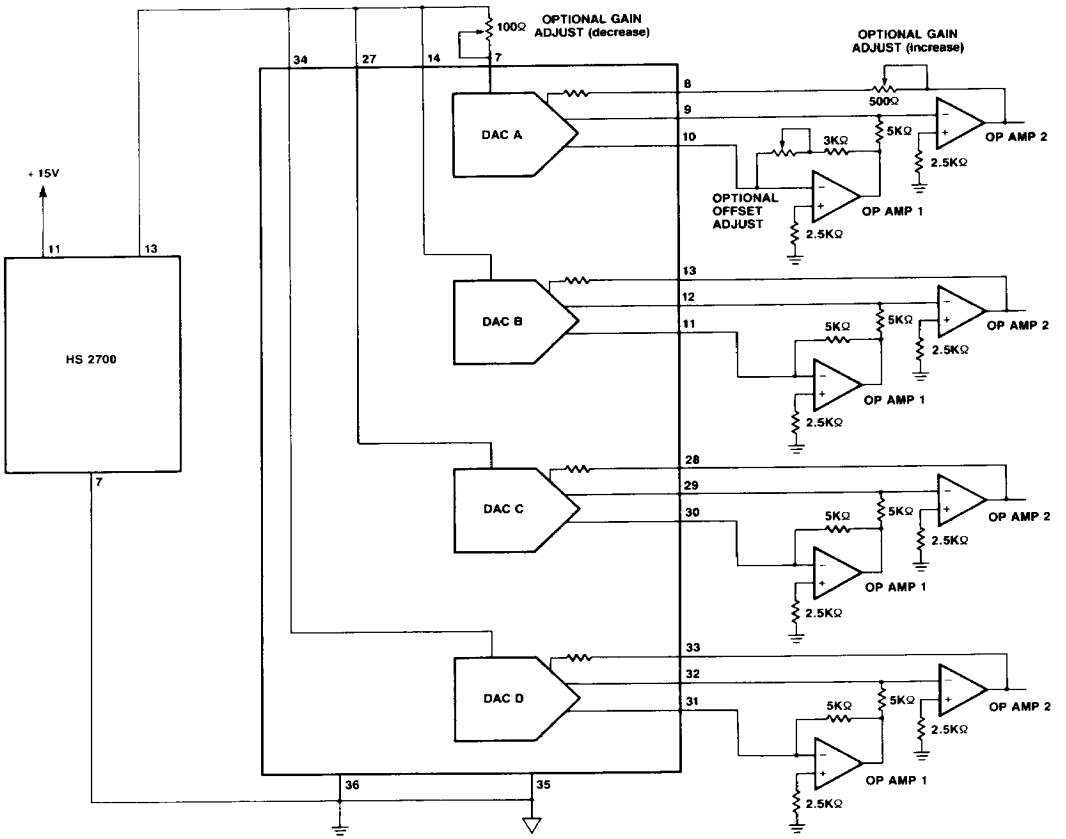
Note: Trimpots reduce stability coefficients given in specifications and should be used only in cases where the specified end point accuracy is not sufficient.

Coding: Straight Binary

INPUT MSB LSB	OUTPUT
0000 0000 0000	0
0000 0000 0001	1 LSB
0111 1111 1111	$-V_{REF}/2$ − 1 LSB
1000 0000 0000	$-V_{REF}/2$
1000 0000 0001	$-V_{REF}/2$ + 1 LSB
1111 1111 1111	$-V_{REF}$ + 1 LSB

$$1\ LSB = \frac{-V_{REF}}{2^{12}}$$

BIPOLAR OPERATION



OFFSET AND GAIN ADJUSTMENT

Offset Adjust. The resistor in feedback loop of the first op-amp can be a 3KΩ resistor in series with a 5KΩ trimpot. This will give enough adjustment range to match the absolute tolerance of the DAC's resistors. Apply a 1 MSB and all 0's code and adjust for 0.000 Volts.

Gain Adjust. The circuit may be modified which would allow the user to adjust gain. 100 Ohm trimpots in series between the reference and reference input would allow for a 0 to −1.4% adjustment range. A 500 Ohm trimpot in series with the feedback resistor of the second op-amp would allow for a 0 to +7% adjustment range.

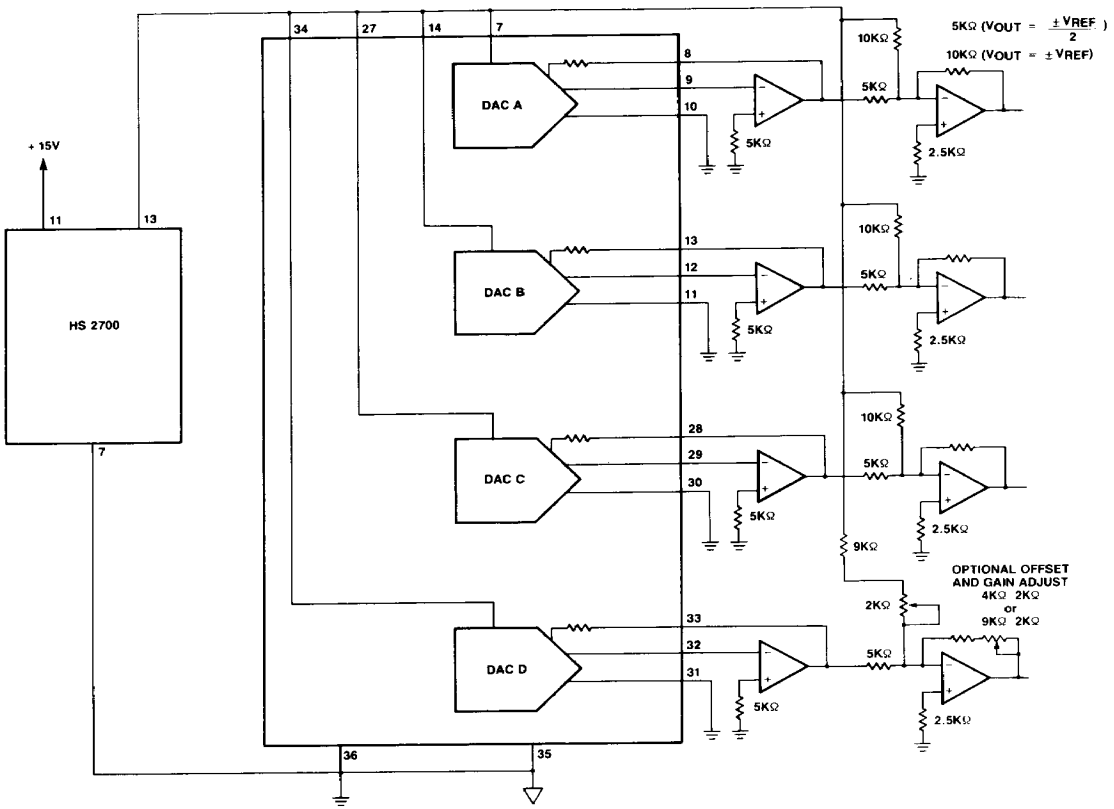
Note: Trimpots reduce stability coefficients given in specifications and should be used only in cases where the specified end point accuracy is critical.

Coding: Complementary Binary

INPUT MSB LSB	OUTPUT
0000 0000 0000	V_{REF}
0000 0000 0001	V_{REF} − 1 LSB
0111 1111 1111	0 − 1 LSB
1000 0000 0000	0
1000 0000 0001	0 + 1 LSB
1111 1111 1111	$-V_{REF}$ − 1 LSB

$$1\ LSB = \frac{V_{REF}}{2^{12}}$$

BIPOLAR OPERATION



OFFSET AND GAIN ADJUSTMENT

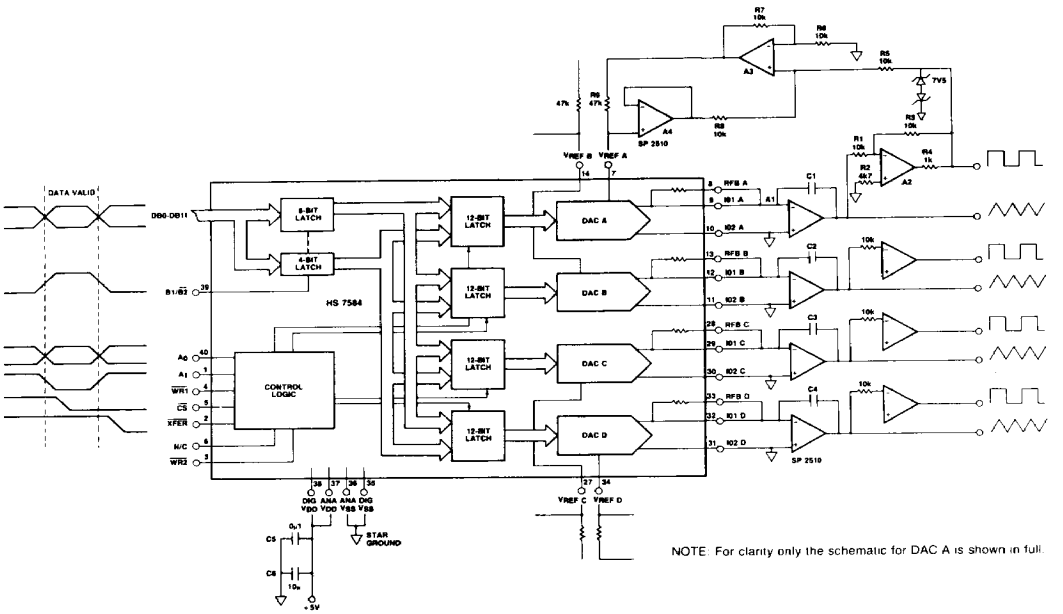
Offset Adjust. The resistor from V_{REF} to the negative summing junction of the second op-amp can be a 9K Ω resistor in series with a 2K Ω trimpot. This will give a ± 10% adjustment range. Apply a 1000 0000 0000 code and adjust for 0.000 Volts.

Gain Adjust. Gain adjust should be performed after offset adjust and is done by utilizing a trimpot in the feedback loop of the second op-amp. Apply all ones digital input code and adjust for $+V_{REF} - 1$ LSB. A 4.0K Ω resistor in series with 2K Ω trimpot will adjust out any errors, for $\pm V_{REF}/2$, or a 9K Ω resistor in series with a 2K Ω trimpot for $\pm V_{REF}$.

Note: Trimpots reduce stability coefficients given in specifications and sould be used only in cases where the specified end point accuracy is not sufficient.

Coding: Straight Binary

INPUT	OUTPUT	
MSB LSB	10KΩ FEEDBACK	5KΩ FEEDBACK
0000 0000 0000	$-V_{REF}$	$-V_{REF}/2$
0000 0000 0001	$-V_{REF} + 1$ LSB	$-V_{REF}/2 + 1$ LSB
0111 1111 1111	0 − 1 LSB	0 − 1 LSB
1000 0000 0000	0	0
1111 1111 1111	$+V_{REF} - 1$ LSB	$+V_{REF}/2 + 1$ LSB
	1 LSB = $\frac{2\,V_{REF}}{2^{12}}$	1 LSB = $\frac{V_{REF}}{2^{12}}$



TRIANGLE/SQUAREWAVE GENERATOR

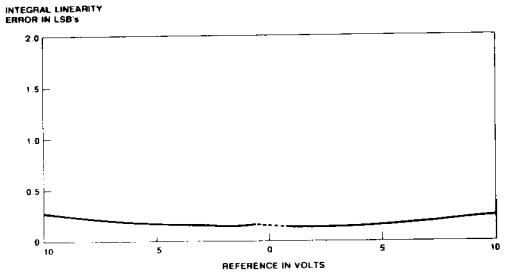
TRIANGLE/SQUAREWAVE GENERATOR

A programmable triangle/squarewave generator can easily be implemented utilizing the HS 7584, providing micropressor control of multiple signal sources.

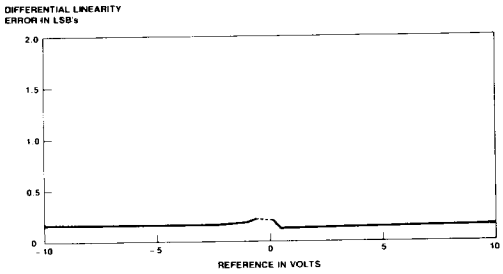
The outputs are derived from an 8-Bit or 12-Bit source determined by the state of B1/$\overline{B2}$. In a 12-Bit system this control line should be tied high. The digitally controlled integrator has a frequency determined by:

$$f = \frac{\text{Digital Input}}{4\,RC}$$

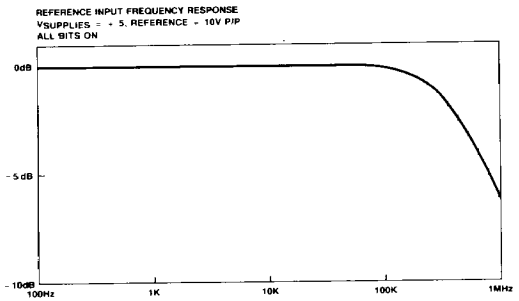
C is the value of C_1 to C_4 and R is the resistance of the DAC. With the four DACs on a single chip the resistance matching is excellent resulting in very stable timing relationships at the generator outputs. The output of the comparator A_2 determines whether the constant current source provided by A_3 and A_4 is positive or negative. The system performance is determined by the selection of the amplifiers A_1, A_2, A_3 and A_4. For good high frequency performance the SP 2510 has been used. The SP 2510 has a slew rate of 65V/ μs and settles to 0.1% of the final output in 0.25 μs.



Integral Linearity Error Vs. Reference Voltage
Typical Results For 5V Supply



Differential Linearity Error Vs. Reference Voltage
Typical Results For 5V Supply



7

ORDERING INFORMATION

MODEL	DESCRIPTION	TEMPERATURE RANGE	PACKAGE	SCREENING
HS 7584C	12-Bit Quad DAC	0 to +70°C	40 Pin DIP	—
HS 7584C/LCC	12-Bit Quad DAC	0 to +70°C	44 Pin LCC	—
HS 7584B	12-Bit Quad DAC	−55°C to +125°C	40 Pin DIP	MIL-STD-883C
HS 7584B/LCC	12-Bit Quad DAC	−55°C to +125°C	44 Pin LCC	MIL-STD-883C
HS 7584C/PLCC	12-Bit Quad DAC	0 to +70°C	44 Pin PLCC	—
HS 7584C/PDIP	12-Bit Quad DAC	0 to +70°C	40 Pin PDIP	—