DDX-4100 Errata

DDX Multichannel Digital Audio Processor

ERRATA

A] When using the sample rate converter (SRC), **it is mandatory to apply a valid input signal to the DDX-4100 prior to unmuting.** Failure to do so will result in large DC offsets applied to speaker outputs which may damage loudspeakers.

To ensure proper operation using the S/PDIF input, be sure to poll the "S/PDIF Status" bit (register 0x77, bit 1 which determines S/PDIF lock) indicating a valid input signal prior to unmuting. Bit 1 will report logic '0' for a valid S/PDIF input signal or logic '1' for an invalid signal. Delay unmuting until after a valid signal is detected.

To ensure proper operation using the serial I2S inputs or AC97, valid clock signals must be applied to DDX-4100 pins 3,4 (LRCKI/SYNC, BICKI/BIT_CLK) prior to unmuting. The "SRC Status" bit (register 0x77, bit 0 which determines SRC lock), does not provide a correct indication prior to receiving a valid input signal. The "SRC Status" bit 0 will indicate SRC lock , logic '0', whether or not valid input signals are applied. Subsequent to receiving a valid input signal, the "SRC Status" bit operates as intended, i.e. removing the input signal will cause an out-of-lock indication.

B] **It is recommended to configure the device using a 24.576MHz crystal**. Be sure the "PLL_Factor" bit in CRA is cleared (Configuration Register A, Subaddress 0x5B, bit 7= '0'). This is the default value following hardware RESET (pin 7) being deasserted or writing to the "Reset Register" (Subaddress 0x00) via I^2C. **The alternate 6.144MHz crystal is not recommended.** When using the 6.144MHz crystal, difficulties have been observed following power-up which may appear as I^2C related. These include unexpected muting or failure to un-mute when commanded, poor S/N ratio which improves after power cycling, or high DC output with no audio. These operational difficulties can be solved by substituting a 24.576MHz crystal and clearing the PLL_Factor.

C] **V_{DD} should be limited to 3.4V maximum for proper operation**.

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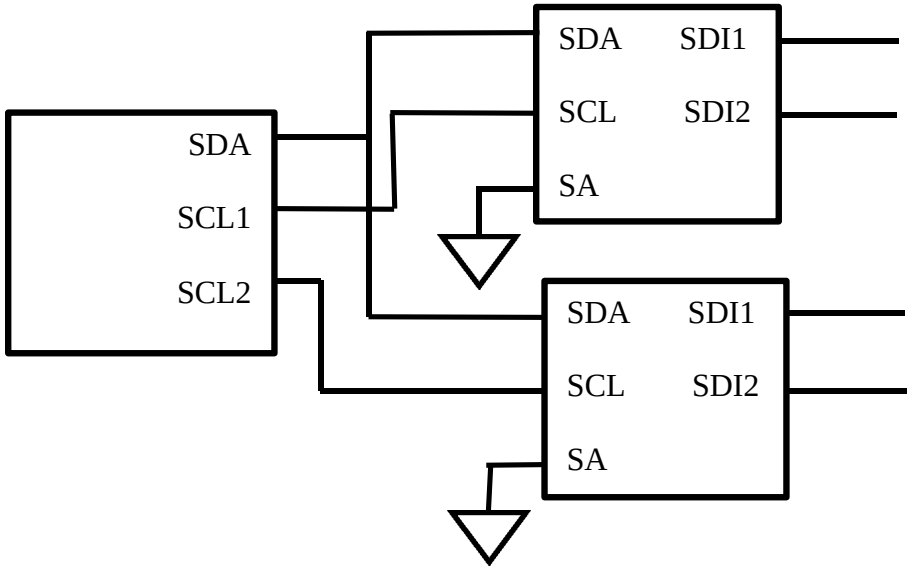
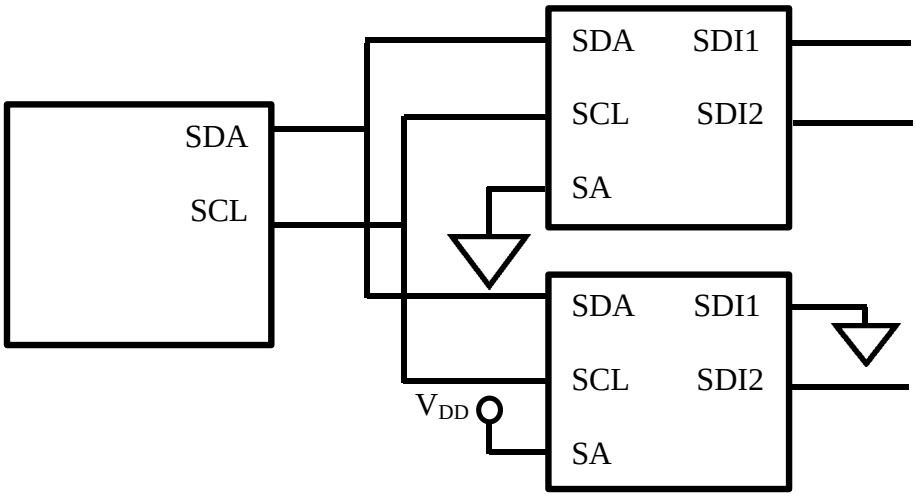
D] When using the DDX-4100 in dual processor configuration, **there is an operational error when using the combination of I^2C address = 0011 111x (SA {pin 11} connected to Vdd) and serial I^2S input SDI1 (pin 1).** The serial data input SDI1 will not operate per the datasheet in this configuration. Using I^2C address = 0011 110x (SA {pin 11} connected to ground) the device operates properly as described in the datasheet. Single processor configurations are not affected by this error, provided the SA pin is connected to ground. There are two choices for a corrective action.

The first choice is to ground SA pin 11 on both ICs, causing both ICs to have the same I^2C address = 0011 110x, and use two separate I^2C clock pins (SCL pin 10) from the system microcontroller, one for each IC, to address the two processors independently. When communicating with the first processor, the SCL signal connected to the second must remain static and vice versa. The advantage is that full functionality is achieved and no other changes are required. The disadvantage is that there is an additional signal required from the system microcontroller.



First Choice: Ground SA on both controllers

The second choice is to ground the SDI1 pin (pin 1) on the DDX-4100 when the SA pin (pin 11) is connected to V_{DD}. This means that you cannot use this input disabling L and R outputs on this device and so only the LS and RS surround outputs will be available.



Second Choice: Ground SA on one controller

For further information please contact Apogee Technology Applications Engineering.