CYPRESS

UltraLogic™ Very High Speed 4K Gate CMOS FPGA

Features

- Very high speed
  - Loadable counter frequencies greater than 150 MHz
  - Chip-to-chip operating frequencies up to 110 MHz
  - Input + logic cell + output delays under 6 ns
- Unparalleled FPGA performance for counters, data path, state machines, arithmetic, and random logic
- High usable density
  - 16 x 24 array of 384 logic cells provides 12,000 total available gates
  - 4,000 typically usable "gate array" gates in 84-pin PLCC, 145-pin CPGA, 100-pin and 144-pin TQFP, and 160-pin CQFP packages
- Fully PCI compliant inputs and outputs
- Low power, high output drive
  - Standby current typically 2 mA
  - 16-bit counter operating at 150 MHz consumes 50 mA
  - Minimum I_{OL} and I_{OH} of 20 mA
- Flexible logic cell architecture
  - Wide fan-in (up to 14 input gates)
  - Multiple outputs in each cell
  - Very low cell propagation delay (1.7 ns typical)
- Powerful design tools—*Warp3*™
  - Designs entered in VHDL, schematics, or both
  - Fast, fully automatic place and route
  - Waveform simulation with back annotated net delays
  - PC and workstation platforms
- Extensive 3rd party tools support
  - See Development Systems section
- Robust routing resources
  - Fully automatic place and route of designs using up to 100 percent of logic resources
  - No hand routing required
- 80 (7C385P) to 114 (7C386P) bidirectional input/output pins
- 6 dedicated input/high-drive pins
- 2 clock/dedicated input pins with fan-out-independent, low-skew nets
  - Clock skew <0.5 ns
- Input hysteresis provides high noise immunity
- Thorough testability
  - Built in scanpath permits 100 percent factory testing of logic and I/O cells
- 0.65μ CMOS process with ViaLink™ programming technology
  - High-speed metal-to-metal link
  - Non-volatile antifuse technology
- 100-pin TQFP is pinout compatible with the 1K (CY7C382P) FPGAs and 2K (CY7C384A) devices
- 84-pin PLCC is pinout compatable with the 2K (CY7C384A) devices
- 144-pin TQFP is pinout compatable with the 8K (CY7C388P) devices

Functional Description

The CY7C385P and CY7C386P are very high speed CMOS user-programmable ASIC (pASIC™) devices. The 384 logic cell field-programmable gate array (FPGA) offers 4,000 typically usable "gate array" gates. This is equivalent to 12,000 EPLD or LCA gates. The CY7C385P is available in a 84-pin PLCC and the 100-pin TQFP packages. The CY7C386P is available in 144-pin TQFP, 145-pin and CPGA and 160-pin CQFP packages.

Low-impedance, metal-to-metal ViaLink interconnect technology provides non-volatile custom logic capable of operating at speeds above 150 MHz with input delays under 1.5 ns and output delays under 3 ns. This permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors.

Designs are entered into the CY7C385P and CY7C386P using Cypress *Warp3* software or one of several third-party tools. See the Development Systems section of the *Programmable Logic Databook* for more tools information. *Warp3* is a sophisticated CAE package that features schematic entry, waveform-based timing simulation, and VHDL design synthesis. The CY7C385P and CY7C386P feature ample on-chip routing channels for fast, fully automatic place and route of high gate utilization designs.

For detailed information about the pASIC380 architecture, see the pASIC380 Family datasheet.

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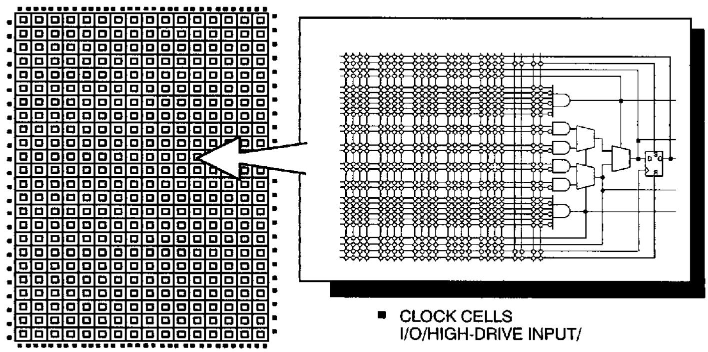
Logic Block Diagram



84, 100, and 144 (145) AND 160 PINS, 114 I/O CELLS, 6 INPUT HIGH DRIVE CELLS, 2 INPUT/CLK (HIGH DRIVE) CELLS 7C385P-1

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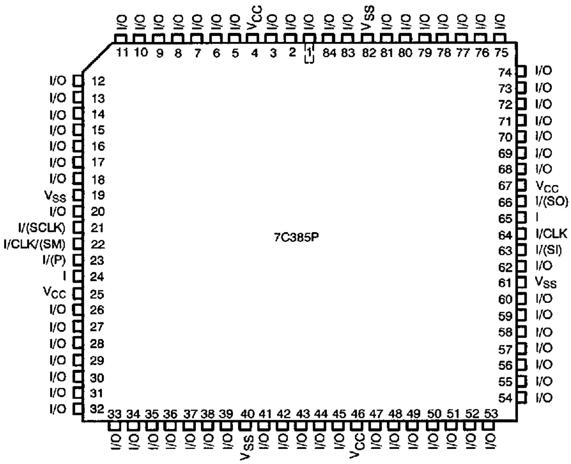
Pin Configurations

PLCC/CLCC
Top View



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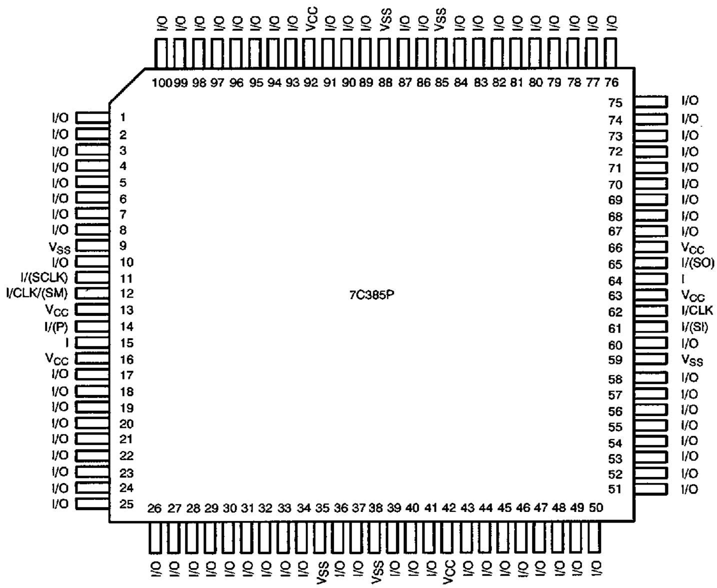
TQFP
Top View



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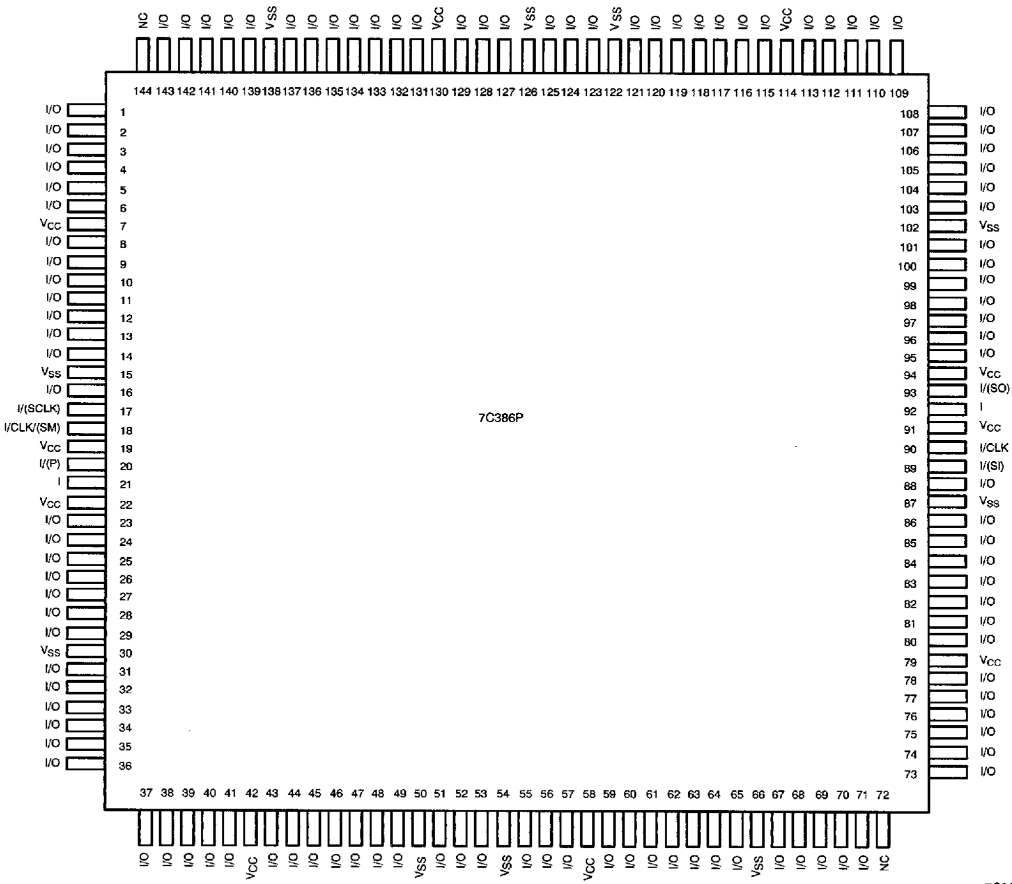
Pin Configurations (continued)

TQFP
Top View



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Pin Configurations (continued)

CPGA
Bottom View

	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
1	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
2	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC	I/O
3	I/O	I/O	V_{SS}	I/O	V_{CC}	I/O	V_{SS}	I/O	V_{CC}	I/O	V_{SS}	I/O	V_{CC}	I/O	I/O
4	I/O	I/O	I/O									■	I/O	I/O	I/O
5	I/O	I/O	V_{CC}										V_{SS}	I/O	I/O
6	I/O	I/O	I/O										I/O	I/O	I/O
7	I	I/(SO)	V_{SS}										V_{CC}	I/O	I/O
8	I/O	I/(SI)	I/CLK					7C386P					I/CLK/(SM)	I/(SCLK)	I/O
9	I/O	I/O	V_{CC}										V_{SS}	I	I/(P)
10	I/O	I/O	I/O										I/O	I/O	I/O
11	I/O	I/O	V_{SS}										V_{CC}	I/O	I/O
12	I/O	I/O	I/O										I/O	I/O	I/O
13	I/O	I/O	V_{CC}	I/O	V_{SS}	I/O	V_{CC}	I/O	V_{SS}	I/O	V_{CC}	I/O	V_{SS}	I/O	I/O
14	I/O	NC	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O

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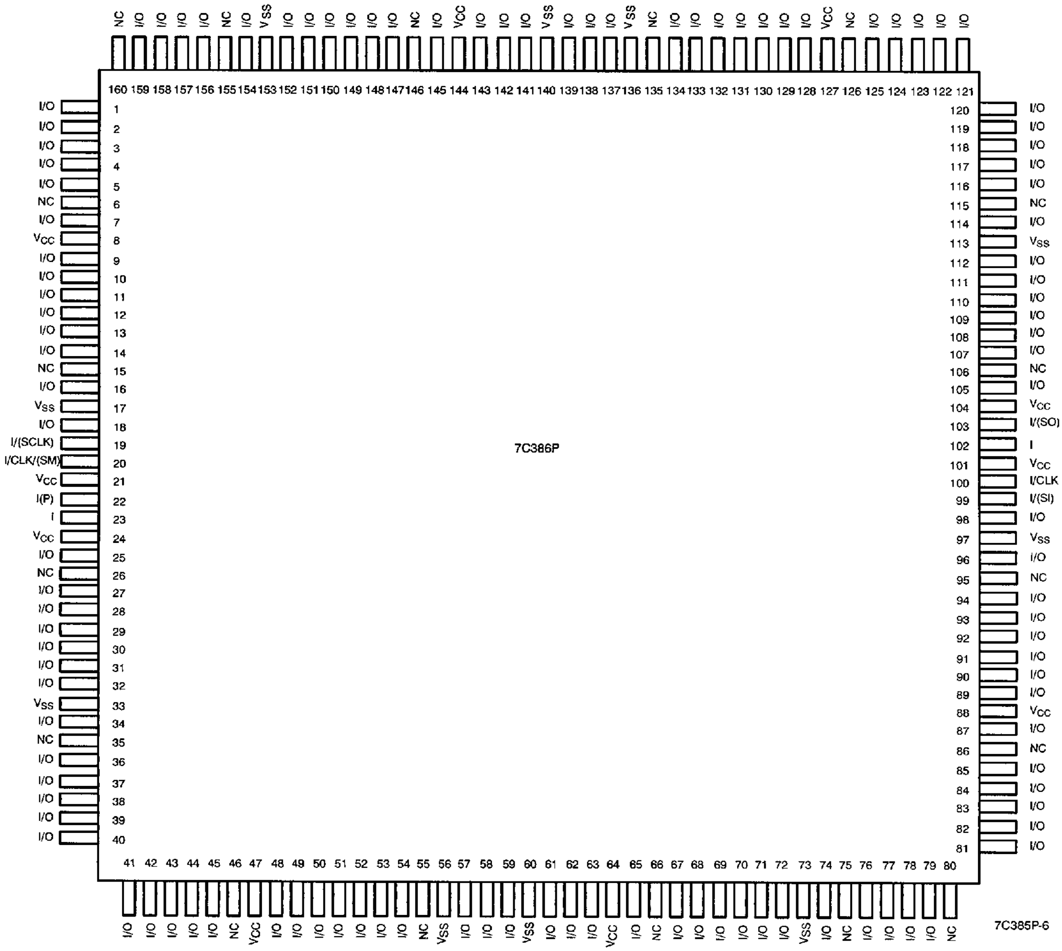
Pin Configurations (continued)

CQFP
Top View



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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature
- Ceramic .... −65°C to +150°C
- Plastic .... −40°C to +125°C

Lead Temperature .... 300°C

Supply Voltage .... −0.5V to +7.0V

Input Voltage .... −0.5V to V_{CC} +0.5V

ESD Pad Protection .... ±2000 V

DC Input Voltage .... −0.5V to 7.0V

DC Input Current .... ±20 mA

Latch-Up Current .... ±200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Industrial	−40°C to +85°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Delay Factor (K)

Speed Grade	Military		Industrial		Commercial	
	Min.	Max.	Min.	Max.	Min.	Max.
−X	0.39	3.00	0.4	2.75	0.46	2.55
−0	0.39	1.82	0.4	1.67	0.46	1.55
−1	0.39	1.56	0.4	1.43	0.46	1.33
−2			0.4	1.35	0.46	1.25

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −4.0 mA	3.7		V
		I_{OH} = −20 mA	2.4		V
		I_{OH} = −10.0 μA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage	I_{OL} = 20 mA		0.4	V
		I_{OL} = 10.0 μA		0.1	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IL}	Input LOW Voltage			0.8	V
I_I	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}	−10	+10	μA
I_{OZ}	Three-State Output Leakage Current	V_{IN} = V_{CC} or V_{SS}	−10	+10	μA
I_{OS}	Output Short Circuit Current[1]	V_{OUT} = V_{SS}	−10	−80	mA
		V_{OUT} = V_{CC}	30	140	mA
I_{CC1}	Standby Supply Current	V_{IN}, $V_{I/O}$ = V_{CC} or V_{SS}		10	mA

Capacitance

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance[2]	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:
1. Only one output at a time. Duration should not exceed 30 seconds.
2. C_I = 45 pF max. on I/(SI) and I/(P).

Switching Characteristics (At V_{CC}=5V, T_A=25°C, K=1)

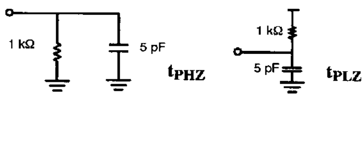
Parameter	Description	Propagation Delays[3] with Fanout of 1	2	3	4	8	Unit
LOGIC CELLS							
t_{PD}	Combinatorial Delay[4]	1.7	2.2	2.6	3.2	5.3	ns
t_{SU}	Set-Up Time[4]	2.1	2.1	2.1	2.1	2.1	ns
t_H	Hold Time	0.0	0.0	0.0	0.0	0.0	ns
t_{CLK}	Clock to Q Delay	1.0	1.5	1.9	2.6	4.7	ns
t_{CWHI}	Clock HIGH Time	2.0	2.0	2.0	2.0	2.0	ns
t_{CWLO}	Clock LOW Time	2.0	2.0	2.0	2.0	2.0	ns
t_{SET}	Set Delay	1.7	2.2	2.6	3.2	5.3	ns
t_{RESET}	Reset Delay	1.5	1.9	2.2	2.7	4.4	ns
t_{SW}	Set Width	1.9	1.9	1.9	1.9	1.9	ns
t_{RW}	Reset Width	1.8	1.8	1.8	1.8	1.8	ns

Parameter	Description	Propagation Delays[3] 1	2	3	4	8	12	Unit
INPUT CELLS								
t_{IN}	Input Delay (HIGH Drive)	2.8	2.9	3.0	3.1	4.0	5.3	ns
t_{INI}	Input, Inverting Delay (HIGH Drive)	3.0	3.1	3.2	3.3	4.1	5.7	ns
t_{IO}	Input Delay (Bidirectional Pad)	1.4	1.9	2.2	2.9	4.7	6.5	ns
t_{GCK}	Clock Buffer Delay[5]	2.7	2.8	2.9	3.0	3.1	3.3	ns
t_{GCKHI}	Clock Buffer Min. HIGH[5]	2.0	2.0	2.0	2.0	2.0	2.0	ns
t_{GCKLO}	Clock Buffer Min. LOW[5]	2.0	2.0	2.0	2.0	2.0	2.0	ns

Parameter	Description	Propagation Delays[3] with Output Load Capacitance (pF) of 30	50	75	100	150	Unit
OUTPUT CELLS							
t_{OUTLH}	Output Delay LOW to HIGH	2.7	3.4	4.2	5.0	6.7	ns
t_{OUTHL}	Output Delay HIGH to LOW	2.8	3.7	4.7	5.6	7.6	ns
t_{PZH}	Output Delay Three-State to HIGH	4.0	4.9	6.1	7.3	9.7	ns
t_{PZL}	Output Delay Three-State to LOW	3.6	4.2	5.0	5.8	7.3	ns
t_{PHZ}	Output Delay HIGH to Three-State[6]	2.9					ns
t_{PLZ}	Output Delay LOW to Three-State[6]	3.3					ns

Notes:

3. Worst-case propagation delay times over process variation at V_{CC} = 5.0V and T_A = 25°C. Multiply by the appropriate delay factor, K, for speed grade to get worst-case parameters over full V_{CC} and temperature range as specified in the operating range. All inputs are TTL with 3-ns linear transition time between 0 and 3 volts.
4. These limits are derived from worst-case values for a representative selection of the slowest paths through the pASIC380 logic cell including net delays. Guaranteed delay values for specific paths should be determined from simulation results.
5. Clock buffer fanout refers to the maximum number of flip-flops per half column. The number of half columns used does not affect clock buffer delay.
6. The following loads are used for t_{PXZ}:

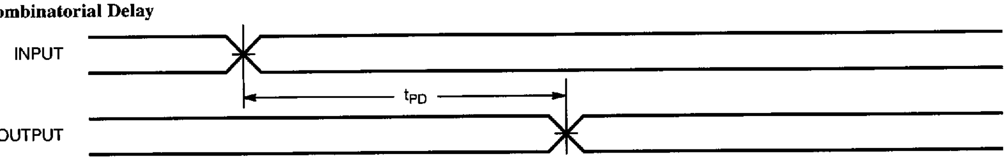


High Drive Buffer

Parameter	Description	# High Drives Wired Together	Propagation Delays[3] with Fanout of 12	24	48	72	96	Unit
t_{IN}	High Drive Input Delay	1	5.3	6.7				ns
		2		4.5	6.6			ns
		3			5.3	6.2	7.2	ns
		4				5.4	6.2	ns
t_{INI}	High Drive Input, Inverting Delay	1	5.7	7.2				ns
		2		4.6	6.8			ns
		3			5.5	6.4	7.4	ns
		4				5.6	6.4	ns

Switching Waveforms

Combinatorial Delay



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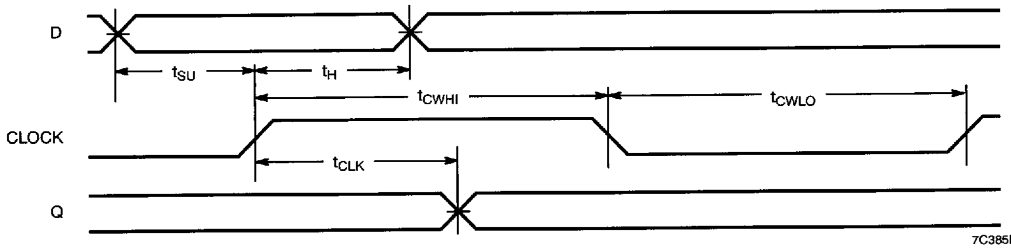
Set-Up and Hold Times



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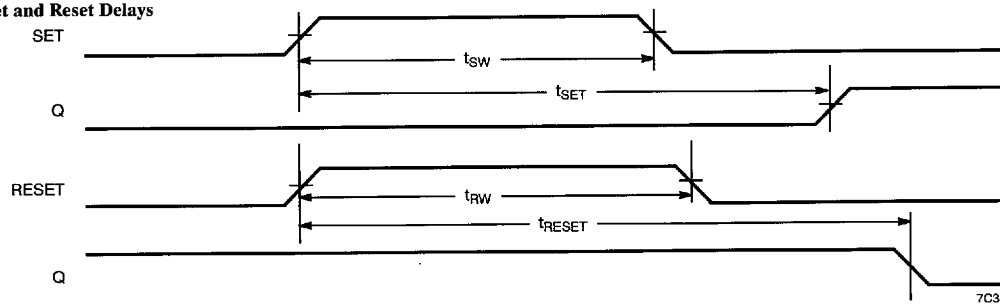
Set and Reset Delays



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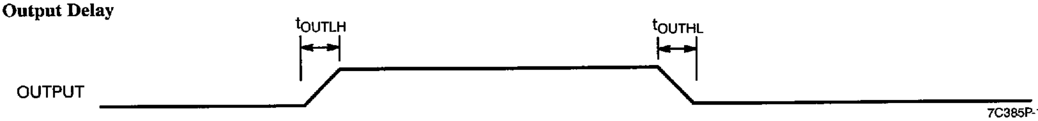
Output Delay



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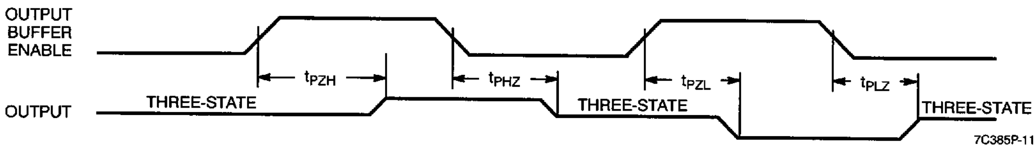
Switching Waveforms (continued)

Three-State Delay



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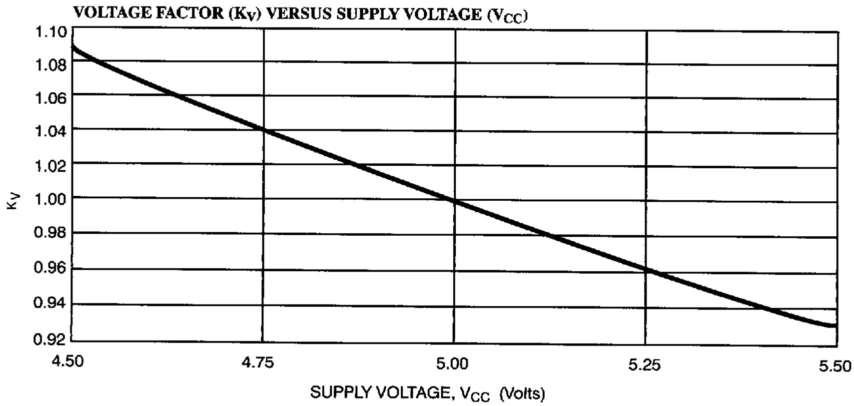
Typical AC Characteristics

Propagation delays depend on routing, fanout, load capacitance, supply voltage, junction temperature, and process variation. The AC Characteristics are a design guide to provide initial timing estimates at nominal conditions. Worst-case estimates are obtained when nominal propagation delays are multiplied by the appropriate Delay Factor, K, as specified by the speed grade in the Delay Factor table. The effects of voltage and temperature variation are illustrated in the graphs below. The *Warp3* Delay Modeler extracts specific timing parameters for precise simulation results following place and route.



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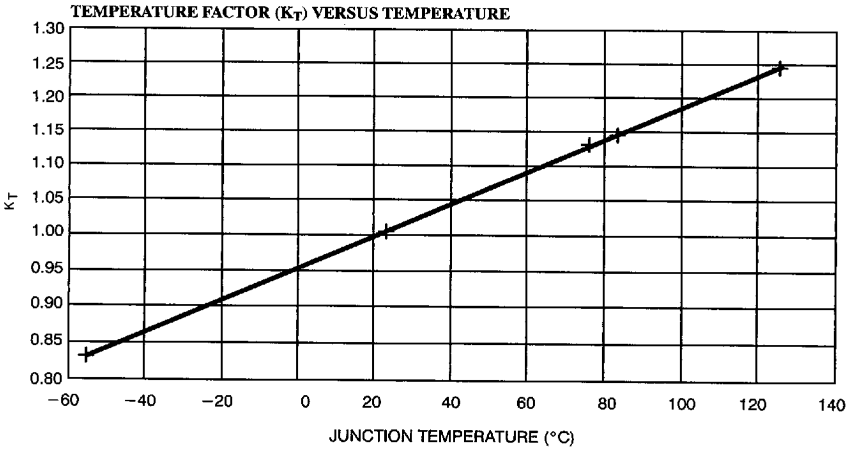

*THETA JA = 45 °C/WATT FOR PLCC

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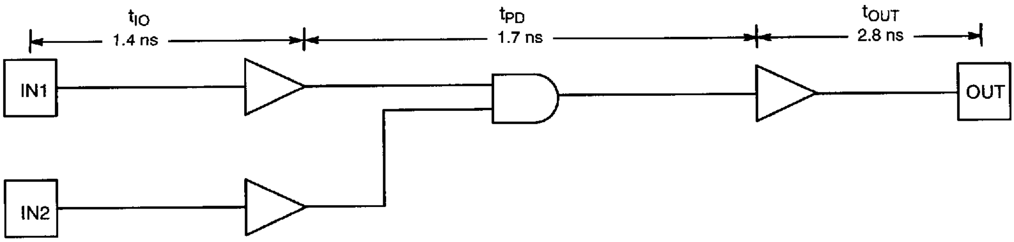
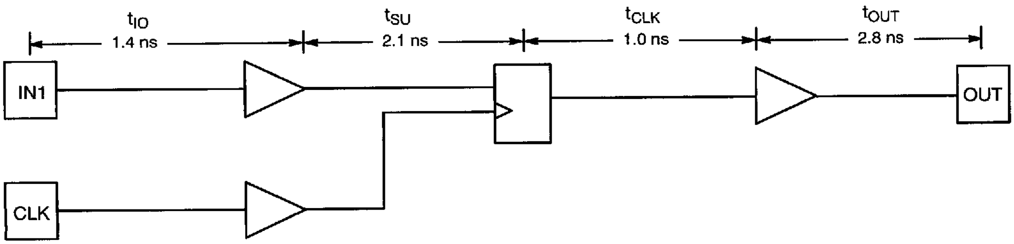
Combinatorial Delay Example (Load = 30 pF, K=1, Fanout=1)



INPUT DELAY + COMBINATORIAL DELAY + OUTPUT DELAY = 5.9 ns

Sequential Delay Example (Load = 30 pF, K=1, Fanout=1)



INPUT DELAY + REG SET-UP + CLOCK TO Q DELAY + OUTPUT DELAY = 7.3 ns

Ordering Information

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
2	CY7C385P–2AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C385P–2JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C385P–2AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C385P–2JI	J83	84-Lead Plastic Leaded Chip Carrier	
1	CY7C385P–1AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C385P–1JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C385P–1AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C385P–1JI	J83	84-Lead Plastic Leaded Chip Carrier	
0	CY7C385P–0AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C385P–0JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C385P–0AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C385P–0JI	J83	84-Lead Plastic Leaded Chip Carrier	
X	CY7C385P–XAC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C385P–XJC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C385P–XAI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C385P–XJI	J83	84-Lead Plastic Leaded Chip Carrier	

Speed Grade	Ordering Code	Package Name	Package Type	Operating Range
2	CY7C386P–2AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C386P–2AI	A144	144-Pin Thin Quad Flat Pack	Industrial
1	CY7C386P–1AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C386P–1AI	A144	144-Pin Thin Quad Flat Pack	Industrial
	CY7C386P–1GMB	G145	145-Pin Grid Array (Cavity Up)	Military
	CY7C386P–1UMB[7]	U160	160-Lead Ceramic Quad Flatpack (Cavity Up)	
0	CY7C386P–0AC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C386P–0AI	A144	144-Pin Thin Quad Flat Pack	Industrial
	CY7C386P–0GMB	G145	145-Pin Grid Array (Cavity Up)	Military
	CY7C386P–0UMB[7]	U160	160-Lead Ceramic Quad Flatpack (Cavity Up)	
X	CY7C386P–XAC	A144	144-Pin Thin Quad Flat Pack	Commercial
	CY7C386P–XAI	A144	144-Pin Thin Quad Flat Pack	Industrial
	CY7C386P–XGMB	G145	145-Pin Grid Array (Cavity Up)	Military
	CY7C386P–XUMB[7]	U160	160-Lead Ceramic Quad Flatpack (Cavity Up)	

Shaded area contains preliminary information.

Note:
7. Shipped in molded carrier ring. Contact local sales office for information on trim and form.

Military Specifications
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC1}	1, 2, 3
I_I	1, 2, 3

Switching Characteristics

Parameters	Subgroups
Delay Factor (K)	7, 8, 9, 10, 11

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