- Performance analysis tools
- Traffic scripting tools

- **C-Ware Development System**
  - Compact PCI chassis
  - PowerPC-based host application module
  - One or more C-5 Switching Modules
  - Various Physical Interface Modules (OC-3, OC-12, OC-48, Gigabit Ethernet, Ethernet/OC-3 combination, and so on)
  - Support for Fabric and other coprocessor modules
  - Complete hardware reference designs

Another aspect of the development environment is the comprehensive customer support from C-Port, which includes hands-on training and Web access for all your support needs at www.cportcorp.com.

Universal Networking Applications

The C-5 NP can support a wide breadth of applications from access to edge to core, such as:

- Multiservice Access Platforms (MSAPs)
- Digital Subscriber Line Access Multiplexor (DSLAM)
- Cable and wireless head-end systems
- MAN CPE and head-end equipment
- Ethernet/IP/Frame Relay/ATM interworking
- Internet access switch/routers
- Load balancing web server switches
- Optical edge switch/routers and add/drop multiplexors
- IP Gigabit/Terabit routers
- WAN Customer Premises Equipment (CPE)

The following sections provide examples of three applications using the C-5 NP.

Example 1: Optical Ec

The new breed of sv
designed for edge "r
networks often supp
the core protocols, F
access protocol, and
to implement the en
dard. Each of these p
supported across a r
types ranging from c
links, SONET OC-3/C
100 and Gigabit Ethe
addition to the basic
face types, these sw
provide advanced ne
as IP Quality of Serv
Private Networks (VP
firewalls.

This broad combinat
interfaces, and servi
difficult challenge to
vendors, especially i
market constraints. T
approaches require
separate hardware
design efforts, each
balancing a mix of
ASICs, Application
Specific Standard
Products (ASSPs),
and general-purpose
CPUs for each inter-
face type and
protocol.

A system design
delivering the proto-
cols and interfaces
needed by this

C-5 Network Processor

Overview

The C-5™ Network Processor (NP), the first member of the C-Port™ family of network processors, is specially designed for networking applications. Its high-level of programmability and wire-speed performance make it the best foundation for building networking products and services.

The C-5 NP incorporates an unprecedented combination of functionality, computing power, and data bandwidth in a flexible, patent-pending architecture. This architecture supports complete programmability from Layer 2 through Layer 7 of the OSI model, allowing the C-5 NP to be used in a wide range of networking applications. In addition, the C-5 NP's simple programming model and advanced development tools enable you to get to market sooner with clearly differentiated products.

Cell and packet processing, table lookup processing, and queue management

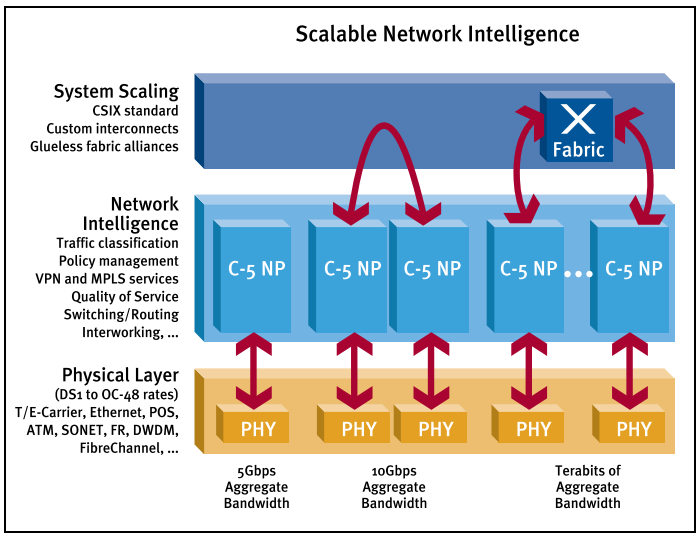
functions are all inte
C-5 NP architecture.
physical interfaces, n
circuit/routing tables
descriptor queues), a
logic, the C-5 NP car
implement intelligen
mixed media, multip
switches and routers

Stable programming
complete developme
and third-party suppo
ola's Smart Network
to a fully integrated p
that can solve a wide
cations tasks and sir
ment of full-featured
applications.

Programmability and

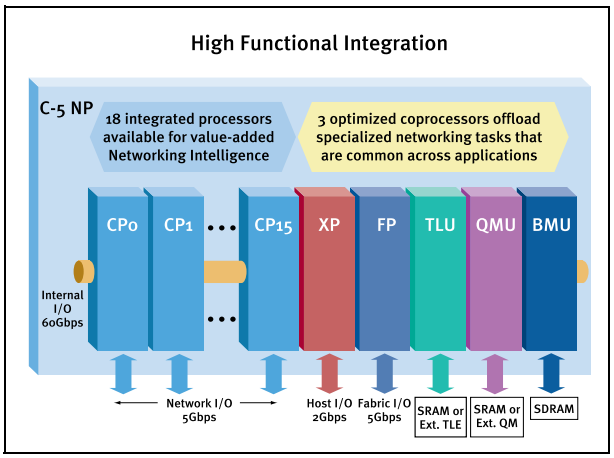
The C-5 NP provides
plane intelligence for
networking products
variety of networking
traffic classification a
ment in addition to s
and interworking fun
networking services
and deployed efficien
under software cont

Each C-5 NP provide
bandwidth and more
computing power to



and tomorrow's demanding communications requirements. The C-5 NP's 5Gbps of bandwidth gives you non-blocking throughput and the 3,000 MIPs of computing power allows you to add services throughout the protocol stack — all at wire-speed.

You can use more than one C-5 NP per device to increase both your bandwidth and computing power. In addition, multiple C-5 NPs can be used in conjunction with a switching fabric to implement large scale switching systems. With two C-5 NPs, you can scale your system up to 10Gbps aggregate bandwidth. By adding multiple C-5 NPs and a fabric interface, you can achieve Terabits per second of



mon networking-spe
architecture allows t
coprocessors to sup
cessing, which helps
deliver software flexi
speeds.

The C-5 NP's sixteer
Channel Processors (
for receiving, proces
ting cells and packet
coprocessors operat
resources for the CPs
perform a range of n
tasks. The coproces

- **Executive Processo** the C-5 NP, and co C-5 NP and externa
- **Fabric** scaling industr
- **Table L** implen table s update
- **Queue (QMU)** queue ageme
- **Buffer (BMU)** flexible ment

Powerful, Intelligent Processing Engines

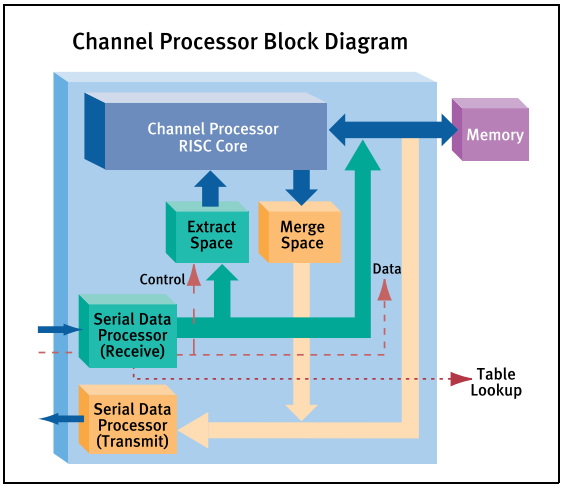
Each Channel Processor (CP) contains a RISC Core *plus* dual parallel Serial Data Processors (SDPs). Together these components act as powerful communications building blocks that can be customized through standard software and that enable more than three billion RISC cycles per second to be used for value-added services. Cell and packet processing is pipelined using special-purpose memories that loosely couple these processors.

Specific forwarding functions supporting different wire-speed network interfaces, line speeds, and protocols are implemented using the C/C++ programmable RISC Core. The RISC Core specifically manages:

- Characterization and classification
- Policy enforcement
- Traffic scheduling

The programmable SDPs handle common, time-consuming tasks such as:

- Programmable field parsing, extraction (including header validation), insertion, and deletion
- CRC validation/calculation
- Framing and encoding/decoding



Flexible, Lower Cost I Interfaces

The C-5 NP's architec supports a variety of standard serial and p cols and individual p from DS1 (1544Mbp Integrated functions MACs and SONET Fr system developmen device design, and lo system costs.

The physical interfac NP are programmed basis, enabling a sing simultaneously supp of physical interface

Simple Programming

The C-5 NP is progra dard C/C++ language figurable state-mach languages, thus prov ple programming mo C-5 NP's standard RI enhances code porta use of standard deve

The key to a simple p however, is an open gramming int C-Ware Applic ming Interfac simplify comm ware develop leverage the p

Similar to API world, the C-V sophisticated NP and abstra mon network

or even mixed within a card for per-port service provisioning by the service provider customer. You basically change the 'personality' of the C-5 NP by downloading a new program.

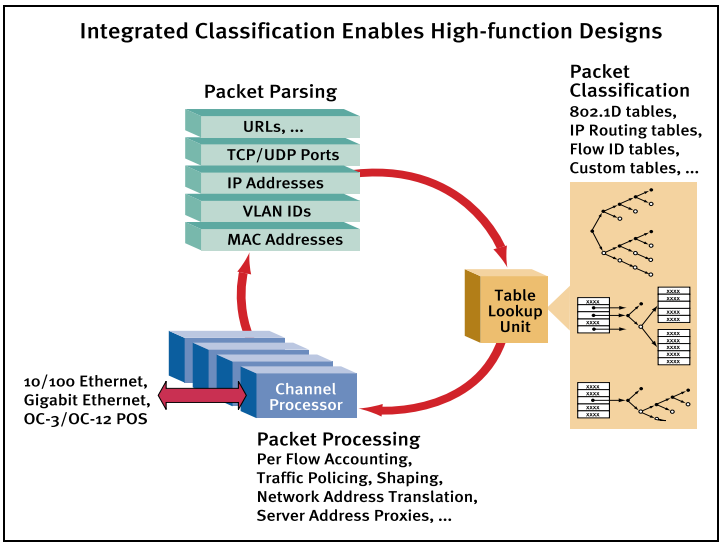
In addition, you can connect these line cards through best-in-class switching fabrics from members of Motorola's Smart Networks Alliance, such as Power X Networks™ and IBM™. The C-5 NP has a glueless interface to both the Power X TeraChannel® Switch Fabric and the IBM Packet Routing Switch Fabric, in addition to conforming to standard Utopia 2 and 3 interfaces.

Thus, one basic hardware design, matched with many different PHY interfaces, yields a vast range of different solutions leveraging a common platform. By using the C-5 NP's universality, a multi-year phased product delivery can be radically condensed, offering a massive time-to-market competitive advantage.

Example 2: High Func
IP Switch

As enterprise netwo
dated on IP, the desi
gent Ethernet switch
functions (such as se
firewalling, accountin
tion, and specific Qo
These Layer 3 throug
capabilities have bec
number of enterprise
working applications

While the intellectua
implementing these
in the system softwa
packet parsing, class
cessing tasks have r
dors to choose betw
or complex hardware
piece-part ASSPs or
a result, many netwo
had difficulty meetin
demands for perform
to new functionality



For more information about the C-Ware Software Toolset, please contact your local Motorola sales representative or call (800) 521-6274. You can also visit Motorola's Smart Networks Web site at:

www.motorola.com/smartnetworks

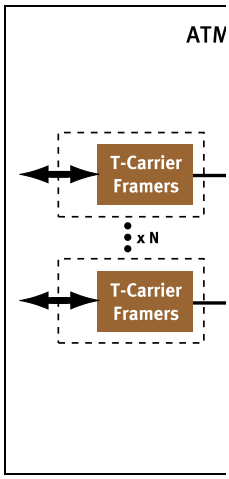
These designs face a number of limitations:

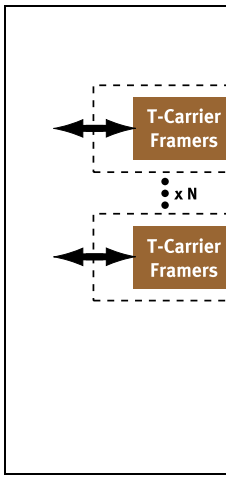
- Frame processing is limited by the CPU performance. A generous estimate of top-end performance for Frame Relay or IP is up to 350,000 frames per second (though typically far worse), which is approximately one-third of wire-speed performance for one DS3 (assuming 8-byte Frame Relay frames).
- Density is limited by processing performance, PCI bandwidth, and component board space. A generous best-case design might support up to five DS3s.
- System cost is driven by the ASSP costs, with complex HDLC controllers and OC-12 SARs typically costing hundreds of dollars for each part.

The C-5 NP breaks through these limitations by integrating these functions into a single chip. Channel Processors are dedicated to ATM, SAR, HDLC multiplexing and demultiplexing, Frame Relay, and IP functions, enabling wire-speed operations.

The C-5 NP implementation offers clear benefits:

- Density of up to 10 DS3s is easily achieved, enabled by the processing power, internal bandwidth, and integration of a single C-5 NP.
- Wire-speed performance can be achieved even for 10 individual DS3 links (over 7 million frames per second), delivering over 20 times the performance of general-purpose CPU-based designs.
- System costs are dramatically reduced, both through integration of multiple, expensive components and provision of much higher port densities.
- The same hardware and software architecture scales to higher speeds, up to OC-48, enabling extensive leverage across the product line for improved time-to-market and lower support costs.





Summary

The C-5 NP is a revo
through for networki
customers. Its uniqu
complete programm
speed performance
foundation for buildi
networking products
the 21st century.

C-5 NP Feature Highlights

Feature	Function	
C-5 NP General	Concurrent Network Processing	• 16 Channel Processors fo processing • Five coprocessors for net tasks: - Executive Processor (s - Fabric Processor (high- interface management) - Table Lookup Unit (net - Queue Management U - Buffer Management Un
	Throughput	• 5Gbps aggregate
	Internal Bandwidth	• Three internal buses with bandwidth
	Processing Power	• Over 3000 MIPS
	Layout	• Single Chip System • Ball Grid Array (BGA) pack
Channel Processor (CP)	Physical Interfaces	• Up to 16 (user configurabl
	Physical protocols supported	• 10Mb Ethernet (RMII) • 100Mb Ethernet (RMII) • 1Gb Ethernet (GMII and T • OC-3c • OC-12/OC-12c • OC-48 • FibreChannel • T1/E1 (with external frame • T3/E3 (with external frame
	RISC Core	• 32-bit C/C++ programmab instruction set
	Programmable Serial Data Processors (SDPs)	• Two SDPs (one receive an CP
Executive Processor (XP)	RISC Core	• C/C++ programmable, sta set
	External Interfaces	• 32-bit, 33/66MHz PCI • Serial PROM interface • Two-wire serial bus interfa
Fabric Processor (FP)	Interface Type	• Conforms to UTOPIA (Lev interface standards, and s compatibility with Power X
	Interface Bandwidth	• Transmit and receive full-d 3200Mbps each direction
Table Lookup Unit (TLU)	Number of Lookups per Second	• 133M maximum
	External Memory Size	• Up to 16MB maximum (8
Queue Management Unit (QMU)	Internal Mode	• Up to 512 queues • Automated multicast elab
Buffer Management Unit (BMU)	Buffer Memory Width	• 139 bit (128 bits data, 9 bi control)
	Buffer Memory Size	• Up to 128MB