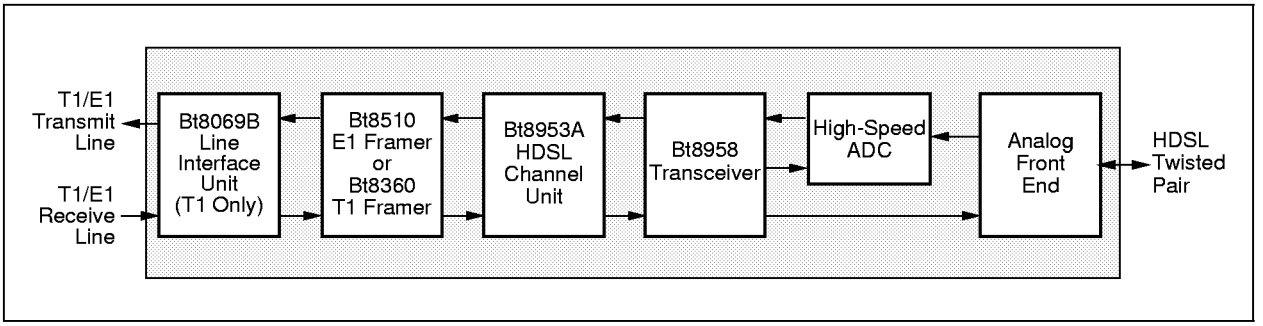
Overview

System Overview

The Bt8958 single-pair HDSL transceiver is an integral component of Brooktree's High-Bit-Rate Digital Subscriber Line (HDSL) product line. When combined with other members of the product-line family, transmission systems conforming to proposed ETSI and ANSI single-pair HDSL standards may be realized. The major building blocks of a single-pair HDSL terminal are shown in Figure 1.

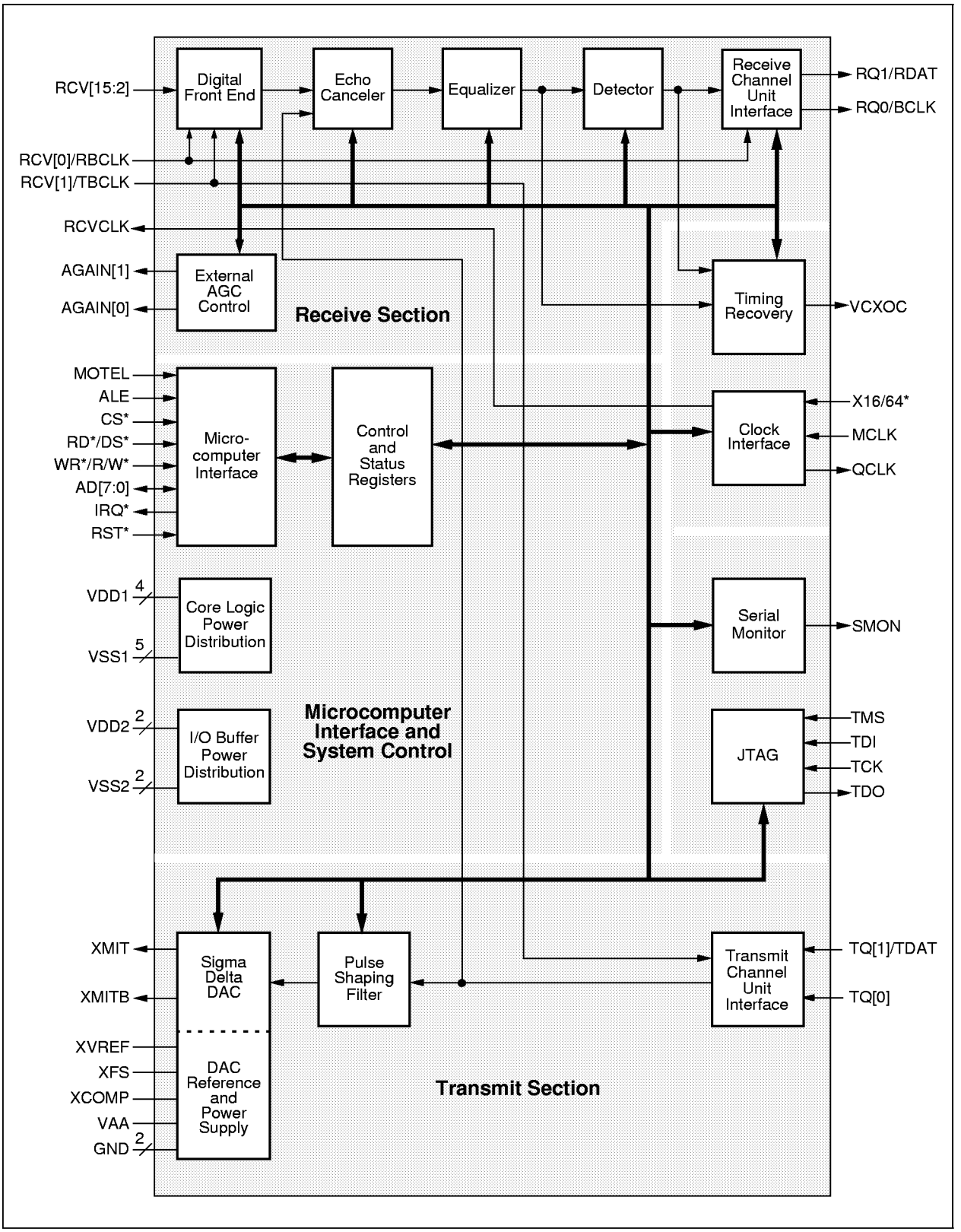
Figure 1. ETSI/ANSI Single-Pair HDSL Terminal



The Analog Front End (AFE) circuitry performs line isolation, amplification, and filtering functions on the 2B1Q-encoded transmit and receive signals in the analog domain. Received symbols are converted to the digital domain by a high-speed Analog-to-Digital Converter (ADC). The Bt8958 receive section performs adaptive echo cancellation, equalization, symbol quantization, and clock recovery on the receive signal. The transmit section performs pulse shaping and Digital-to-Analog Conversion (DAC) on the encoded output waveform. The Bt8953A Channel Unit is responsible for HDSL framing and overhead functions, as well as rate equalization between the single HDSL channel and the primary-rate T1/E1 data stream.

The Bt8958 comprises six major functions: a transmit section, a receive section, timers and meters, a microcomputer interface, a timing recovery and clock interface, and a test and diagnostic interface. Each of these blocks is described briefly in this chapter. Connections within and between each of these functions are illustrated in the block diagram in Figure 2.

Figure 2. Block Diagram



Transmit Section

The source of transmitted symbols is programmable through the microcomputer interface. The primary choices include external 2B1Q-encoded data present at pins TQ[1,0]/TDAT of the channel unit interface, internally looped-back receive symbols from the detector, or a constant "all ones" source. The symbols are then optionally scrambled. A Finite Impulse Response (FIR) digital filter provides pulse shaping prior to (DAC) where a 64 times oversampled sigma-delta DAC sources complementary current-mode outputs.

Receive Section

Receive data is input in offset binary form from an external ADC where each sample is then converted to two's complement format. After DC offset cancellation, a replica of the transmit signal is subtracted from the total receive signal by a digital echo canceler. The resultant far-end signal is then conditioned by an equalization stage consisting of automatic gain control, a feed-forward equalizer, a decision-feedback equalizer, and an error predictor. A mode-dependant detector is then used to recover the 2B1Q-encoded data from the equalized signal. The channel unit interface then provides an optional descrambling function followed by parallel or serial output of the sign and magnitude bits on pins RQ1,0/RDAT. A number of meters are implemented within the receiver to provide average level indications at various points in the receive signal path. The receive section also performs far-end signal clock recovery through an on-chip Phase Lock Loop (PLL) circuit formed with an external Voltage-Controlled Crystal Oscillator (VCXO).

Timers and Meters

Eight 16-bit timers and 10 measurement meters are integrated into the transceiver. The timers support various metering functions within the receiver section, and offload the external microcomputer from complex timing operations associated with ETSI- and ANSI-compliant startup procedures. Four timers are allocated for startup support, two for meter timing, and two for general purpose use. Control and monitoring access to the timers and meters is provided through the microcomputer interface.

Timing Recovery and Clock Interface

The master clock input to the transceiver must run at either 16 times or 64 times the desired symbol rate of the transceiver, depending upon the symbol rate and the position of the X16/64* pin. A fixed crystal oscillator may be used for this source when the transceiver is used exclusively in an exchange or central-office terminal application. For customer or remote terminal applications, or selectable central office/remote terminal applications, a VCXO must be used. In these applications, the control voltage for the VCXO is provided through the VCXOC output pin by an internal timing recovery module.

Microcomputer Interface

The Microcomputer Interface (MCI) uses a multiplexed address/data bus to provide access to a 256-byte address space within the transceiver. A combination of direct and indirect addressing methods access all internal locations. A MOTEL control pin configures the bus-interface control/handshake lines to conform to common Motorola/Intel conventions. Little-endian data formatting (least significant byte of a multibyte word stored at the lowest byte-address location) is used in all cases, regardless of MOTEL pin selection. An interrupt request output pin (IRQ*) supports low-latency responses to time-critical event occurrences within the transceiver.

Test and Diagnostic Interface

The test and diagnostic interface comprises a test access port and a serial monitor (SMON) output. The test access port conforms to IEEE Std 1149.1-1990, IEEE Standard Test Access Port and Boundary Scan Architecture. Also referred to as JTAG (Joint Test Action Group), this interface provides direct serial access to each of the transceivers I/O pins. This capability can be used during in-circuit board test to increase the testability and reduce the cost of the in-circuit test process.

The serial monitor output can be viewed as a real-time virtual probe for looking at the transceiver's internal signals. The programmable signal source is shifted out serially at 16 times the symbol rate. Much of the receive signal path is accessible through this output.

Pin Descriptions

The Bt8958 is packaged in a 68-Pin Plastic Leaded Chip Carrier (PLCC). Figure 3 and Figure 4 illustrate the pinout and logic diagrams, respectively. Table 1 lists the pin labels, signal names, input/output functions, and descriptions.

Figure 3. Pinout Diagram

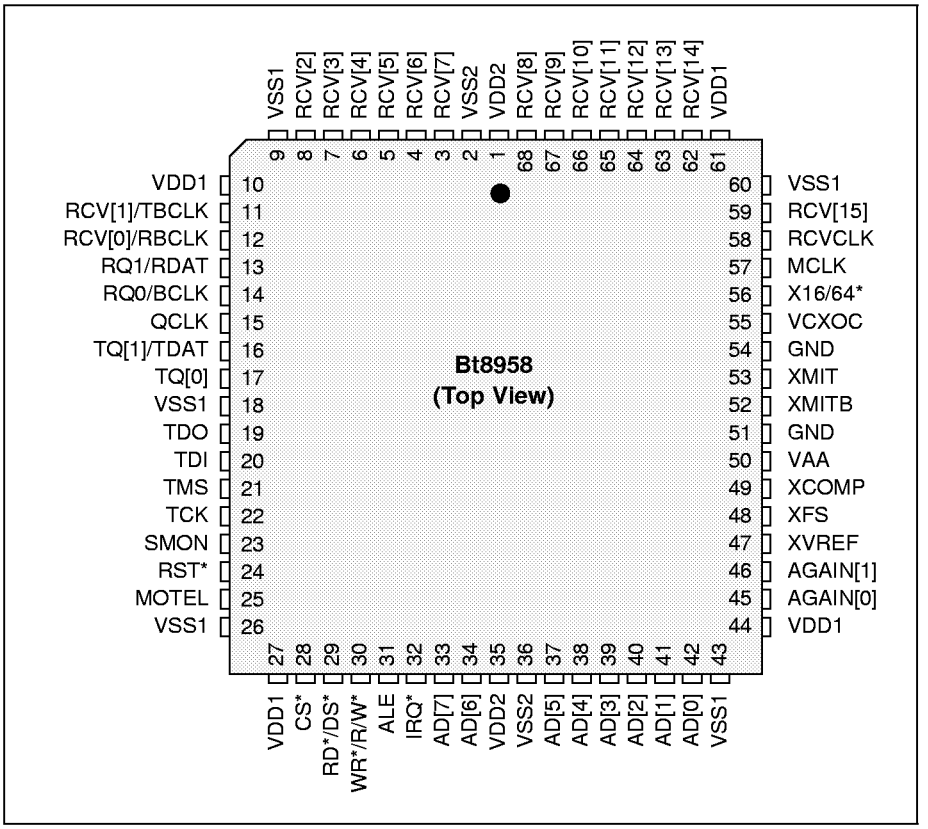


Figure 4. Bt8958 Logic Diagram

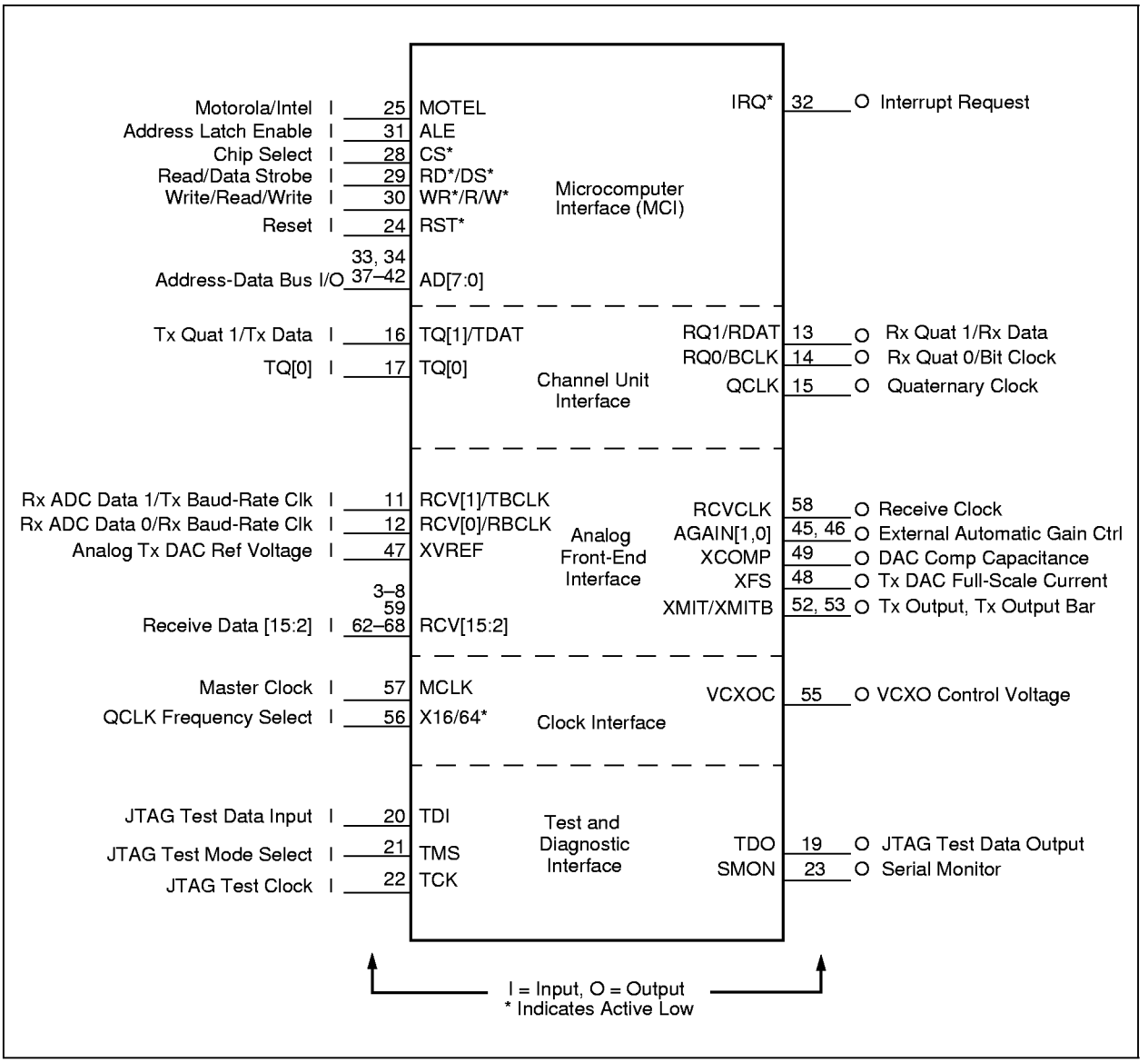


Table 1. Hardware Signal Definitions (1 of 5)

	Pin Label	Signal Name	I/O	Definition
Microcomputer Interface (MCI)	MOTEL	Motorola/Intel	I	Selects between Motorola and Intel handshake conventions for the RD*/DS* and WR*/R/W* signals. MOTEL = 1 for Motorola protocol: DS*, R/W* MOTEL = 0 for Intel protocol: RD*, WR*
	ALE	Address Latch Enable	I	Falling-edge-sensitive input. The value of AD[7:0] is internally latched on the falling edge of ALE.
	CS*	Chip Select	I	Active-low input that enables read/write operations on the MCI. May be used as an alternate strobe for all read/write cycle operations.
	RD*/DS*	Read/Data Strobe	I	Bimodal input that controls read/write access on the MCI. When MOTEL = 1 and CS* = 0, RD*/DS* behaves as an active-low data strobe DS*. Internal data is output on AD[7:0] when DS* = 0 and R/W* = 1. External data is internally latched from AD[7:0] on the rising edge of DS* when R/W* = 0. When MOTEL = 0 and CS* = 0, RD*/DS* behaves as an active-low read strobe RD*. Internal data is output on AD[7:0] when RD* = 0. Write operations are not controlled by RD* in this mode.
	WR*/ R/W*	Write/ Read/Write	I	Bimodal input that controls read/write access on the MCI. When MOTEL = 1 and CS* = 0, WR*/R/W* behaves as a read/write select line R/W*. Internal data is output on AD[7:0] when DS* = 0 and R/W* = 1. External data is internally latched from AD[7:0] on the rising edge of DS* when R/W* = 0. When MOTEL = 0 and CS* = 0, WR*/R/W* behaves as an active-low write strobe WR*. External data is internally latched from AD[7:0] on the rising edge of WR*. Read operations are not controlled by WR* in this mode.
	AD[7:0]	Address-Data Bus	I/O	Eight-bit bidirectional multiplexed address data bus. AD[7] = MSB, AD[0] = LSB.
	IRQ*	Interrupt Request	O	Active-low open-drain output that indicates requests for interrupt. Asserted whenever at least one unmasked interrupt flag is set. Remains inactive whenever no unmasked interrupt flags are present.
	RST*	Reset	I	Asynchronous, active-low, level-sensitive input that places the transceiver in an inactive state by setting the PWRDN bit of the Global Modes and Status Register [global_modes; 0x00] and by zeroing the mclk_freq[1,0] bits of the PLL Modes Register [pll_modes; 0x22]. Does not affect the state of the Test Access Port which is reset automatically at power-up only.

Table 1. Hardware Signal Definitions *(2 of 5)*

	Pin Label	Signal Name	I/O	Definition
Channel Unit Interface	RQ[1]/RDAT RQ[0]/BCLK	Receive Quat 1/Receive Data Receive Quat 0/Bit Clock	O O	RQ[1]/RDAT and RQ[0]/BCLK are bimodal outputs that represent the sign and magnitude bits of the received quaternary output symbol in parallel channel unit modes (RQ[1], RQ[0]), and the serial data and bit-clock outputs in serial channel unit modes (RDAT, BCLK). Behavior of these outputs is configurable through the Channel Unit Interface Modes Register [cu_interface_modes; 0x06] for parallel master, parallel slave, serial magnitude-bit-first, and serial sign-bit-first operation. For parallel master/slave operation: RQ[1] = Sign bit output RQ[0] = Magnitude bit output Both outputs are updated at the symbol rate on the rising edge of QCLK (master mode) or the rising/falling edge (programmable) of RBCLK (slave mode). For serial magnitude/sign-first operation: RDAT = Sign bit output when QCLK = 0 RDAT = Magnitude bit output when QCLK = 1 BCLK = Bit-rate (two times symbol rate) clock output. RDAT is updated at the bit rate on the rising edge of BCLK.
	TQ[1]/TDAT TQ[0]	Transmit Quat 1/ Transmit Data Transmit Quat 0	I I	TQ[1]/TDAT and TQ[0] are bimodal inputs that represent the sign and magnitude bits of the quaternary input symbol to be transmitted in parallel channel unit modes (TQ[1], TQ[0]), and the serial data input in serial channel unit modes (TDAT). Interpretation of these inputs is configurable through the Channel Unit Interface Modes Register [cu_interface_modes; 0x06] for parallel master, parallel slave, serial magnitude-bit-first, and serial sign-bit-first operation. For parallel master/slave operation: TQ[1] = Sign bit input TQ[0] = Magnitude bit input Both inputs are sampled at the symbol rate on the falling edge of QCLK (master mode) or the rising/falling edge (programmable) of TBCLK (slave mode). For serial magnitude/sign-first operation: TDAT = Sign bit input when QCLK = 0 TDAT = Magnitude bit input when QCLK = 1 TQ[0] = Don't care (tie/pull to supply rail) TDAT is sampled at the bit rate (two times symbol rate) on the falling edge of BCLK.
	QCLK	Quaternary Clock	O	The quaternary clock output running at the symbol rate, as configured by the X16/64* input. FQCLK = FMCLK ÷ 16 when X16/64* = 1 FQCLK = FMCLK ÷ 64 when X16/64* = 0 QCLK is also used to frame transmit/receive quats in serial mode.

Table 1. Hardware Signal Definitions (3 of 5)

	Pin Label	Signal Name	I/O	Definition
Analog Front End Interface	RCV[1]/ TBCLK	Receive ADC Data 1/ Transmit Baud-Rate Clock	I	Bimodal input pin configured by the interface_mode[1,0] field of the Channel Unit Interface Modes Register [cu_interface_modes; 0x06]. In the parallel-slave channel unit interface operating mode, this signal functions as the transmit baud-rate clock input TBCLK. It must be frequency locked to QCLK. The second-least-significant ADC input bit position, RCV[1], is internally zeroed in this mode. In all other channel unit interface operating modes, this signal functions as the second-least-significant ADC input bit, RCV[1]. If a 14-bit or smaller ADC is used, this input should be tied/pulled to ground.
	RCV[0]/ RBCLK	Receive ADC Data 0/ Receive Baud-Rate Clock	I	Bimodal input pin configured by the interface_mode[1,0] field of the Channel Unit Interface Modes Register [cu_interface_modes; 0x06]. In the parallel-slave channel unit interface operating mode, this signal functions as the receive baud-rate clock input RBCLK. It must be frequency locked to QCLK. The least-significant ADC input bit position, RCV[0], is internally zeroed in this mode. In all other channel unit interface operating modes, this signal functions as the least-significant ADC input bit, RCV[0]. If a 15-bit or smaller ADC is used, this input should be tied/pulled to ground.
	RCVCLK	Receive Clock	O	Sample clock output that strobes the ADC. RCVCLK operates at the symbol rate with a 1/16 duty cycle. The phase relationship between RCVCLK and QCLK is programmable through the Receive Phase Select Register [receive_phase_select; 0x07].
	AGAIN[1,0]	External Automatic Gain Control	O	Digital control outputs that selects external automatic gain control circuits, if implemented. Outputs are configured/controlled through the ADC Gain Control Register [adc_control; 0x21]. In fixed-mode external AGC, both output levels are set by directly writing their values to the again[1,0] field of this control register. In continuous-mode external AGC, AGAIN[1] is automatically updated to indicate the direction of external gain change required. AGAIN[1] = 1 when more external gain required AGAIN[1] = 0 when less external gain required. AGAIN[0] is not affected in this mode. In continuous mode, AGAIN[1] is updated on the rising edge of QCLK. In fixed mode, both outputs are updated by an internal 64-times symbol-rate clock.
	XVREF	Analog Transmit DAC Reference Voltage	I	Analog input for an external precision voltage reference. Used in conjunction with XFS to set full-scale current for the internal transmit DAC.
	XCOMP	DAC Compensation Capacitance	O	Analog output connection point for a transmit DAC compensation capacitor to VAA.
	XFS	Transmit DAC Full-Scale Current	O	Analog output connection point for a precision resistor, R_{FS}, to analog ground. Used to set the transmit DAC full-scale output current, I_{FS}, using the equation $I_{FS} = XVREF \div R_{FS}$.

Table 1. Hardware Signal Definitions (4 of 5)

	Pin Label	Signal Name	I/O	Definition
Analog Front End Interface	XMIT, XMITB	Transmit Output, Transmit Output Bar	O	Complementary unipolar current-mode outputs of the internal sigma-delta transmit DAC. The sum of XMIT and XMITB currents, IFS, is always constant, and equal to XVREF÷ RFS (RFS is an external full-scale-setting precision resister connected between signal XFS and analog ground). Five possible output current levels exist for each signal: 0, 1/4IFS, 1/2IFS, 3/4IFS, IFS. Outputs switch at 64 times the symbol rate.
	RCV[15:2]	Receive Data [15:2]	I	Fourteen most-significant inputs of the 16-bit ADC input interface. Input data is required to be in offset binary format with RCV[15] representing the MSB. All inputs are sampled on the rising edge of RCVCLK. Any unused inputs should be tied/pulled to ground.
Clock Interface	MCLK	Master Clock	I	The input frequency must be either 16 or 64 times the desired symbol rate, as determined by the level of the X16/64* input pin.
	X16/64*	QCLK Frequency Select	I	Selects between two different FMCLK ÷ FQCLK frequency relationships. X16/64* = 1 for FMCLK ÷ FQCLK = 16 X16/64* = 0 for FMCLK ÷ FQCLK = 64
	VCXOC	VCXO Control Voltage	O	Control voltage output of the timing recovery module's first-order sigma-delta DAC. The single-bit output switches between the I/O supply levels of VDD2 and VSS2 at a minimum oversampling rate of 256. Updated at the symbol rate on the rising edge of QCLK.
Test and Diagnostic Interface	TDI	JTAG Test Data Input	I	Test data input per IEEE Std 1149.1-1990. Loads all serial instructions and data into internal test logic. Sampled on the rising edge of TCK. If unused, TDI should be pulled high.
	TMS	JTAG Test Mode Select	I	Test mode select input per IEEE Std 1149.1-1990. Internally pulled-up input signal that controls the test-logic state machine. Sampled on the rising edge of TCK. If unused, TMS may be left unconnected.
	TDO	JTAG Test Data Output	O	Test data output per IEEE Std 1149.1-1990. Three-state output that reads all serial configuration and test data from internal test logic. Updated on the falling edge of TCK.
	TCK	JTAG Test Clock	I	Test clock input per IEEE Std 1149.1-1990. Used for all test interface and internal test-logic operations. If unused, TCK should be pulled low.
	SMON	Serial Monitor	O	Serial data output used for real-time monitoring of internal signal-path registers. The source register is selected through the Serial Monitor Source Select Register [serial_monitor_source; 0x01]. 16-bit words are shifted out, LSB first, at 16 times the symbol rate. The rising edge of QCLK defines the start (LSB) of each word. When X16/64* = 1, the output is updated on the rising edge of MCLK. When X16/64* = 0, the output is updated by an internal clock.

Table 1. Hardware Signal Definitions *(5 of 5)*

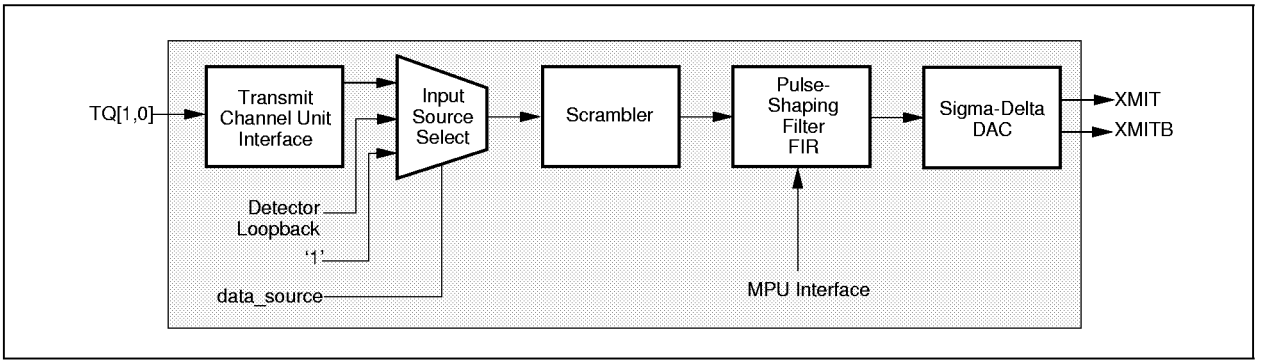
	Pin Label	Signal Name	I/O	Definition
Power and Ground	VDD1	Core Logic Power	–	Dedicated supply pins powering the digital core logic functions.
	VSS1	Core Logic Ground	–	Dedicated ground pins for the digital core logic functions.
	VDD2	I/O Buffer Power	–	Dedicated supply pins powering the digital I/O buffers.
	VSS2	I/O Buffer Ground	–	Dedicated ground pins for the digital I/O buffers.
	VAA	Analog Power Supply	–	Dedicated supply pin powering the transmit DAC analog circuitry.
	GND	Analog Ground	–	Dedicated ground pins for the transmit DAC analog circuitry.

Functional Description

Transmit Section

The transmit section, illustrated in Figure 5, comprises five major functions: a channel unit interface, a symbol-source selector, a scrambler, a pulse-shaping filter, and a Digital-to-Analog Converter (DAC).

Figure 5. Transmit Section Block Diagram



Transmit Channel Unit Interface

The transmit channel unit interface samples the sign and magnitude input at TQ[1,0] and converts it to two's complement binary form. The interface can operate in parallel master, parallel slave, and two serial modes. They can all be configured through the Channel Unit Interface Modes Register [cu_interface_modes; 0x06].

Input Source Select

The input source select can be configured through the data_source[2:0] bits of the Transmitter Modes Register [transmitter_modes; 0x0B] to select two-level or four-level output, all ones, isolated pulse, or detector loopback.

Scrambler

The scrambler block connects the output of the input source selector to the pulse shaping filter. The scrambler may either scramble the signal or pass it through unmodified. The scrambler is essentially a 23-bit-long Linear Feedback Shift Register (LFSR) with feedback as described in TA-NWT-001210. The feedback points are programmable for central office and remote terminal applications. The LFSR polynomials are:

$$\text{NTU/HTU-R} \Rightarrow x^{-23} \oplus x^{-18} \oplus 1$$
$$\text{LTU/HTU-C} \Rightarrow x^{-23} \oplus x^{-5} \oplus 1$$

The scrambler operates differently depending on whether two-level or four-level mode is specified. In two-level mode, the LFSR is clocked once per symbol; in four-level mode the LFSR is clocked twice per symbol.

The bit stream output of the scrambler in two-level mode is converted into symbols as shown in Table 2.

Table 2. Two-Level Bit-to-Symbol Conversion

Input Bit	Output Symbol
0	–3
1	+3
NA	–1
NA	+1

The bit stream is converted into symbols for the four-level case as shown in Table 3.

Table 3. Four-Level Bit-to-Symbol Conversions

First Input Bit (sign)	Second Input Bit (magnitude)	Output Symbol
0	0	–3
0	1	–1
1	1	+1
1	0	+3

The most useful combinations of the transmitter source mode bits are summarized in Table 4.

Table 4. Symbol Source Combinations

Input Source Select	Scrambler	Levels	Use
External	Off	4	Normal operation
External	Off	2	Special start-up, magnitude bit of input is ignored
Ones	On	2	Stand alone start-up
Ones	On	4	Stand alone start-up
Ones	Off	–	Produces a DC signal which cannot be transmitted
Loopback	–	–	Diagnostics

Pulse Shaping Filter

A 48-tap interpolating Finite Impulse Response (FIR) filter shapes the transmitted signal. Sixteen different output phases are computed using three transmit symbols. The output is computed according to the following equation:

$$O_{k,j} = \sum_{i=0}^{2} B_{k-i} \times C_{16i+j}$$

where: O = Output to DAC
B = Quaternary symbol to be transmitted
C = Interpolative coefficients
k = Symbol number
j = Sub-baud phase (range from 0 – 2 π over 16 intervals)

A current-mode sigma-delta DAC accurately converts the output of the pulse-shaping filter to analog form.

Transmit Digital-to-Analog Converter (DAC)

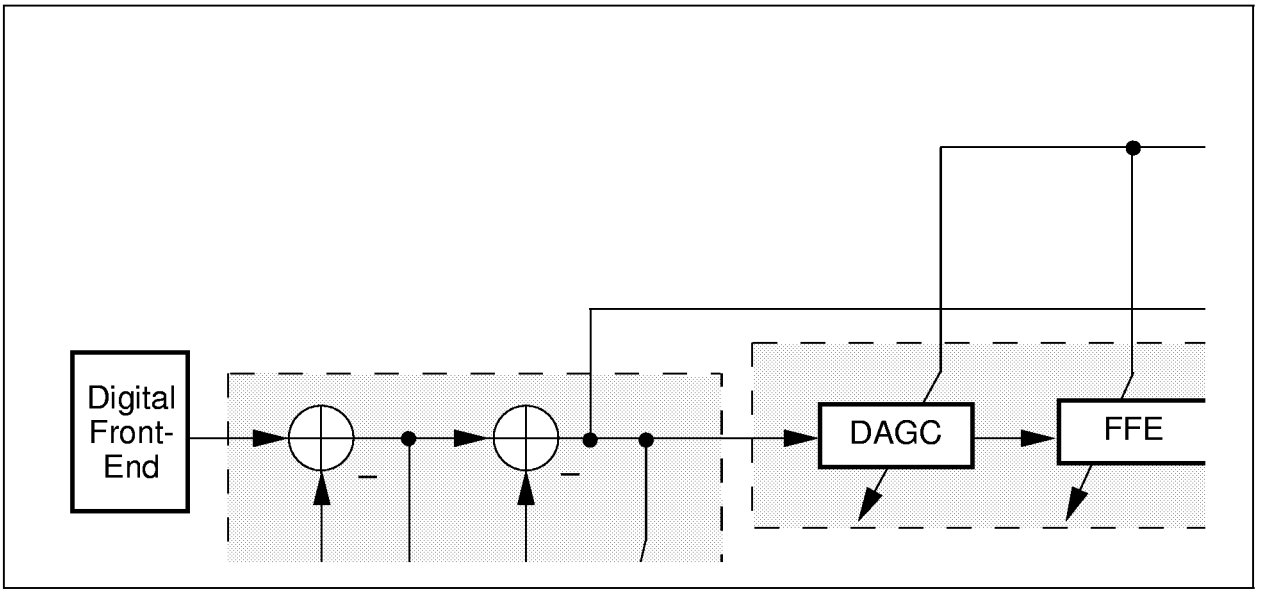
A 12-bit sigma-delta DAC provides digital-to-analog current conversion of the output of the pulse shaping filter. The analog front-end performs DAC reconstruction filtering. This filter, in conjunction with the digital interpolating filter and sigma-delta DAC, produces pulses that meet the pulse shape and power spectral density requirements specified by Bellcore in TA-NWT-001210 and by ETSI RTR/TM-03036.

Receive Section

Receiver Processing

The receiver processing section includes front-end processing, echo cancellation, equalization, timing recovery, and symbol detection. Five Least Mean Squared (LMS) filters equalize the received signal so that transmitted symbols can be reliably recovered. The receiver uses symbol rate sampling for all processing functions. The filters include an Echo Canceler (EC), a Digital Automatic Gain Controller (DAGC), a Feed Forward Equalizer (FFE), an Error Predictor (EP), and a Decision Feedback Equalizer (DFE). Their interconnections and relationships to the digital front-end and the detector are shown in Figure 6.

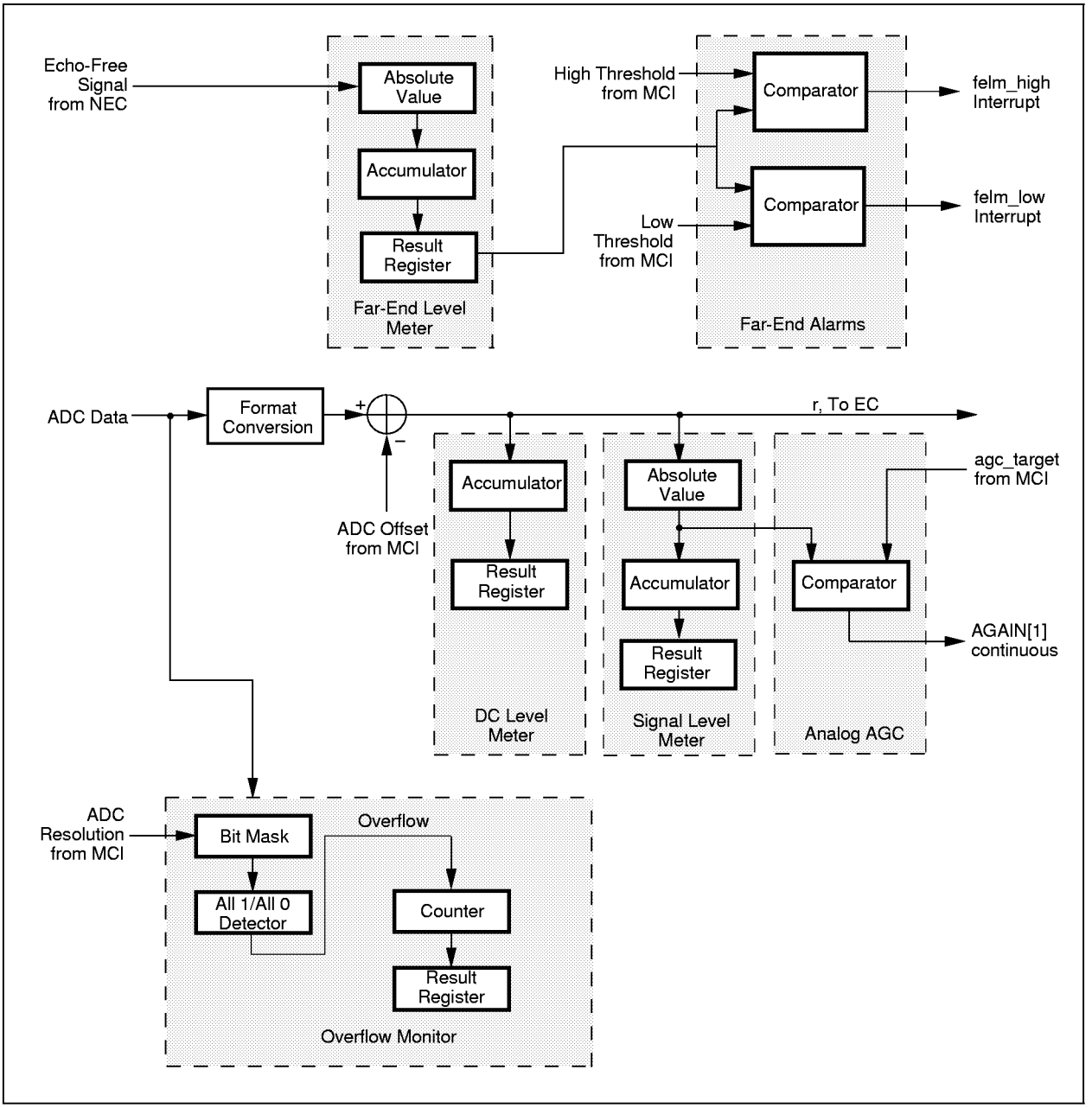
Figure 6. Receiver Filters



Digital Front-End

Prior to the main signal processing, the input signal must be converted to the proper format and adjusted for any DC offset. The front-end module also monitors the input signal level. This includes measuring DC and AC input signal levels, detecting and counting overflows, and detecting alarms based on the far-end signal level. Figure 7 summarizes the features of the digital front-end module.

Figure 7. Digital Front-End Block Diagram



Format Conversion

The input signal from the ADC at the receive data interface must be in offset binary format. The first step in the processing is inversion of the Most Significant Bit (MSB) to convert to two's complement format. If an Analog-to-Digital Converter (ADC) with fewer than 16 bits is being used, the ADC's output should be connected to the MSBs of the input bus with the unused Least Significant Bits (LSBs) grounded.

Offset Adjustment

A nonzero DC level on the input can be corrected by an ADC offset value [dc_offset_low, dc_offset_high; 0x26, 0x27] which is subtracted from the input (after conversion to two's complement format). The ADC offset is a 16-bit number and is programmed via the microcomputer interface. The result of this subtraction is saturated to a proper two's complement 16-bit number.

DC Level Meter

The DC Level Meter provides the monitoring needed for adaptive offset compensation. The offset adjusted input signal is accumulated over the interval TMETER. The 16 MSBs are placed into the DC Meter Registers [dc_meter_low, dc_meter_high; 0x44, 0x45].

Signal Level Meter

The Signal Level meter provides the monitoring needed for adjusting the analog gain circuit located prior to the ADC. This value is accumulated over the time span TMETER. The 16 MSBs are placed in the Signal Level Meter Registers [slm_low, slm_high; 0x46, 0x47].

Overflow Detection and Monitoring

The overflow sensor detects an overflow if the input from the ADC is all-ones or all-zeros. The resolution of the ADC is programmed into the ADC Bit Width Register [adc_bit_width; 0x20]. If the resolution is less than 16 bits, the unused LSBs are ignored in detecting an overflow. Table 5 shows the input data values which are overflows.

The overflow monitor counts the number of overflows, as indicated by the overflow sensor, during the TMETER interval. The counter is limited to 8 bits. In the case of 256 or more overflows during the measurement interval, the counter will hold at 255. The counter is loaded into the Overflow Meter Register [overflow_meter; 0x42] at the end of each measurement interval.

Table 5. Overflow Bit Masking

ADC Resolution	RCV15	RCV14	RCV13	RCV12	RCV11	RCV10	RCV9	RCV8	RCV7	RCV6	RCV5	RCV4	RCV3	RCV2	RCV1	RCV0
16	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14	1	1	1	1	1	1	1	1	1	1	1	1	1	1	X	X
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X	X
12	1	1	1	1	1	1	1	1	1	1	1	1	X	X	X	X
	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X

Far-End Level Meter

The Far-End Level Meter monitors the output of the echo canceler. Since the output of the echo canceler has had the echo of the transmitted signal subtracted from it, it is fair to call it the far-end signal. This value is accumulated over the time span TMETER. The 16 MSBs are placed into the Far-End Level Meter Register [felm_low, felm_high; 0x48, 0x49].

Far-End Level Alarm

The result of the Far-End Level Meter is compared to two thresholds. When exceeded, an interrupt is sent to the microcomputer interface, if enabled. The threshold is determined by the value in the Far-End High Alarm Threshold Registers [far_end_high_alarm_th_low, far_end_high_alarm_th_high; 0x30, 0x31] and the Far-End Low Alarm Threshold Registers [far_end_low_alarm_th_low, far_end_low_alarm_th_high; 0x32, 0x33].

The interrupts, high_felm, and low_felm are bits 2 and 1 respectively of IRQ Source Register [irq_source; 0x05]. The interrupts far_end_low_alarm_th_high and far_end_low_alarm_th_low, can be masked by writing a one to bits 2 and 1 respectively of the Interrupt Mask Register High [mask_high; 0x03].

External Automatic Gain Control (AGC)

The external AGC function controls user supplied gain stages prior to the ADC. The external AGC can operate in two modes: fixed or continuous.

In the fixed mode, the two AGC control bits are simply specified via the ADC Gain Control Register [adc_control; 0x21] and driven onto the AGAIN[1,0] pins.

In the continuous mode, the AGAIN[1] pin is changed based on each input sample. The AGC Target Register [agc_target_low, agc_target_high; 0x28, 0x29] is treated as a two's complement number but should always be positive. The resulting signal on AGAIN[1] can be low-pass filtered and used to control a continuously variable gain amplifier.

NOTE: AGAIN[0] is still set as in the fixed mode, and the bit value specified for AGAIN[1] is not used.

Echo Canceler (EC)

The Echo Canceler (EC) removes images of the transmitted symbols from the received signal. It is made up of two blocks: a Linear Echo Canceler (LEC) and a Nonlinear Echo Canceler (NEC). The organization of the blocks can be seen in Figure 6.

1 LEC—A conventional LMS Finite Impulse Response (FIR) filter that removes linear images of the transmitted symbols from the received signal. LEC consists of a 120-tap FIR filter with 32-bit linear adapted coefficients. When enabled, the last data tap (#119) of the echo canceler is treated specially. The data value used for this tap is always 0x0003. This serves to cancel any DC offset which may be present. A freeze coefficient mode may be specified via the microcomputer interface. This mode disables the coefficient updates only. A special mode exists to zero all of the coefficients; it is also enabled through the microcomputer interface. An additional mode exists to zero the output of the FIR with no effect on the coefficients. It is also enabled through the microcomputer interface. Individual EC coefficients can be read and written through the microcomputer interface. Adaptation should be frozen prior to reading or writing coefficients.

2 NEC—Reduces the residual echo power in the echo canceler output caused by nonlinear effects in the transmitter DAC, receiver ADC, analog hybrid circuitry, or line cables. The delay of the transmit symbol input to the NEC can be specified via the microcomputer interface, Nonlinear Echo Canceler Mode Register [nonlinear_ec_modes; 0x09]. This allows the NEC to operate on the peak of the echo regardless of differing delays in the echo path. The delay would differ, for example, if a pipelined ADC were used. A freeze coefficient mode may be specified via the microcomputer interface. This mode disables the coefficient updates only. A special mode exists to zero all of the coefficients; it is also enabled through the microcomputer interface. An additional mode exists to zero the output of the look-up table with no effect on the coefficients. It is also enabled through the microcomputer interface. The 64, 14-bit individual NEC coefficients can be read and written through the microcomputer interface. Adaptation should be frozen prior to reading or writing coefficients.

Equalizer

Four LMS filters are used in the equalizer to process the echo canceler output so that received symbols can be reliably recovered. The filters are a Digital Automatic Gain Controller (DAGC), a Feed Forward Equalizer (FFE), an Error Predictor (EP), and a Decision Feedback Equalizer (DFE). Their interconnections are shown in Figure 6, and the four filters are described as follows:

1 DAGC—Scales the echo-free signal to the optimum magnitude for subsequent processing. Its structure is that of an LMS filter but it is a degenerate case since there is only one tap. A freeze coefficient mode may be specified via the microcomputer interface. This mode disables the coefficient update only. The DAGC gain coefficient can be read or written through the microcomputer interface. Adaptation should be frozen prior to reading or writing the coefficient.

2 FFE—Removes precursors from the received signal. The FFE may be operated in a special *adapt last* mode. In this mode, which is useful during start-up, only the last coefficient is updated. The last coefficient is the one multiplied with the oldest data sample, sample number 7. A freeze coefficient mode may be specified via the microcomputer interface. This mode disables the coefficient updates only. A special mode exists to zero all of the coefficients; it is also enabled through the microcomputer interface. Individual FFE coefficients can be read and written through the microcomputer interface. Adaptation should be frozen prior to reading or writing coefficients.

3 EP—Improves the performance of the equalizer by prognosticating errors before they occur. A freeze coefficient mode may be specified via the microcomputer interface. This mode disables the coefficient updates only. A special mode exists to zero all of the coefficients; it is also enabled through the microcomputer interface. Individual EP coefficients can be read and written through the microcomputer interface. Adaptation should be frozen prior to reading or writing coefficients.

4 DFE—Removes postcursors from the received signal. A freeze coefficient mode may be specified via the microcomputer interface. This mode disables the coefficient updates only. A zero coefficients mode exists to zero all of the coefficients; it is also enabled through the microcomputer interface. A zero filter output mode exists to zero the output of the FIR with no effect on the coefficients. It is also enabled through the microcomputer interface. Individual DFE coefficients can be read and written through the microcomputer interface. Adaptation should be frozen prior to reading or writing coefficients.

The DAGC, FFE, and EP filters are implemented using an internal microprogrammable Digital Signal Processor (DSP) optimized for LMS filters. Internal DSP micro-instructions are stored in an on-chip RAM. This microcode RAM is loaded after power-up through the microcomputer interface when the transceiver is initialized.

Detector

The detector converts the equalized received signal into a 2B1Q symbol and produces two error signals (16-bit slicer error and 16-bit equalizer error) used in adapting the receiver equalizers: a 16-bit slicer error and a 16-bit equalizer error. The signal detection uses two subblocks: a slicer, and a Peak Detector (PKD). Additionally, the detector contains a scrambler and Bit Error Rate (BER) meter for use during the start-up sequence.

The slicer thresholds the equalized signal to produce a 2B1Q symbol. The input to the slicer is the FFE output minus the DFE and EP outputs. The slicer can operate in two modes: two-level and four-level. In the two-level mode, used during the part of start-up when the only transmitted symbols are +3 or –3, the slicer threshold is set at zero. When in four-level mode, the cursor level is specified via the microcomputer interface. It is a 16-bit two's complement number but must be positive and less than 0x2AAA for proper operation.

The PKD is only used during the two-level transmission part of start-up. It operates on the echo free signal. A signal is detected to be a +3 if it is higher than both of its neighbors, or a –3 if it is lower than both of its neighbors. If neither peaked condition exists, the output of the slicer is used.

The scrambler operates as either a scrambler or as a descrambler. The scrambler block is used during the scrambled ones part of the start-up sequence. This provides an error-free signal for equalizer adaptation. This scrambler is essentially a 23-bit-long Linear Feedback Shift Register (LFSR) with feedback as described in TA-NWT-001210. The feedback point depends on whether the transceiver is being used in a central-office or remote-terminal application.

When operating as a descrambler, the input source is the detector output. The symbol is converted to a bit stream as shown in Table 6 for the two-level case.

The symbol is converted to a bit stream as shown in Table 7 for the four-level case. The LFSR operates in the same way in both cases, except in the two-level case it is clocked once per symbol and in the four-level case it is clocked twice per symbol.

Table 6. Two-Level Symbol-to-Bit Conversion

Input Symbol	Output Bit
–3	0
+3	1
–1	NA
+1	NA

Table 7. Four-Level Symbol-to-Bit Conversion

Input Symbol	First Output Bit (sign)	Second Output Bit (magnitude)
–3	0	0
–1	0	1
+1	1	1
+3	1	0

When operating as a scrambler, the LFSR must first be locked to the far-end source. Once locked, it is then able to replicate the far-end input sequence, when its input is held at all ones.

The locking sequence is controlled internally, initiated through the microcomputer interface by setting lfsr_lock [bit 2] of the Symbol Detector Modes Register [detector_modes; 0x3A]. The locking sequence consists of four steps.

1. Operate the LFSR as a *descrambler* for 23 bits.
2. Operate the LFSR as a *scrambler* for 127 bits. The sync detector is active during this period.
3. If synchronization was not achieved go to step 1; otherwise continue to step 4.
4. Send an interrupt to the microcomputer, if unmasked, indicating successful locking and continue operating as a scrambler.

The sequence continues until the lfsr_lock control bit is cleared by the microcomputer.

Sync Detector

The sync detector compares the output of the scrambler with the output of the symbol detector. The number of equivalent bits is accumulated for 128 comparisons. The result is then compared to a Scrambler Synchronization Threshold Register [scr_sync_th; 0x2E]. Lock is declared and the sync bit of the IRQ Source Register [irq_source; 0x05] is set if the count is greater than the threshold. For a count less than or equal to the threshold, no lock condition is declared and the sync bit is unaffected.

Detector Meters

Five meters are included in the detector: a BER meter, a symbol histogrammer, a noise-level meter, a noise-level histogram meter, and an SNR alarm meter.

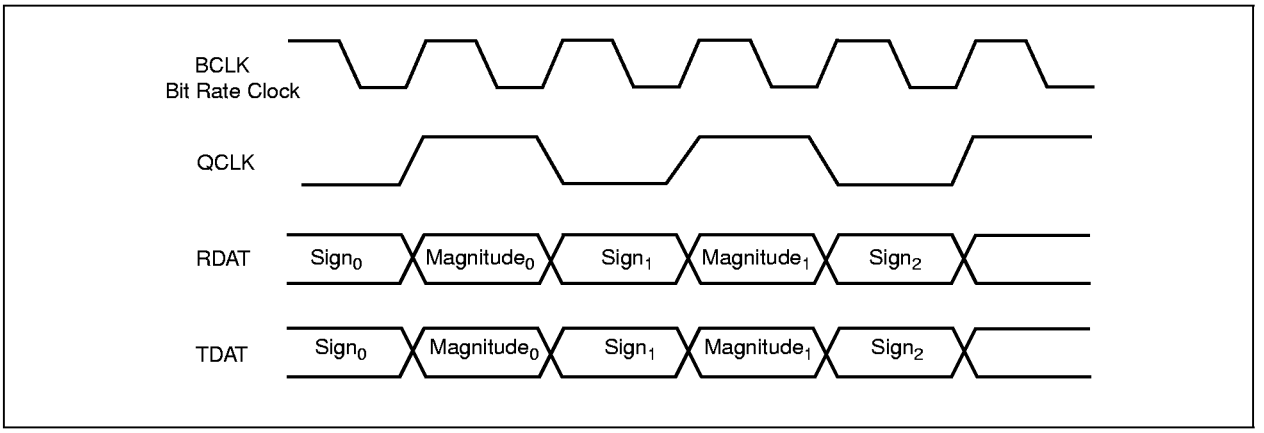
1. BER Meter—Provides an estimate of the bit error rate when the received symbols are known to be scrambled ones. When the LFSR is operating as a descrambler the meter counts the number of ones on the descrambler output. When the LFSR is operating as a scrambler, the BER meter counts the number of equal scrambler and symbol detector outputs. The counter operates over the TMETER interval. The counter is saturated to 16 bits. At the end of the measurement interval the counter is loaded into a separate result register.
2. Symbol Histogrammer—Computes a coarse histogram of the received symbols. It operates by counting the number of ones received during TMETER interval. That is, at the start of the measurement interval a counter is cleared. For each detector output which is +1 or –1 the counter is incremented. If the detector output is +3 or –3 the count is held at its previous value. The count is saturated to 16 bits. At the end of the measurement interval, the 8 MSBs of the counter are loaded into the Symbol Histogram Meter Register [symbol_histogram; 0x4E].
3. Noise Level Meter—Estimates the noise at the input to the slicer. It operates by accumulating the absolute value of the slicer error over TMETER interval.
4. At the end of the measurement interval performed by the Noise Level Meter, the 16 MSBs of the 32-bit accumulator loaded into the Noise Level Histogram Meter Register [alm_low, alm_high; 0x50, 0x51.
5. SNR Alarm—Provides a rapid indication of impulse noise disturbances and loss of signal so that corrective action can be taken. The alarm is based on a second noise level meter. The meter is the same as the preceding noise level meter except it operates on a dedicated timer, the SNR Alarm Timer. The absolute value of the slicer error is accumulated during the timer period. At the end of the measurement interval, the 16 MSBs of the accumulator are compared against the SNR Alarm Threshold Register [snr_alarm_th_low, snr_alarm_th_high; 0x34, 0x35]. If the result is greater than this threshold, an interrupt is set in the IRQ Source Register. The threshold is set via the microcomputer interface.

Channel Unit Interface

The quaternary signals of the channel unit interface have four modes that are programmable through bits 0 and 1 of the Channel Unit Interface Modes Register [cu_interface_modes; 0x06]. The four modes are serial sign-bit first, serial magnitude-bit first, parallel master, and parallel slave.

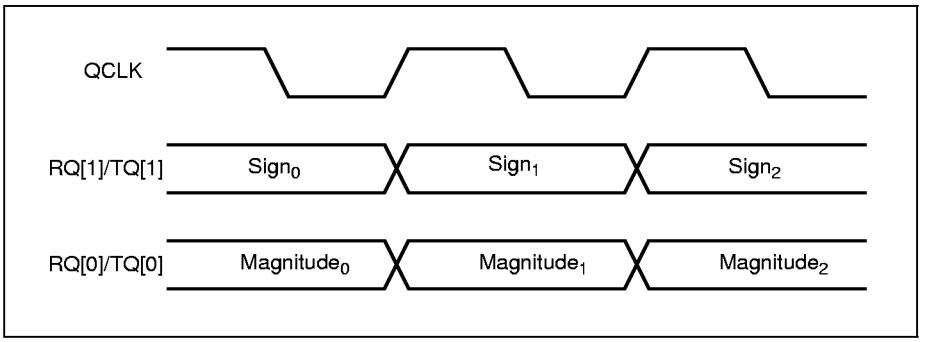
In serial mode, a bit rate clock (BCLK) is output at twice the symbol rate. The sign and magnitude bits of the receive data are output through RDAT on the rising edge of BCLK. The sign and magnitude bits of the transmit data are sampled on the falling edge of BCLK at the TDAT input. The sign bit is transferred first followed by the magnitude bit of a given symbol in sign-bit first mode, while the opposite occurs in magnitude-bit first mode. The clock relationships for sign-bit first mode are shown in Figure 8.

Figure 8. Serial Sign-Bit First Mode



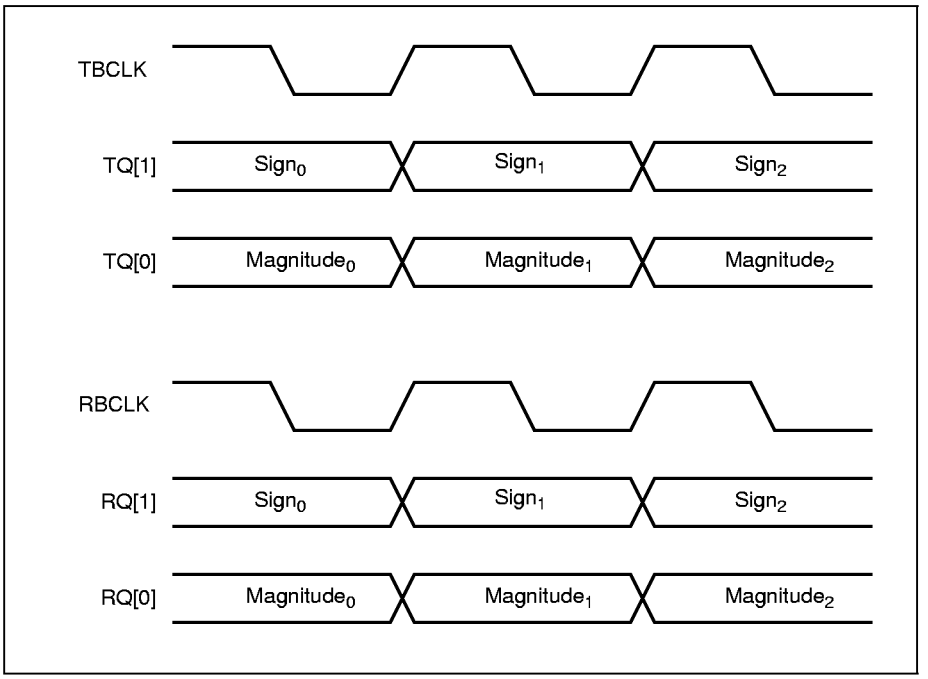
In parallel master mode, the sign and magnitude receive data is output through RQ[1] and RQ[0], respectively, on the rising edge of QCLK. The quaternary transmit data is sampled on the falling edge of QCLK. This clock and data relationship is illustrated in Figure 9.

Figure 9. Parallel Master Mode



Parallel slave mode uses RBCLK and TBCLK inputs to synchronize data transfer. RBCLK and TBCLK must be frequency locked to QCLK, though the use of two internal FIFOs allow an arbitrary phase relationship to QCLK. TQ[1] and TQ[0] are sampled on the active edge of TBCLK, as programmed through the MCI. RQ[1] and RQ[0] are output on the active edge of RBCLK, also as programmed through the MCI. The clock relationships for the case where TBCLK is programmed to be falling-edge active and RBCLK is rising-edge active are illustrated in Figure 10.

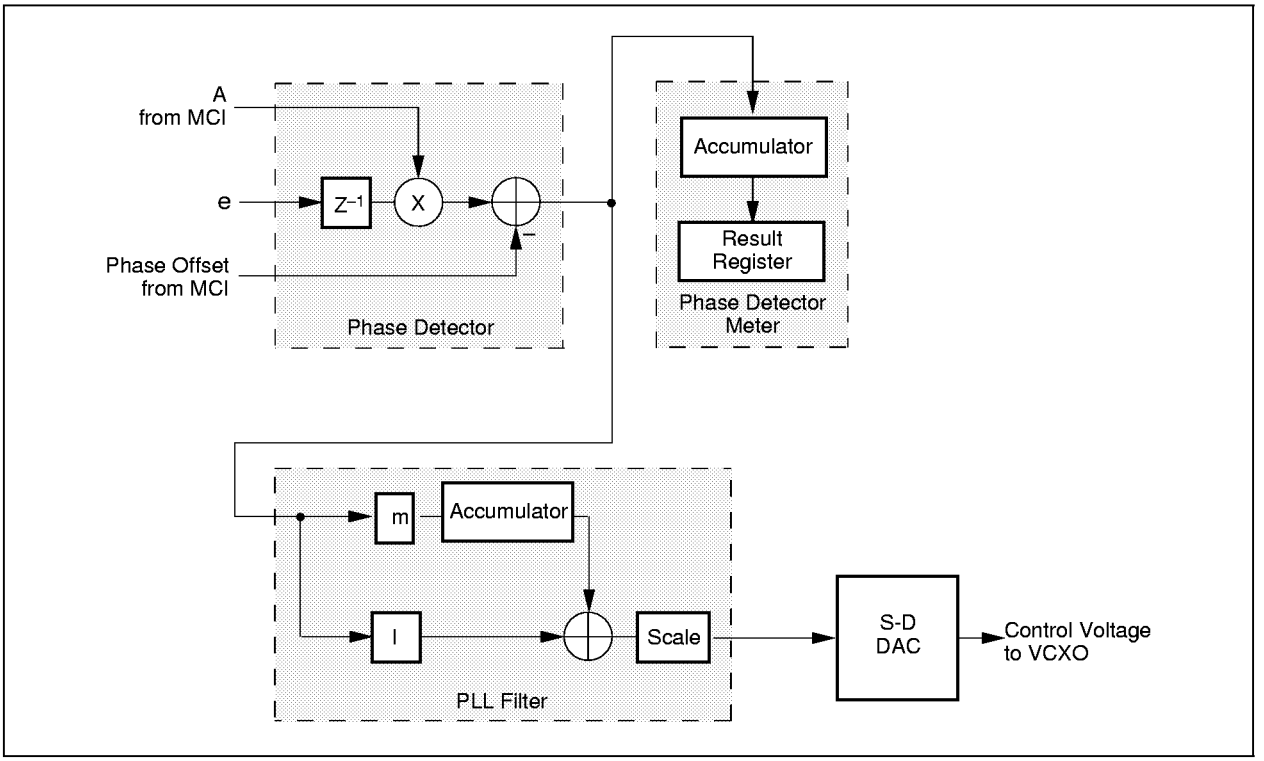
Figure 10. Parallel Slave Mode



Timing Recovery

The timing recovery block provides the processing needed to generate a VCXO control voltage to generate a sampling clock at the proper phase and frequency. It consists of a phase detector, loop filter, DAC, and meters as shown in Figure 11.

Figure 11. Timing Recovery Module



The phase detector computes a phase error signal. The Phase Lock Loop (PLL) works to minimize the equalizer error. Phase offset is a constant which is specified via the MCI interface.

An integral, proportional loop filter stabilizes the timing. The filter characteristics are selected via the microcomputer interface. Saturation is used in setting the results.The loop filter can also be frozen. In this case the accumulator is not updated. This allows the user to directly specify the frequency via the microcomputer interface. A phase detector negate mode, bit 5 of the PLL Modes Register [pll_modes; 0x22], exists to enable use of negative slope VCXOs. The difference is the sign of the error signal.

The analog control voltage for the VCXO is generated by an integrated 14-bit sigma-delta DAC. The input to the DAC is latched every 256 symbols. The output switches at the symbol rate.

The phase detector meter measures the average value of the phase correction signal. This information is needed during start-up to correctly set the phase offset in the Receive Phase Select Register [receive_phase_select; 0x07]. The output of the phase detector is accumulated over the interval TMETER. The accumulation is saturated to 32 bits. At the end of the measurement interval, the 16 MSBs of the value are loaded into the Phase Detector Meter Register [pdm_low, pdm_high; 0x40, 0x41].

Timers

Eight timers are integrated into the transceiver to control the various on-chip meters and to aid the microcomputer in stepping through the events of the start-up sequence.

General Timer Structure

The structure of each timer includes down counter, zero detect logic, and control circuitry which determines when the counter is reloaded or decremented.

For each of the eight timers, there is a 2-byte timer interval register that determines the value from which the timer decrements. Three 8-bit registers control timer operation: Timer Restart Register [timer_restart; 0x0C], Timer Continuous Mode Register [timer_continuous; 0x0E], Timer Enable Register [timer_enable; 0x0D]. Each bit of the 8-bit registers corresponds to a timer. Each logic-high bit in timer_restart acts as an event that causes the corresponding timer to reload. Each logic-high bit in timer_enable acts to enable the corresponding timer. Each logic-high bit in timer_continuous acts to reload the counter after timing out.

Each counter is loaded with the value in its interval register. The counter decrements until it reaches zero. Upon reaching zero, an interrupt is generated if enabled by the Interrupt Mask Low Register [mask_low_reg; 0x02]. The interrupt is edge triggered so that only one interrupt will be caused by a single time out.

A prescaler may precede the timer. This increases the time span available at the expense of resolution. Only the start-up timers have prescalers. Table 8 summarizes the timer information.

Table 8. Timers

Timer Name	Purpose	Clock Rate	Control Bits
Start-up Timer 1	Start-up Events	Symbol Rate ÷ 1024	sut 1
Start-up Timer 2	Start-up Events	Symbol Rate ÷ 1024	sut 2
Start-up Timer 3	Start-up Events	Symbol Rate ÷ 1024	sut 3
Start-up Timer 4	Start-up Events	Symbol Rate ÷ 1024	sut 4
SNR Alarm Timer	SNR Measurement	Symbol Rate	snr
TMETER	Measurement	Symbol Rate	meter
General Purpose Timer 3	Miscellaneous	Symbol Rate	t3
General Purpose Timer 4	Miscellaneous	Symbol Rate	t4

Four timers are for timing start-up events. These timers share a single prescaler that divides the symbol clock by 1024 and supplies this slow clock to the four counters. The timers are Start-Up Timer 1, Start-Up Timer 2, Start-Up Timer 3, and Start-Up Timer 4. Each one is independent with separate interval timer values and separate interrupts.

Two timers control the measurement intervals for the various meters: SNR Alarm Timer and TMETER (meter timer). The SNR Alarm Timer is used only by the low SNR meter, while TMETER is used by all other meters, excluding the low SNR meter. Their respective interrupts are set when each of these two timers expire. There are no prescalers for these timers; they count at the symbol rate. Both timers are normally used in the continuous mode.

Two timers are for general use: General Purpose Timer 3 and General Purpose Timer 4. Both timers are identical. There are no prescalers for these timers; they count at the symbol rate. Each timer signals an interrupt when it expires.

Microcomputer Interface (MCI)

The Microcomputer Interface (MCI) provides operational mode control and status through internal registers. A microcomputer write sets the operating modes to the appropriate registers. A read to a register verifies the operating mode or provides the status. The microcomputer interface can be programmed to generate an interrupt on certain conditions.

Source Code

Brooktree provides portable C source code under a no-cost licensing agreement. This source code provides a fully ETSI and Bellcore compliant start-up procedure, as well as diagnostic and system monitoring functions.

Microcomputer Read/Write

The MCI uses an 8-bit-wide address-data bus for access to the internal control and status registers, coefficients, and microcode RAM. The interface is compatible with Intel or Motorola microcomputers, and is configured with the MOTEL input. MOTEL low selects Intel-type microcomputer and control signals: ALE, CS*, RD*, WR*. MOTEL high selects Motorola-type microcomputer and control signals: ALE, CS*, DS*, R/W*.

The MCI provides access to a 256-byte internal address space. These registers provide configuration, control, status, and monitoring capability. Meter values are read lower-byte then upper-byte. When the lower-byte is read, the upper-byte is latched at the corresponding value. This ensures that multiple byte values correspond to the same reading. Most information can be directly read or written, however, the filter coefficients require an indirect access.

RAM Access Registers

The internal RAMs of the transmit filter, LEC, NEC, DFE, equalizer, and microcode are accessed indirectly. They all share a common data register which is used for both read and write operations, Access Data Register [access_data_byte[3:0]; 0x7C–0x7F]. Each RAM has an individual read select and write select register. These registers specify the location to access and trigger the actual RAM read or write.

To perform a read, the address of the desired RAM location is first written to the corresponding read tap select register. Two symbol periods later, the individual bytes of that location are available for reading from the Access Data Register.

To perform a write, the value to be written is first stored in the Access Data Register. The address of the affected RAM location is then written to the corresponding write tap select register. When writing the same value to multiple locations, it is not necessary to rewrite the Access Data Register.

To assure reliable access to the embedded RAMs, internal read and write operations are performed synchronous to the symbol clock. This has the effect of limiting access to these internal RAMs to one every other cycle.

When reading or writing multiple filter coefficients, it may be desirable to freeze adaptation so that all values will correspond to the same state.

Multiplexed Address-Data Bus

The timing for a read or write cycle is stated explicitly in the Electrical and Mechanical Specifications section. During a read operation, an external microcomputer places an address on the address-data bus which is then latched on the falling edge of ALE. Data is placed on the address-data bus after CS* and RD* (or DS*) go low. The read cycle is completed with the rising edge of CS* and RD* (or DS*).

A write operation latches the address from the address-data bus at the falling edge of ALE. The microcomputer places data on the address-data bus after CS* and WR* (or DS*) go low. Motorola MCI will have R/W* falling edge preceding the falling edge of CS* and DS*. The rising edge of R/W* will occur after the rising edge of CS* and DS*. Data is latched on the address-data bus on the rising edge of WR* or DS*.

Interrupt Request

There are 12 interrupt sources: eight timers, a far-end signal high alarm, a far-end signal low alarm, an SNR alarm, and a scrambler synchronization detection. All of the interrupts are requested on a common pin, IRQ*. Each interrupt may be individually enabled or disabled through the Interrupt Mask Registers [mask_low_reg, mask_high_reg; 0x02, 0x03]. The cause of an interrupt is determined by reading the Timer Source Register [timer_source; 0x04] and the IRQ Source Register [irq_source; 0x05].

Timer interrupts are edge sensitive. The interrupt status is set only when the timer transitions to zero. Alarm interrupts are edge and level sensitive. Level sensitive interrupts cannot be cleared while the alarm is active. In other words, they cannot be cleared while the condition still exists.

IRQ* is an open-drain output and must be tied to a pull-up resistor. This allows IRQ* to be tied together with a common interrupt request.

Reset

The reset input (RST*) is an active-low input that places the transceiver in an inactive state by setting mode [bit 0] in the Global Modes and Status Register [global_modes; 0x00]. An internal supply monitor circuit ensures that the transceiver will be in an inactive state upon initial application of power to the chip.

Registers

The transceiver has many directly addressable registers. These registers include control and monitoring functions. Write operations to undefined registers will have unpredictable effects. Read operations from undefined registers will have undefined results.

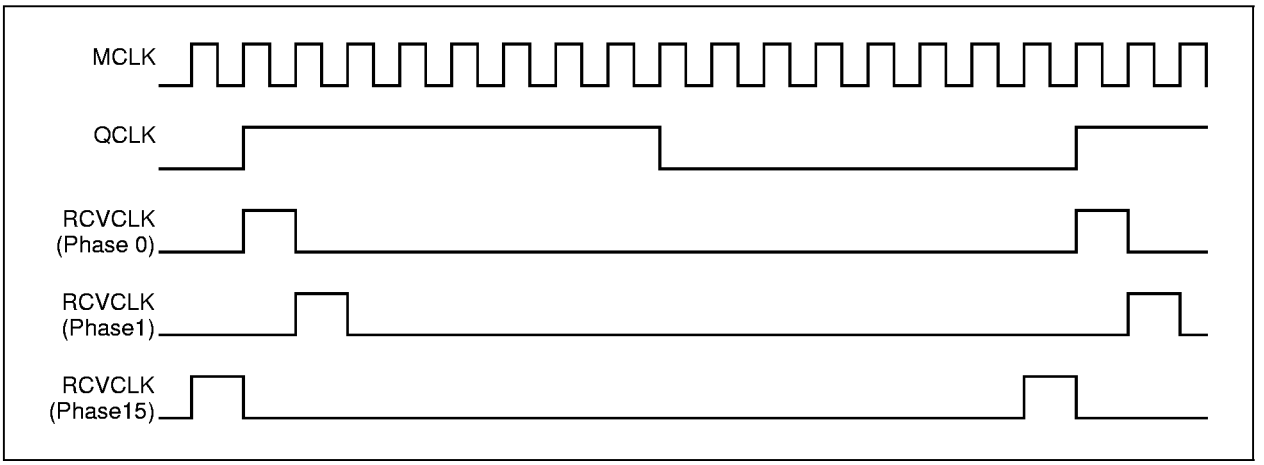
Clock Interface

The clock interface provides synchronization for the transmit and receive sections as well as timing for internal processing.

The master clock (MCLK) operates at 16 or 64 times the symbol (baud) rate, selectable by pin X16/64*. The master clock generates all internal timing as well as QCLK, RCVCLK, and BCLK outputs. In a central-office configuration, MCLK can be supplied by a crystal oscillator or a system clock. A remote-terminal configuration requires that MCLK be frequency synchronized to the central office. This is accomplished with a VCXO implementation of a PLL. The VCXO control voltage is generated from an internal sigma-delta DAC. The output of the sigma-delta DAC requires an RC reconstruction filter between the VCXOC pin and the control voltage input of the VCXO.

An ADC sample clock, RCVCLK, is provided. This clock is derived from MCLK and has 16 phase options which are specified through the Receiver Phase Select Register [receiver_phase_select; 0x07]. The phase relationships of MCLK, QCLK, and RCVCLK, for the case of X16/64* = 1, are illustrated in Figure 12.

Figure 12. Clock Relationship Diagram



Test and Diagnostic Interface

Boundary Scan Testability Structures

As the complexity of communications chips increases, the need to easily access individual chips for PCB verification is becoming vital. As a result, special circuitry has been incorporated within the transceiver which complies fully with IEEE Std 1149.1-1990, "Standard Test Access Port and Boundary Scan Architecture" set by the Joint Test Action Group (JTAG).

JTAG consists of four dedicated pins comprising the Test Access Port (TAP). These pins are Test Mode Select (TMS), Test Clock (TCK), Test Data Input (TDI), and Test Data Out (TDO). Verification of the integrated circuit and its connection to other modules on the printed circuit board can be achieved through these four TAP pins.

JTAG's approach to testability utilizes boundary scan cells placed at each digital pin, both inputs and outputs. All scan cells are interconnected into a boundary-scan register (see Figure 13) which applies or captures test data used for functional verification of the PC board interconnection. JTAG is particularly useful for board testers using functional testing methods.

With boundary-scan cells at each digital pin, the ability to apply and capture the respective logic levels is provided. Since all of the digital pins are interconnected as a long shift register, the TAP logic has access and control of all necessary pins to verify functionality.

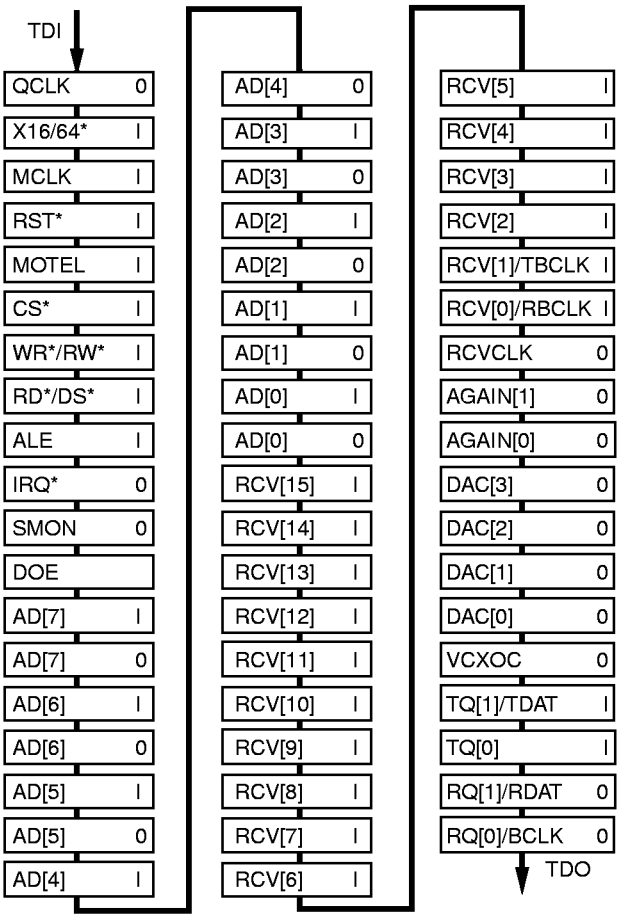
For mixed signal ICs, the chip boundary definition is expanded to include the on-chip interface between digital and analog circuitry. Thus, the digital inputs to the transmitter DAC are included in the boundary scan.

Internal supply monitor circuitry ensures that each pin is initialized to operate as an HDSL transceiver instead of a JTAG test mode during a power-up sequence.

The JTAG standard defines an optional device identification register. This register is included and contains a revision number, a part number, and a manufacturers identification code specific to Brooktree. This register can be accessed through the TAP controller via the standard JTAG instruction set. (See Table 9).

A variety of verification procedures can be performed through the TAP controller. Board connectivity can be verified at all digital pins through a set of four instructions accessible through the use of a state machine standard to all JTAG controllers. Four instructions are accessible through the Instruction Register: Sample/Preload, Extest, IDCode, and Bypass (see Figure 14). Refer to the IEEE 1149.1 specification for details concerning the Instruction Register and JTAG state machine.

Figure 13. Boundary Scan Register



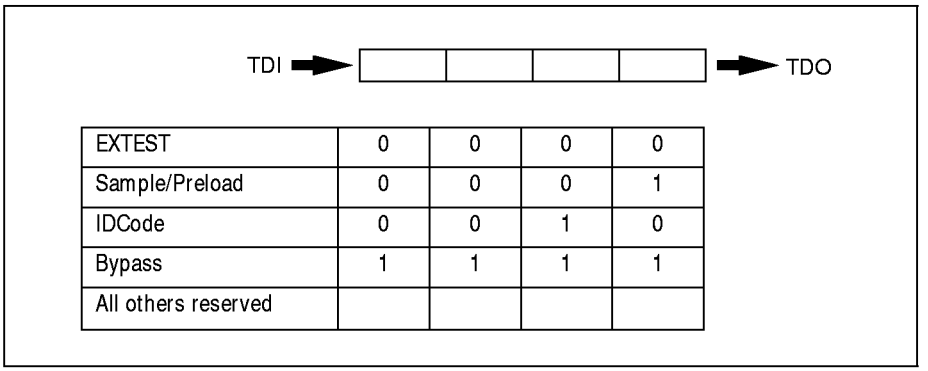
Note: Data Output Enable (DOE): Logic high three-states MCI address-data pins.

e Identification JTAG Register

Part Number																Manufacturer ID										
0	0	1	0	0	0	1	0	1	1	1	1	1	0	0	0	0	0	0	1	1	0	1	0	1		
0x22F8																0x0D6										
16 bits																11 bits										

onsult factory for current version number

Figure 14. Instruction Register (IR)



EXTEST	0	0	0	0
Sample/Preload	0	0	0	1
IDCode	0	0	1	0
Bypass	1	1	1	1
All others reserved				

Registers

Conventions

Unless otherwise noted, the following conventions apply to all applicable register descriptions.

- For storage of multiple-bit data fields within a single byte-wide register, the Least Significant Bits (LSBs) of the field are located at the lower register bit positions while the Most Significant Bits (MSBs) are located at the higher positions.
- If only a single data field is stored in a byte-wide register, the field will be justified such that the LSB of the field is located in the lowest register bit position, bit 0.
- For storage of multiple-byte data words across multiple byte-wide registers, the least significant bytes of the word are located at the lower byte-address locations while the most significant bytes are located at the higher byte-address locations.
- When writing to any control or data register with less than all 8 bit positions defined, a logic zero value must be assigned to each unused/undefined/reserved position. Writing a logic one value to any of these positions may cause undefined behavior.
- When reading from any control/status or data register with less than all 8 bit positions defined, an indeterminate value will be returned from each unused/undefined/reserved position.
- Control/status/data and indirectly addressable RAM locations are not affected by power-up reset or RST* pin assertion. Initial values after power application are undefined. Exceptions include the mode bit of the Global Modes and Status Register [global_modes; 0x00] and the mclk_freq field of the PLL Modes Register [pll_modes; 0x22].

0x00—Global Modes and Status Register (global_modes)

7	6	5	4	3	2	1	0
hw_revision[3]	hw_revision[2]	hw_revision[1]	hw_revision[0]	–	–	–	mode

hw_revision[3:0] Chip Revision Number—Read-only unsigned binary field encoded with the chip revision number. Smaller values represent earlier versions, larger values represent later versions. The zero value represents the original prototype release. Consult factory for current value/revision.

mode Power Down Mode—Read/write control bit. When set, stops all filter processing and zeros the transmit output for reduced power consumption. Transmit filter coefficients and equalizer microcode RAM contents are preserved; all other filter coefficients are lost. Automatically set by RST* assertion and upon initial power application. Can only be cleared by writing a logic zero at which time filter processing and transmitter operation can proceed.

0x01—Serial Monitor Source Select Register (serial_monitor_source)

7	6	5	4	3	2	1	0
–	–	smon[5]	smon[4]	smon[3]	smon[2]	smon[1]	smon[0]

smon[5:0] Serial Monitor Source Select—Read/write binary field selects the serial monitor output (SMON) source.

smon[5:0]		Source
Decimal	Binary	
0–47	00 0000–10 1111	Equalizer Register File
48	11 0000	Digital Front-End Output/LEC Input
49	11 0001	Linear Echo Replica
50	11 0010	DFE Output/EP Input
51	11 0011	EP Output/Slicer Input
52	11 0100	Timing Recovery Phase Detector Output/Loop Filter Input
53	11 0101	Timing Recovery Loop Filter Output/DAC Input

0x02—Interrupt Mask Register Low (mask_low_reg)

Independent read/write mask bits for each of the Timer Source Register [timer_source; 0x04] interrupt flags. A logic one represents the masked condition, a logic zero the unmasked condition. All mask bits behave identically with respect to their corresponding interrupt flags. Setting a mask bit prevents the corresponding interrupt flag from affecting the IRQ* output. Clearing a mask allows the interrupt flag to affect IRQ* output. Unmasking an active interrupt flag will immediately cause the IRQ* output to go active, if currently inactive. Masking an active interrupt flag will cause IRQ* to go inactive, if no other unmasked interrupt flags are set.

7	6	5	4	3	2	1	0
t4	t3	snr	meter	sut4	sut3	sut2	sut1

0x03—Interrupt Mask Register High (mask_high_reg)

Independent read/write mask bits for each of the IRQ Source Register [irq_source; 0x05] interrupt flags. Individual mask bit behavior is identical to that specified for Interrupt Mask Register Low [mask_low_reg; 0x02].

7	6	5	4	3	2	1	0
–	–	–	–	sync	high_felm	low_felm	low_snr

0x04—Timer Source Register (timer_source)

Independent read/write (zero only) interrupt flags, one for each of eight internal timers. Each flag bit is set and stays set when its corresponding timer value transitions from one to zero. If unmasked, this event will cause the IRQ* output to be activated. Flags are cleared by writing them with a logic zero value. Once cleared, a steady-state timer value of zero will not cause a flag to be reasserted. Clearing an unmasked flag will cause the IRQ* output to return to the inactive state, if no other unmasked interrupt flags are set.

7	6	5	4	3	2	1	0
t4	t3	snr	meter	sut4	sut3	sut2	sut1

t4 General Purpose Timer 4

t3 General Purpose Timer 3

snr SNR Alarm Timer

meter Meter Timer

sut4 Start-Up Timer 4

sut3 Start-Up Timer 3

sut2 Start-Up Timer 2

sut1 Start-Up Timer 1

0x05—IRQ Source Register (irq_source)

Independent read/write (zero only) interrupt flags, one for each of four internal sources. Each flag bit is set and stays set when its corresponding source indicates that a valid interrupt condition exists. If unmasked, this event will cause the IRQ* output to be activated. Writing a logic zero to an interrupt flag whose underlying condition no longer exists will cause the flag to be immediately cleared. Attempting to clear a flag whose underlying condition still exists will not immediately clear the flag, but allow it to remain set until the underlying condition expires, at which time the flag will be cleared automatically. The clearing of an unmasked flag will cause the IRQ* output to return to an inactive state, if no other unmasked interrupt flags are set.

7	6	5	4	3	2	1	0
–	–	–	–	sync	high_felm	low_felm	low_snr

sync Sync Indication—Active when the sync detector is enabled and its accumulated equivalent comparisons exceeds (greater than) the threshold value stored in the Scrambler Sync Threshold Register [scr_sync_th; 0x2E].

high_felm Far-End Level Meter High Alarm—Active when the far-end level meter value exceeds (greater than) the threshold stored in the Far-End High Alarm Threshold Register [0x30, 0x31].

low_felm Far-End Level Meter Low Alarm—Active when the far-end level meter value exceeds (less than) the threshold stored in the Far-End Low Alarm Threshold Register [0x32, 0x33].

low_snr Signal-to-Noise Ratio Low Alarm—Active when the SNR Alarm meter value exceeds (greater than) the threshold stored in the SNR Alarm Threshold Register [0x34, 0x35].

0x06—Channel Unit Interface Modes Register (cu_interface_modes)

7	6	5	4	3	2	1	0
–	–	–	tbclk_pol	rbclk_pol	fifos_mode	interface_mode[1]	interface_mode[0]

tbclk_pol Transmit Baud Clock Polarity—Read/write control bit defines the polarity of the TBCLK input while in the parallel slave interface mode. When set, TQ[1,0] is sampled on the falling edge of TBCLK; when cleared, TQ[1,0] is sampled on the rising edge.

rbclk_pol Receive Baud Clock Polarity—Read/write control bit defines the polarity of the RBCLK input while in the parallel slave interface mode. When set, RQ[1,0] is updated on the falling edge of RBCLK; when cleared, RQ[1,0] is updated on the rising edge.

fifos_mode FIFOs Mode—Read/write control bit used to stagger the transmit and receive FIFO's read and write pointers while in the parallel slave interface mode. A logic one forces the pointers to a staggered position while a logic zero allows them to operate normally. Must be first set then cleared once after QCLK-TBCLK-RBCLK frequency lock is achieved to maximize phase-error tolerance.

interface_mode[1,0] Interface Mode—Read/write binary field specifies one of four operating modes for the channel unit interface.

interface_mode [1,0]	Mode	Pin Functions					
		11	12	13	14	16	17
00	Parallel Master. Parallel quat transfer synchronized to QCLK out.	RCV[1]	RCV[0]	RQ[1]	RQ[0]	TQ[1]	TQ[0]
01	Parallel Slave. Parallel quat transfer synchronized to separate TBCLK & RBCLK inputs.	TBCLK	RBCLK	RQ[1]	RQ[0]	TQ[1]	TQ[0]
10	Serial, Mag. First. Serial quat transfer synchronized to BCLK out; magnitude-bit first followed by sign bit.	RCV[1]	RCV[0]	RDAT	BCLK	TDAT	–
11	Serial, Sign First. Serial quat transfer synchronized to BCLK out; sign-bit first followed by magnitude bit.	RCV[1]	RCV[0]	RDAT	BCLK	TDAT	–

0x07—Receive Phase Select Register (receive_phase_select)

7	6	5	4	3	2	1	0
–	–	–	–	rphs[3]	rphs[2]	rphs[1]	rphs[0]

rphs[3:0] Receive Phase Select—Read/write binary field which defines the relative phase relationship between the QCLK and RCVCLK outputs by affecting RCVCLK. The rising edges of QCLK and RCVCLK are aligned when rphs = 0000. Each binary increment of rphs represents a 1/16 QCLK period delay in RCVCLK relative to QCLK. Since RCV[15:0] input sampling is tied to RCVCLK, rphs increments will delay this input sampling as well.

0x08—Linear Echo Canceler Modes Register (linear_ec_modes)

7	6	5	4	3	2	1	0
–	–	enable_dc_tap	adapt_ coefficients	zero_coefficients	zero_output	adapt_gain[1]	adapt_gain[0]

enable_dc_tap Enable DC Tap—Read/write control bit which, when set, forces a constant +1 value into the last data tap of the Linear Echo Canceler (LEC). This condition enables cancelation of any residual DC offset present at the input to the LEC. When cleared, the last data tap operates normally, as the oldest transmit data sample.

adapt_coefficents Adapt Coefficients—Read/write control bit which enables coefficient adaptation when set; disables/freezes adaptation when cleared. Coefficient values are preserved when adaptation is disabled.

zero_coefficients Zero Coefficients—Read/write control bit which continuously zeros all coefficients when set; allows normal coefficient updates, if enabled, when cleared. This behavior differs slightly from the similar function (zero_coefficients) of the Feed Forward Equalizer (FFE) and Error Predictor (EP) filters.

zero_output Zero Output—Read/write control bit which, when set, zeros the echo replica before subtraction from the input signal. Achieves the affect of disabling, or bypassing, the echo cancelation function. Does not disable coefficient adaptation. When cleared, normal echo canceler operation is performed.

adapt_gain[1,0] Adaptation Gain—Read/write binary field which specifies the adaptation gain.

adapt_gain[1,0]	Normalized Gain
00	1
01	4
10	64
11	512

0x09—Nonlinear Echo Canceler Modes Register (nonlinear_ec_modes)

7	6	5	4	3	2	1	0
negate_symbol	symbol_delay[2]	symbol_delay[1]	symbol_delay[0]	adapt_ coefficients	zero_coefficients	zero_output	adapt_gain

negate_symbol Negate Symbol—Read/write control bit which, when set, inverts (two's complement) the receive signal path at the output of the Nonlinear Echo Canceler (NEC). When cleared, the signal path is unaffected. This function is independent of all other NEC mode settings.

symbol_delay[2:0] Symbol Delay—Read/write binary field which specifies the number of symbol delays inserted in the transmit symbol input path.

adapt_coefficients Adapt Coefficients—Same function as Linear Echo Canceler Modes Register [0x08].

zero_coefficients Zero Coefficients—Same function as Linear Echo Canceler Modes Register [0x08].

zero_output Zero Output—Same function as Linear Echo Canceler Modes Register [0x08].

adapt_gain Adaptation Gain—Read/write control bit which specifies the adaptation gain. When set, the adaptation gain is eight times higher than when cleared.

0x0A—Decision Feedback Equalizer Modes Register (dfe_modes)

7	6	5	4	3	2	1	0
–	–	–	timing_function	adapt_ coefficients	zero_coefficients	zero_output	adapt_gain

timing_function Timing Function—Read/write control bit which, when set, places the Decision Feedback Equalizer (DFE) in the special timing function calculation mode. Coefficient adaptation must be disabled for proper operation. While in this mode, the sum of the first 29 odd DFE coefficients (C1, C3, ..., C57) is subtracted from the sum of the first 29 even coefficients (C0, C2, ..., C56). The absolute value of the result is placed in the Timing Function Result Register [0x52, 0x53]. When this control bit is cleared, the regular DFE function is performed.

adapt_coefficents Adapt Coefficients—Read/write control bit which enables coefficient adaptation when set; disables/freezes adaptation when cleared. Coefficient values are preserved when adaptation is disabled.

zero_coefficients Zero Coefficients—Read/write control bit which continuously zeros all coefficients when set; allows normal coefficient updates, if enabled, when cleared.

zero_output Zero Output—Read/write control bit which, when set, zeros the equalizer correction signal before subtraction from the input signal. Achieves the affect of disabling, or bypassing, the equalization function. Does not disable coefficient adaptation. When cleared, normal equalizer operation is performed.

adapt_gain Adaptation Gain—Read/write control bit which specifies the adaptation gain. When set, the adaptation gain is eight times higher than when cleared.

0x0B—Transmitter Modes Register (transmitter_modes)

7	6	5	4	3	2	1	0
–	isolated_pulse[1]	isolated_pulse[0]	transmitter_off	htur_lfsr	data_source[2]	data_source[1]	data_source[0]

isolated_pulse[1,0] Isolated Pulse Level Select—Read/write binary field selects one of four output pulse levels while in the isolated pulse transmitter mode.

isolated_pulse[1,0]	Output Pulse Level
00	–3
01	–1
10	+3
11	+1

transmitter_off Transmitter Off—Read/write control bit zeros the output of the transmitter when set; allows normal transmitter operation (as defined by data_source[2:0]) when cleared.

htur_lfsr HTU-R Polynomial Select—Read/write control bit selects one of two feedback polynomials for the transmit scrambler. When set, selects the ANSI/ETSI standard HTU-R/NTU transmit polynomial ($x^{-23} + x^{-18} + 1$); when cleared, selects the HTU-C/LTU polynomial ($x^{-23} + x^{-5} + 1$).

data_source[2:0] Data Source—Read/write binary field selects the data source and mode of the transmitter output. The transmitter must be enabled (transmitter_off = 0) for these modes to be active.

data_source[2:0]	Transmitter Mode
000	**Isolated pulse**. Level selected by isolated_pulse[1,0]. The meter timer must be enabled and in the continuous mode. The pulse repetition interval is determined by the meter timer countdown interval.
001	**Four-level scrambled detector loop-back**. Sign and magnitude bits from the receiver detector are scrambled and looped back to the transmitter. Feedback polynomial determined by the htur_lfsr control bit.
010	**Four-level unscrambled data**. Transmits the four-level (2B1Q) sign and magnitude bits from the channel unit transmit interface without scrambling.
011	**Four-level scrambled ones**. Transmits a scrambled, constant high logic level as a four-level (2B1Q) signal. Feedback polynomial determined by the htur_lfsr control bit.
100	**Reserved**.
101	**Four-level scrambled data**. Scrambles and transmits the four-level (2B1Q) sign and magnitude bits from the channel unit transmit interface. Feedback polynomial determined by the htur_lfsr control bit.
110	**Two-level unscrambled data**. Constantly forces the magnitude bit from the channel unit transmit interface to a logic zero and transmits the resulting two-level signal (as determined by the sign bit) without scrambling. Valid output levels limited to +3, –3.
111	**Two-level scrambled ones**. Transmits a scrambled, constant high logic level as a two-level signal. Feedback polynomial determined by the htur_lfsr control bit. Scrambler is run at the symbol rate (1/2 bit rate) to produce the sign bit of the transmitted signal while the magnitude bit is sourced with a constant logic zero. Valid output levels limited to +3, –3.

0x0C—Timer Restart Register (timer_restart)

Independent read/write restart bits, one for each of eight internal timers. Setting an individual bit causes the associated timer to be reloaded with the contents of its interval register. For the four symbol-rate timers (meter, snr, t3, t4), reloading will occur within one symbol period. For the four start-up timers (sut1–4), reloading will occur within 1024 symbol periods. Once reloaded, the restart bit is automatically cleared. If a restart bit is set and then cleared (by writting a logic zero) before the reload actually takes place, no timer reload will occur. Once reloaded, if enabled in the Timer Enable Register [0x0D], the timer will begin counting down toward zero; otherwise, it will hold at the interval register value.

7	6	5	4	3	2	1	0
t4	t3	snr	meter	sut4	sut3	sut2	sut1

t4 General Purpose Timer 4

t3 General Purpose Timer 3

snr SNR Alarm Timer

meter Meter Timer

sut4 Start-Up Timer 4

sut3 Start-Up Timer 3

sut2 Start-Up Timer 2

sut1 Start-Up Timer 1

0x0D—Timer Enable Register (timer_enable)

Independent read/write enable bits, one for each of eight internal timers. When any individual bit is set, the corresponding timer is enabled for counting down from its current value toward zero. For the four symbol-rate timers (meter, snr, t3, t4), counting will begin within one symbol period. For the four start-up timers (sut1-4), counting will begin within 1024 symbol periods. When an enable bit is cleared, the timer is disabled from counting while it holds its current value. If an enable bit is set and then cleared before a count actually takes place, no timer countdown will occur.

7	6	5	4	3	2	1	0
t4	t3	snr	meter	sut4	sut3	sut2	sut1

0x0E—Timer Continuous Mode Register (timer_continuous)

Independent read/write mode bits, one for each of eight internal timers. When any individual bit is set, the corresponding timer is placed in the continuous count mode. While in this mode, after reaching the zero count, an enabled timer will reload the contents of its interval register and continue counting. When a mode bit is cleared, the timer is taken out of the continuous mode. While in this configuration, after reaching the zero count, an enabled timer will simply stop counting and remain at zero.

7	6	5	4	3	2	1	0
t4	t3	snr	meter	sut4	sut3	sut2	sut1

0x10, 0x11—Start-Up Timer 1 Interval Register (sut1_low, sut1_high)

Two-byte read/write register stores the countdown interval for Start-up Timer 1 in unsigned binary format. Each increment represents 1024 symbol periods. The contents of this register are automatically loaded into its associated timer after the timer's timer_restart bit is set or after it counts down to zero while in the continuous mode.

0x12, 0x13—Start-Up Timer 2 Interval Register (sut2_low, sut2_high)

Two-byte read/write register stores the countdown interval for Start-up Timer 2 in unsigned binary format. Each increment represents 1024 symbol periods. The contents of this register are automatically loaded into its associated timer after the timer's timer_restart bit is set or after it counts down to zero while in the continuous mode.

0x14, 0x15—Start-Up Timer 3 Interval Register (sut3_low, sut3_high)

Two-byte read/write register stores the countdown interval for Start-up Timer 3 in unsigned binary format. Each increment represents 1024 symbol periods. The contents of this register are automatically loaded into its associated timer after the timer's timer_restart bit is set or after it counts down to zero while in the continuous mode.

0x16, 0x17—Start-Up Timer 4 Interval Register (sut4_low, sut4_high)

Two-byte read/write register stores the countdown interval for Start-up Timer 4 in unsigned binary format. Each increment represents 1024 symbol periods. The contents of this register are automatically loaded into its associated timer after the timer's timer_restart bit is set or after it counts down to zero while in the continuous mode.

0x18, 0x19—Meter Timer Interval Register (meter_low, meter_high)

Two-byte read/write register stores the countdown interval for the Meter Timer in unsigned binary format. Each increment represents one symbol period. The contents of this register are automatically loaded into its associated timer after the timer's timer_restart bit is set or after it counts down to zero while in the continuous mode.

0x1A, 0x1B—SNR Alarm Timer Interval Register (snr_timer_low, snr_timer_high)

Two-byte read/write register stores the countdown interval for the SNR Alarm Timer in unsigned binary format. Each increment represents one symbol period. The contents of this register are automatically loaded into its associated timer after the timer's timer_restart bit is set or after it counts down to zero while in the continuous mode.

0x1C, 0x1D—General Purpose Timer 3 Interval Register (t3_low, t3_high)

Two-byte read/write register stores the countdown interval for General Purpose Timer 3 in unsigned binary format. Each increment represents one symbol period. The contents of this register are automatically loaded into its associated timer after the timer's timer_restart bit is set or after it counts down to zero while in the continuous mode.

0x1E, 0x1F—General Purpose Timer 4 Interval Register (t4_low, t4_high)

Two-byte read/write register stores the countdown interval for General Purpose Timer 4 in unsigned binary format. Each increment represents one symbol period. The contents of this register are automatically loaded into its associated timer after the timer's timer_restart bit is set or after it counts down to zero while in the continuous mode.

0x20— ADC Bit Width Register (adc_bit_width)

7	6	5	4	3	2	1	0
–	–	–	–	–	–	width[1]	width[0]

width[1,0] ADC Width—Read/write binary field specifies the number of Receive Data Interface bits (RCV[15:0]) processed during overflow calculations. The specified number of MSBs are used to compute overflow while any residual LSBs (0, 2, or 4 bits) are ignored. The contents of this field affect overflow calculations only; they have no effect on the precision of any receiver processing functions.

width[1,0]	MSBs in Overflow Calculation
00	16 bits
01	14 bits
10	12 bits
11	Reserved

0x21— ADC Gain Control Register (adc_control)

7	6	5	4	3	2	1	0
–	–	–	–	–	adc_cont_fix_gain	again[1]	again[0]

adc_cont_fix_gain Continuous External AGC Mode—Read/write mode bit defines the behavior of the AGAIN[1] output pin (pin 46). When set, continuous external AGC is selected and the AGAIN[1] pin is automatically updated by the receiver's continuous external AGC function. When cleared, fixed external AGC is selected and the AGAIN[1] pin simply tracks the value of the again[1] data bit.

again[1] Again 1—Read/write data bit specifies the value to be driven onto the AGAIN[1] output pin (pin 46) while in the fixed external AGC mode (adc_cont_fix_gain = 0). While in the continuous external AGC mode (adc_cont_fix_gain = 1), this data bit is not used.

again[0] Again 0—Read/write data bit specifies the value to be driven onto the AGAIN[0] output pin (pin 45). The value of again[0] is always driven onto the AGAIN[0] output pin regardless of the type of external AGC selected.

0x22— PLL Modes Register (pll_modes)

7	6	5	4	3	2	1	0
mclk_freq[1]	mclk_freq[0]	negate_symbol	phase_detector_ gain[1]	phase_detector_ gain[0]	freeze_pll	pll_gain[1]	pll_gain[0]

mclk_freq[1,0] MCLK Frequency Select—Read/write binary field specifies one of four frequency ranges for the MCLK input signal (pin 57) when using the internal 16x clock multiplier. Pulling the X16/64* input signal high (pin 56 = 1) selects this mode. The 00 state is automatically selected by RST* assertion and upon initial power application. If the internal clock multiplier is not used (pin 56 = 0), this field has no effect on performance.

mclk_freq[1,0]	Nominal MCLK Center Frequency	Resulting QCLK Center Frequency
00	9.344 MHz	584 kHz
01	6.272 MHz	392 kHz
10	16.448 MHz to 18.560 MHz	1028 kHz to 1160 kHz
11	12.416 MHz	776 kHz

negate_symbol Negate Input Symbol—Read/write control bit inverts the sign of the timing-recovery phase detector symbol input when set; has no effect on the symbol input when cleared. A logic zero value in negate_symbol configures the timing recovery function to generate a positive slope VCXO control voltage (frequency increases with increasing voltage) on pin 55 (VCXOC) while a logic one generates a negative slope control voltage (frequency decreases with increasing voltage).

phase_detector_ gain[1,0] Phase Detector Gain—Read/write binary field specifies one of four gain settings for the timing recovery phase detector function.

phase_detector_gain[1,0]	Normalized Gain
00	1
01	2
10	4
11	8

freeze_pll Freeze PLL—Read/write control bit zeros the proportional term of the loop compensation filter and disables accumulator updates when set. Causes the reconstructed VCXOC output (pin 55) to remain at a fixed voltage level. When cleared, proportional term effects and accumulator updates are enabled, allowing normal VCXOC output behavior to occur.

pll_gain PLL Gain—Read/write binary field specifies the gain (proportional and integral coefficients) of the loop compensation filter.

pll_gain[1,0]	Normalized Proportional Coefficients	Normalized Integral Coefficients
00	1	1
01	4	32
10	16	256
11	64	4096

0x24, 0x25—Timing Recovery PLL Phase Offset Register (pll_phase_offset_low, pll_phase_offset_high)

Two-byte read/write register interpreted as a 16-bit two's-complement number. The value of this register is subtracted from the output of the timing recovery phase detector after the phase detector meter but before the loop compensation filter.

0x26, 0x27—Receiver DC Offset Register (dc_offset_low, dc_offset_high)

Two-byte read/write register interpreted as a 16-bit two's-complement number. The value of this register is subtracted from the receiver signal path at the output of the digital front end's format conversion block, ahead of the DC level and signal level meters.

0x28, 0x29—External AGC Target Register (agc_target_low, agc_target_high)

Two-byte read/write register interpreted as a 16-bit two's-complement number. The range of meaningful values is limited to positive integers between 0 and 7FFF hex. The value of this register is compared to the absolute value of the receiver signal path at the output of the digital front end, ahead of the echo cancelers. While in the continuous external AGC mode, the result of this comparison is used to drive the level of the AGAIN[1] output pin (pin 46). In the fixed external AGC mode, the result of this comparison is not used.

0x2A, 0x2B—Noise-Level Histogram Threshold Register (noise_histogram_th_low, noise_histogram_th_high)

Two-byte read/write register interpreted as a 16-bit two's-complement number. The range of meaningful values is limited to positive integers between 0 and 7FFF hex. The value of this register is compared to the absolute value of the slicer error signal produced by the detector. A count of error samples which exceed this threshold (greater than) is accumulated in the noise level histogram meter.

0x2C, 0x2D—Error Predictor Pause Threshold Register (ep_pause_th_low,

ep_pause_th_high)

Two-byte read/write register interpreted as a 16-bit two's-complement number. The range of meaningful values is limited to positive integers between 0 and 7FFF hex. The value of this register is compared to the absolute value of the slicer error signal produced by the detector. The result of this comparison (slicer error greater than this threshold) is used to initiate a pause condition by zeroing the output of the error predictor correction signal before subtraction from the receive signal path. Error predictor coefficient updates are not affected. The pause condition lasts for a fixed 5-symbol period from the time the threshold was last exceeded.

0x2E— Scrambler Synchronization Threshold Register (scr_sync_th)

Seven-bit read/write register representing an unsigned binary number. The contents of this register are used to test for scrambler synchronization during the automatic scrambler synchronization mode of the symbol detector. The test passes when the count of equivalent scrambler and detector output bits exceeds (greater than) the value of this register. When the auto scrambler sync mode is not enabled, the contents of this register are not used.

7	6	5	4	3	2	1	0
–	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x30, 0x31— Far-End High Alarm Threshold Register (far_end_high_alarm_th_low, far_end_high_alarm_th_high)

Two-byte read/write register interpreted as a 16-bit two's-complement number. The range of meaningful values is limited to positive integers between 0 and 7FFF hex. The value of this register is compared to the value of the far-end level meter. If the meter reading exceeds (greater than) this threshold, the high_felm interrupt flag is set in the IRQ Source Register [0x05].

0x32, 0x33— Far-End Low Alarm Threshold Register (far_end_low_alarm_th_low, far_end_low_alarm_th_high)

Two-byte read/write register interpreted as a 16-bit two's-complement number. The range of meaningful values is limited to positive integers between 0 and 7FFF hex. The value of this register is compared to the value of the far-end level meter. If the meter reading exceeds (less than) this threshold, the low_felm interrupt flag is set in the IRQ Source Register [0x05].

0x34, 0x35— SNR Alarm Threshold Register (snr_alarm_th_low, snr_alarm_th_high)

Two-byte read/write register interpreted as a 16-bit two's-complement number. The range of meaningful values is limited to positive integers between 0 and 7FFF hex. The value of this register is compared to the value of the SNR alarm meter. If the meter reading exceeds (greater than) this threshold, the low_snr interrupt flag is set in the IRQ Source Register [0x05].

0x36, 0x37— Cursor Level Register (cursor_level_low, cursor_level_high)

Two-byte read/write register interpreted as a 16-bit two's-complement number. The range of meaningful values is limited to positive integers between 0 and 2AAA hex (1/3 of the maximum positive value). The value of this register represents the expected level of a noise-free +1 receive symbol at the output of the DFE. It is multiplied by two to produce the positive and negative slicing levels, in addition to zero, used by the symbol detector in four-level slicing mode. This value is also used to scale the detector output when computing the equalizer error and slicer error signals. The detected symbol (–3, –1, +1, +3) is multiplied by the value of this register to produce the scaled output.

0x38, 0x39— DAGC Target Register (dagc_target_low, dagc_target_high)

Two-byte read/write register interpreted as a 16-bit two's-complement number. The range of meaningful values is limited to positive integers between 0 and 7FFF hex. The value of this register is subtracted from the absolute value of the receive signal at the output of the Digital Automatic Gain Control (DAGC) function. The difference is used as the error input to the DAGC while in the self-adaptation mode. In the DAGC's equalizer-error adaptation mode, the contents of this register are not used.

0x3A— Symbol Detector Modes Register (detector_modes)

7	6	5	4	3	2	1	0
enable_peak_ detector	output_mux_ control[1]	output_mux_ control[0]	scr_out_to_dfe	two_level	lfsr_lock	htur_lfsr	descr_on

enable_peak_detector Enable Peak Detector—Read/write control bit enables the peak detection function when set; disables the function when cleared. When enabled, the peak detector output overrides the slicer output if the peak detection criteria are met. If the criteria are not met, or if the function is disabled, the slicer output is used and peak detector output is ignored.

output_mux_ control[1,0] Output Multiplexer Control—Read/write binary field selects the source of the detector output connected to the channel unit receive interface.

output_mux_ control[1,0]	Detector Output to CU Receive Interface
00	Same as scr_out_to_dfe selection.
01	Transmitter loopback output from CU transmit interface.
10	Scrambler/descrambler output.
11	Reserved.

scr_out_to_dfe Scrambler Output to DFE—Read/write control bit selects the source of the detector output connected to the DFE and timing recovery module inputs, and the transmitter's detector loopback input. When set, selects the scrambler/descrambler function; when cleared, selects the slicer/peak detector output.

two_level Two-Level Mode—Read/write control bit selects two-level mode when set, four-level mode when cleared. Affects the slicer and the scrambler/descrambler function. In two-level mode, the slicer uses a single threshold set at zero to recover sign bits only; all magnitude information is lost. Scrambler/descrambler updates are slowed to the symbol rate (1/2 the normal bit rate)

to process only sign information as well; all magnitude output bits are sourced with a constant logic-zero value producing two-level symbols constrained to +3 and –3 values.

In four-level mode, the slicer uses two thresholds derived from the Cursor Level Register [0x36, 0x37], as well as the zero threshold, to recover both sign and magnitude information. The scrambler/descrambler is updated at the full bit rate to process both sign and magnitude bits as well.

lfsr_lock LFSR Lock—Read/write control bit enables the auto scrambler synchronization mode (lfsr_lock) in the detector when set; disables this mode when cleared. Affects the behavior of the scrambler/descrambler function, overriding the descr_on setting. When enabled, the scrambler/descrambler is forced into the descrambler mode for 23 cycles. It is then switched to the scrambled-ones mode for 128 cycles. While in this mode, the outputs of the scrambler and the slicer/peak detector are compared against one another. The number of equivalent bits (equal comparisons) is accumulated and compared to the value of the Scrambler Synchronization Threshold Register [0x2E].

At any time during the 128 cycles, if the count exceeds the threshold (greater than), the sync interrupt flag is set in the IRQ Source Register [0x05] and the process terminates with the scrambler/descrambler left in the scrambled-ones mode. (The sync interrupt flag cannot be cleared while lfsr_lock remains high.) After 128 cycles, if the threshold is not exceeded, the accumulator is cleared, the scrambler/descrambler re-enters the descrambler mode for another 23 cycles, and the process repeats until either sync is achieved or this mode is disabled. Once disabled, the sync interrupt flag can be cleared (if active) and the scrambler/descrambler returns to the mode specified by descr_on.

htur_lfsr HTU-R Polynomial Select—Read/write control bit selects one of two feedback polynomials for the scrambler/descrambler. When set, selects the ANSI/ETSI standard HTU-R/NTU receive polynomial ($x^{-23} + x^{-5} + 1$); when cleared, selects the HTU-C/LTU polynomial ($x^{-23} + x^{-18} + 1$).

descr_on Descrambler/Scrambler Select—Read/write control bit configures the scrambler/descrambler function as a descrambler when set, and as a scrambler when cleared. As a scrambler, this bit can only generate a scrambled all-ones sequence (constant high logic-level input); all incoming data is ignored. In the auto scrambler synchronization mode (lfsr_lock = 1), this selection is overwritten though the value of the control bit is unaffected.

0x3B— Peak Detector Delay Register (peak_detector_delay)

Four-bit read/write register interpreted as an unsigned binary number. Specifies a number of additional symbol delays inserted in the peak-detector input path of the symbol detector. Must be set to a value that equalizes the total path delay in each of the peak detector and slicer input paths according to the following formula: peak detector delay register value = DAGC delays + FFE delays – fixed peak detector input delays. The DAGC and FFE delays are not fixed, but result from the microprogrammed implementation of these functions. If used unmodified, they equal 0 and 7, respectively. The fixed peak detector input delay is equal to 3.

7	6	5	4	3	2	1	0
D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x3C— Digital AGC Modes Register (dagc_modes)

7	6	5	4	3	2	1	0
–	–	–	–	–	eq_error_ adaptation	adapt_coefficient	adapt_gain

eq_error_ adaptation Equalizer Error Adaptation—Read/write control bit selects between the equalizer-error adaptation mode when set; and the self adaptation mode when cleared. Equalizer-error adaptation uses the equalizer error signal produced by the slicer as the DAGC error input signal. In self adaptation, the value of the DAGC Target Registers [0x38, 0x39] is subtracted from the absolute value of the receive signal at the output of the DAGC, and this difference is used as the error input signal.

adapt_coefficient Adapt Coefficients—Read/write control bit enables coefficient adaptation when set; disables/freezes adaptation when cleared. Coefficient values are preserved when adaptation is disabled.

adapt_gain Adaptation Gain—Read/write control bit specifies the adaptation gain. When set, the adaptation gain is eight times higher than when cleared.

0x3D— Feed Forward Equalizer Modes Register (ffe_modes)

7	6	5	4	3	2	1	0
–	–	–	–	adapt_last_coeff	zero_coefficents	adapt_ coefficients	adapt_gain

adapt_last_coeff Adapt Last Coefficient—Read/write control bit enables adaptation of the last (oldest) coefficient only when set; allows all coefficient adaptation when cleared. Overall coefficient adaptation must be enabled (adapt_coefficients = 1) for this behavior to occur. If coefficient adaptation is disabled (adapt_coefficients = 0), the value of this control bit is not used.

zero_coefficients Zero Coefficients—Read/write control bit which, with coefficient adaptation enabled (adapt_coefficients = 1), continuously zeros all coefficients when set; allows normal coeffi-

cient updates when cleared. If coefficient adaptation is disabled (adapt_coefficients = 0), this control bit has no affect. This behavior differs slightly from the similar function (zero_coefficients) of the LEC, NEC, and DFE filters.

adapt_coefficents Adapt Coefficients—Read/write control bit enables coefficient adaptation when set; disables/freezes adaptation when cleared. Coefficient values are preserved when adaptation is disabled. This overall coefficient adaptation must be enabled for adapt_last_coeff to have an affect.

adapt_gain Adaptation Gain—Read/write control bit specifies the adaptation gain. When set, the adaptation gain is four times higher than when cleared.

0x3E— Error Predictor Modes Register (ep_modes)

7	6	5	4	3	2	1	0
-	-	-	-	zero_output	zero_coefficients	adapt_ coefficients	adapt_gain

zero_output Zero Output—Read/write control bit which, when set, zeros the error predictor correction signal before subtraction from the input signal. Achieves the affect of disabling, or bypassing, the error predictor function. Does not disable coefficient adaptation. When cleared, normal error predictor operation is performed.

zero_coefficients Zero Coefficients—Read/write control bit which, with coefficient adaptation enabled (adapt_coefficients = 1), continuously zeros all coefficients when set; allows normal coefficient updates when cleared. If coefficient adaptation is disabled (adapt_coefficients = 0), this control bit has no affect. This behavior differs slightly from the similar function (zero_coefficients) of the LEC, NEC, and DFE filters.

adapt_coefficents Adapt Coefficients—Read/write control bit enables coefficient adaptation when set; disables/freezes adaptation when cleared. Coefficient values are preserved when adaptation is disabled.

adapt_gain Adaptation Gain—Read/write control bit specifies the adaptation gain. When set, the adaptation gain is four (4) times higher than when cleared.

0x40, 0x41—Phase Detector Meter Register (pdm_low, pdm_high)

Two-byte read-only register containing the 16 MSBs of the 26-bit two's-complement phase detector meter accumulator. This meter sums the output of the timing recovery module's phase detector—prior to being offset by the Timing Recovery PLL Phase Offset Registers [0x24, 0x25]—over each Meter Timer countdown interval. Automatically loaded at the end of each interval, the meter register must be read low byte first, followed by high byte, unseparated by any timing function, VCXO-frequency, or other meter register read access.

7	6	5	4	3	2	1	0
D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]
D[25]	D[24]	D[23]	D[22]	D[21]	D[20]	D[19]	D[18]

0x42—Overflow Meter Register (overflow_meter)

Single-byte read-only register containing all 8 bits of the unsigned overflow meter accumulator. This meter counts the number of Receive Data Interface (RCV[15:0]) overflow conditions which occur during each Meter Timer countdown interval, limited to a maximum count of 255 (FF hex). An overflow condition is defined as all unmasked input bits, as specified by the ADC Bit Width Register [0x20], being equal to logic one or all being equal to logic zero. The meter register is automatically loaded at the end of each countdown interval.

7	6	5	4	3	2	1	0
D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x44, 0x45—DC Level Meter Register (dc_meter_low, dc_meter_high)

Two-byte read-only register containing the 16 MSBs of the 32-bit two's-complement DC-level meter accumulator. This meter sums the value of the receive signal input path—after format conversion and DC offset correction but before echo cancelation—over each Meter Timer countdown interval. Automatically loaded at the end of each interval, the meter register must be read low byte first, followed by high byte, unseparated by any timing function, VCXO frequency, or other meter register read access.

7	6	5	4	3	2	1	0
D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]
D[31]	D[30]	D[29]	D[28]	D[27]	D[26]	D[25]	D[24]

0x46, 0x47— Signal Level Meter Register (slm_low, slm_high)

Two-byte read-only register containing the 16 MSBs of the 32-bit unsigned signal-level meter accumulator. This meter sums the absolute value of the receive signal input path—after format conversion and DC offset correction but before echo cancelation (same point as the DC level meter)—over each Meter Timer countdown interval. Automatically loaded at the end of each interval, the meter register must be read low byte first, followed by high byte, unseparated by any timing function, VCXO frequency, or other meter register read access.

7	6	5	4	3	2	1	0
D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]
D[31]	D[30]	D[29]	D[28]	D[27]	D[26]	D[25]	D[24]

0x48, 0x49— Far-End Level Meter Register (felm_low, felm_high)

Two-byte read-only register containing the 16 MSBs of the 32-bit unsigned far-end level meter accumulator. This meter sums the absolute value of the receive signal path—after echo cancelation but before the DAGC function—over each Meter Timer countdown interval. Automatically loaded at the end of each interval, the meter register must be read low byte first, followed by high byte, unseparated by any timing function, VCXO frequency, or other meter register read access.

7	6	5	4	3	2	1	0
D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]
D[31]	D[30]	D[29]	D[28]	D[27]	D[26]	D[25]	D[24]

0x4A, 0x4B— Noise-Level Histogram Meter Register (noise_histogram_low, noise_histogram_high)

Two-byte read-only register containing all 16 bits of the unsigned noise-level histogram meter accumulator. This meter counts the number of high-noise-level conditions which occur during each Meter Timer countdown interval. A high-noise-level condition is defined as the absolute value of the slicer error signal exceeding (greater than) the threshold specified in the Noise-Level Histogram Threshold Registers [0x2A, 0x2B]. Automatically loaded at the end of each countdown interval, the meter register must be read low byte first, followed by high byte, unseparated by any timing function, VCXO frequency, or other meter register read access.

7	6	5	4	3	2	1	0
D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]

0x4C, 0x4D—Bit Error Rate Meter Register (ber_meter_low, ber_meter_high)

Two-byte read-only register containing all 16 bits of the unsigned bit-error-rate meter accumulator. This meter counts the number of error-free bits recovered by the detector during each Meter Timer countdown interval. An error-free bit is defined as a match (equal comparison) of the detector's slicer/peak detector output and its scrambler/descrambler output, when operating as a scrambler. When operating as a descrambler, the meter simply counts the number of logic ones produced by the descrambler. The meter register is automatically loaded at the end of each countdown interval, and must be read low byte first, followed by high byte, unseparated by any timing function, VCXO frequency, or other meter register read access.

7	6	5	4	3	2	1	0
D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]

0x4E—Symbol Histogram Meter Register (symbol_histogram)

Single-byte read-only register containing the 8 MSBs of the 16-bit unsigned symbol histogram meter accumulator. This meter counts the number of plus-one or minus-one symbols (+1, –1) detected during each Meter Timer countdown interval. No increment occurs when a plus-three or minus-three symbol (+3, –3) is detected. The meter register is automatically loaded at the end of each countdown interval.

7	6	5	4	3	2	1	0
D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x50, 0x51—Noise Level Meter Register (nlm_low, nlm_high)

Two-byte read-only register containing the 16 MSBs of the 32-bit unsigned noise-level meter accumulator. This meter sums the absolute value of the detector's slicer-error signal over each Meter Timer countdown interval. Automatically loaded at the end of each interval, the meter register must be read low byte first, followed by high byte, unseparated by any timing function, VCXO frequency, or other meter register read access.

7	6	5	4	3	2	1	0
D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]
D[31]	D[30]	D[29]	D[28]	D[27]	D[26]	D[25]	D[24]

0x52, 0x53— Timing Function Result Register (timing_function_result_low, timing_function_result_high)

Two-byte read-only register containing the 16-bit DFE timing-function result. Formatted as a positive two's-complement number between 0 and 7FFF hex, this register is automatically loaded each symbol period whenever the DFE timing function is enabled (timing_function = 1 in DFE Modes Register [0x0A]). When the timing function is disabled, the value of this register remains unaffected. Treated much like a meter register, the result register must be read low byte first, followed by high byte, unseparated by any VCXO frequency or meter register read access.

7	6	5	4	3	2	1	0
D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]

0x5E, 0x5F— VCXO Frequency Register (vcxo_frequency_low, vcxo_frequency_high)

Two-byte read/write register comprising the 16 MSBs of the 31-bit two's-complement timing recovery loop compensation filter accumulator. The accumulator's value is a digital representation of the VCXOC output pin's (pin 55) filtered control voltage level. A frequency register/accumulator value of zero represents a filtered control voltage level of VDD2 ÷2 relative to VSS2. Positive accumulator values represent more positive control voltages while negative accumulator values represent less positive control voltages. Maximum/minimum accumulator values represent VDD2/VSS2 voltage levels, respectively. Treated much like a meter register, the frequency register must be read low byte first, followed by high byte, unseparated by any timing function or meter register read access. Writes must occur in the same order, with the low byte written first, followed by the high byte. Write accesses may be separated by any number of other read or write accesses.

7	6	5	4	3	2	1	0
D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]	D[15]
D[30]	D[29]	D[28]	D[27]	D[26]	D[25]	D[24]	D[23]

0x70— LEC Read Tap Select Register (linear_ec_tap_select_read)

Seven-bit read/write register representing an unsigned binary address defined over a range of 0 to 119 decimal. When written, this register causes the selected 32-bit coefficient of the LEC to be subsequently loaded into the Access Data Register [0x7C–0x7F] within two symbol periods. Does not affect the value of the coefficient.

7	6	5	4	3	2	1	0
–	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x71— LEC Write Tap Select Register (linear_ec_tap_select_write)

Seven-bit read/write register representing an unsigned binary address defined over a range of 0 to 119 decimal. When written, this register causes all 32 bits of the Access Data Register [0x7C–0x7F] to be subsequently written to the selected LEC coefficient within two symbol periods. Does not affect the value of the Access Data Register.

7	6	5	4	3	2	1	0
–	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x72— NEC Read Tap Select Register (nonlinear_ec_tap_select_read)

Six-bit read/write register representing an unsigned binary address defined over a range of 0 to 63 decimal. When written, this register causes the selected 14-bit coefficient of the NEC to be subsequently loaded into the lowest-order bits of the Access Data Register [0x7C–0x7F] within two symbol periods. Does not affect the value of the coefficient.

7	6	5	4	3	2	1	0
–	–	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x73— NEC Write Tap Select Register (nonlinear_ec_tap_select_write)

Six-bit read/write register representing an unsigned binary address defined over a range of 0 to 63 decimal. When written, this register causes the lowest-order 14 bits of the Access Data Register [0x7C–0x7F] to be subsequently written to the selected NEC coefficient within two symbol periods. Does not affect the value of the Access Data Register.

7	6	5	4	3	2	1	0
–	–	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x74— DFE Read Tap Select Register (dfe_tap_select_read)

Seven-bit read/write register representing an unsigned binary address defined over a range of 0 to 113 decimal. When written, this register causes the selected 16-bit coefficient of the DFE to be subsequently loaded into the lowest-order bits of the Access Data Register [0x7C–0x7F] within two symbol periods. Does not affect the value of the coefficient.

7	6	5	4	3	2	1	0
–	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x75— DFE Write Tap Select Register (dfe_tap_select_write)

Seven-bit read/write register representing an unsigned binary address defined over a range of 0 to 113 decimal. When written, this register causes the lowest-order 16 bits of the Access Data Register [0x7C–0x7F] to be sub-

sequently written to the selected DFE coefficient within two symbol periods. Does not affect the value of the Access Data Register.

7	6	5	4	3	2	1	0
–	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x76— Transmit Filter Read Tap Select Register (tx_tap_select_read)

Six-bit read/write register representing an unsigned binary address defined over a range of 0 to 63 decimal. When written, this register causes the selected 8-bit coefficient of the transmit filter to be subsequently loaded into the lowest-order bits of the Access Data Register [0x7C–0x7F] within two symbol periods. Does not affect the value of the coefficient.

7	6	5	4	3	2	1	0
–	–	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x77— Transmit Filter Write Tap Select Register (tx_tap_select_write)

Six-bit read/write register representing an unsigned binary address defined over a range of 0 to 63 decimal. When written, this register causes the lowest-order 8 bits of the Access Data Register [0x7C–0x7F] to be subsequently written to the selected transmit filter coefficient within two symbol periods. Does not affect the value of the Access Data Register.

7	6	5	4	3	2	1	0
–	–	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x78— Equalizer Read Select Register (eq_add_read)

Six-bit read/write register representing an unsigned binary address defined over a range of 0 to 47 decimal. When written, this register causes the selected 16-bit location of the equalizer register file to be subsequently loaded into the lowest-order bits of the Access Data Register [0x7C–0x7F] within two symbol periods. Does not affect the value of the register file location. An address map of the shared register file, as defined by the factory-delivered microcode, is shown in Table 10.

7	6	5	4	3	2	1	0
–	–	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

Table 10. Shared Register File Address Map

D[5:0]		Stored Parameter
Decimal	Binary	
0–7	00 0000–00 0111	FFE Coefficients 0–7
8–15	00 1000–00 1111	FFE Data Taps 0–7
16–20	01 0000–01 0100	EP Coefficients 0–4
21–25	01 0101–01 1001	EP Data Taps 0–4
26	01 1010	DAGC Gain - Least-Significant Word
27	01 1011	DAGC Gain - Most-Significant Word
28	01 1100	DAGC Output
29	01 1101	FFE Output
30	01 1110	DAGC Input
31	01 1111	FFE Output, Delayed 1 Symbol Period
32	10 0000	DAGC Error Signal
33	10 0001	Equalizer Error Signal
34	10 0010	Slicer Error Signal
35–47	10 0011–10 1111	Reserved

0x79— Equalizer Write Select Register (eq_add_write)

Six-bit read/write register representing an unsigned binary address defined over a range of 0 to 47 decimal. When written, this register causes the lowest-order 16 bits of the Access Data Register [0x7C–0x7F] to be subsequently written to the selected equalizer register file location within two symbol periods. Does not affect the value of the Access Data Register. An address map of the shared register file, as defined by the factory-delivered microcode, is shown in Table 10.

7	6	5	4	3	2	1	0
–	–	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x7A— Equalizer Microcode Read Select Register (eq_microcode_add_read)

Six-bit read/write register representing an unsigned binary address defined over a range of 0 to 63 decimal. When written, this register causes the selected 32-bit location of the equalizer microprogram store to be subsequently loaded into the Access Data Register [0x7C–0x7F] within two symbol periods. Does not affect the value of the microprogram store location.

7	6	5	4	3	2	1	0
–	–	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x7B— Equalizer Microcode Write Select Register (eq_microcode_add_write)

Six-bit read/write register representing an unsigned binary address defined over a range of 0 to 63 decimal. When written, this register causes all 32 bits of the Access Data Register [0x7C–0x7F] to be subsequently written to the selected equalizer microprogram store location within two symbol periods. Does not affect the value of the Access Data Register. Factory-developed equalizer microcode is included with the no-fee licensed HDSL transceiver software available from Brooktree.

7	6	5	4	3	2	1	0
–	–	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x7C–0x7F— Access Data Register (access_data_byte3:0)

Four-byte read/write register stores filter coefficient, equalizer register file, and equalizer microprogram store contents during indirect accesses to these RAM-based locations. Writes to addresses 0x70 through 0x7B. Utilize the contents of this shared register as specified in each of the individual register descriptions.

Register Summary

***Table 11. Register Table** (1 of 6)*

Addr	Register Name	R/W	Bit Labels							
			7	6	5	4	3	2	1	0
0x00	Global Modes and Status	R/W	hw_revision[3]	hw_revision[2]	hw_revision[1]	hw_revision[0]	—	—	—	mode
0x01	Serial Monitor Source Select	R/W	—	—	smon[5]	smon[4]	smon[3]	smon[2]	smon[1]	smon[0]
0x02	Interrupt Mask Low	R/W	t4	t3	snr	meter	sut4	sut3	sut2	sut1
0x03	Interrupt Mask High	R/W	—	—	—	—	sync	high_felm	low_felm	low_snr
0x04	Timer Source	R/W	t4	t3	snr	meter	sut4	sut3	sut2	sut1
0x05	IRQ Source	R/W	—	—	—	—	sync	high_felm	low_felm	low_snr
0x06	Channel Unit Interface Modes	R/W	—	—	—	tbclk_pol	rbclk_pol	fifos_mode	interface_mode[1]	interface_mode[0]
0x07	Receive Phase Select	R/W	—	—	—	—	rphs[3]	rphs[2]	rphs[1]	rphs[0]
0x08	Linear Echo Canceler Modes	R/W	—	—	enable_dc_tap	adapt_coefficients	zero_coefficients	zero_output	adapt_gain[1]	adapt_gain[0]
0x09	Nonlinear Echo Canceler Modes	R/W	negate_symbol	symbol_delay[2]	symbol_delay[1]	symbol_delay[0]	adapt_coefficients	zero_coefficients	zero_output	adapt_gain
0x0A	Decision Feedback Equalizer Modes	R/W	—	—	—	timing_function	adapt_coefficients	zero_coefficients	zero_output	adapt_gain
0x0B	Transmitter Modes	R/W	—	isolated_pulse[1]	isolated_pulse[0]	transmitter_off	htur_lfsr	data_source[2]	data_source[1]	data_source[0]
0x0C	Timer Restart	R/W	t4	t3	snr	meter	sut4	sut3	sut2	sut1
0x0D	Timer Enable	R/W	t4	t3	snr	meter	sut4	sut3	sut2	sut1
0x0E	Timer Continuous Mode	R/W	t4	t3	snr	meter	sut4	sut3	sut2	sut1
0x10	Start Up Timer 1 Interval, Low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x11	Start Up Timer 1 Interval, High	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]

Table 11. Register Table (2 of 6)

Addr	Register Name	R/W	Bit Labels							
			7	6	5	4	3	2	1	0
0x12	Start Up Timer 2 Interval, Low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x13	Start Up Timer 2 Interval, High	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x14	Start Up Timer 3 Interval, Low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x15	Start Up Timer 3 Interval, High	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x16	Start Up Timer 4 Interval, Low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x17	Start Up Timer 4 Interval, High	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x18	Meter Timer Interval, Low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x19	Meter Timer Interval, High	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x1A	SNR Alarm Timer Interval, Low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x1B	SNR Alarm Timer Interval, High	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x1C	General Purpose Timer 3 Interval, Low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x1D	General Purpose Timer 3 Interval, High	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x1E	General Purpose Timer 4 Interval, Low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x1F	General Purpose Timer 4 Interval, High	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x20	ADC Bit Width	R/W	—	—	—	—	—	—	width[1]	width[0]
0x21	ADC Gain Control	R/W	—	—	—	—	—	adc_cont_fix_gain	again[1]	again[0]
0x22	PLL Modes	R/W	mclk_freq[1]	mclk_freq[0]	negate_symbol	phase_detector_gain[1]	phase_detector_gain[0]	freeze_pll	pll_gain[1]	pll_gain[0]
0x24	Timing Recovery PLL Phase Offset, Low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

Table 11. Register Table (3 of 6)

Addr	Register Name	R/W	Bit Labels							
			7	6	5	4	3	2	1	0
0x25	Timing Recovery PLL Phase Offset, High	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x26	Receiver DC Offset, Low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x27	Receiver DC Offset, High	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x28	External AGC Target, Low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x29	External AGC Target, High	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x2A	Noise-Level Histogram Threshold, Low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x2B	Noise-Level Histogram Threshold, High	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x2C	Error Predictor Pause Threshold, Low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x2D	Error Predictor Pause Threshold, High	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x2E	Scrambler Synchronization Threshold	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x30	Far-End High Alarm Threshold, Low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x31	Far-End High Alarm Threshold, High	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x32	Far-End Low Alarm Threshold, Low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x33	Far-End Low Alarm Threshold, High	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x34	SNR Alarm Threshold, Low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x35	SNR Alarm Threshold, High	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x36	Cursor Level, Low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

Table 11. Register Table (4 of 6)

Addr	Register Name	R/W	Bit Labels							
			7	6	5	4	3	2	1	0
0x37	Cursor Level, High	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x38	DAGC Target, Low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x39	DAGC Target, High	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x3A	Symbol Detector Modes	R/W	enable_peak_ detector	output_mux_ control[1]	output_mux_ control[0]	scr_out_to_dfe	two_level	lfsr_lock	htur_lfsr	descr_on
0x3B	Peak Detector Delay	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x3C	Digital AGC Modes	R/W	—	—	—	—	—	eq_error_ adaptation	adapt_coefficient	adapt_gain
0x3D	Feed Forward Equalizer Modes	R/W	—	—	—	—	adapt_last_coeff	zero_coefficients	adapt_coefficient	adapt_gain
0x3E	Error Predictor Modes	R/W	—	—	—	—	zero_output	zero_coefficients	adapt_coefficients	adapt_gain
0x40	Phase Detector Meter, Low	R	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]
0x41	Phase Detector Meter, High	R	D[25]	D[24]	D[23]	D[22]	D[21]	D[20]	D[19]	D[18]
0x42	Overflow Meter	R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x44	DC Level Meter, Low	R	D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]
0x45	DC Level Meter, High	R	D[31]	D[30]	D[29]	D[28]	D[27]	D[26]	D[25]	D[24]
0x46	Signal Level Meter, Low	R	D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]
0x47	Signal Level Meter, High	R	D[31]	D[30]	D[29]	D[28]	D[27]	D[26]	D[25]	D[24]
0x48	Far-End Level Meter, Low	R	D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]
0x49	Far-End Level Meter, High	R	D[31]	D[30]	D[29]	D[28]	D[27]	D[26]	D[25]	D[24]
0x4A	Noise Level Histogram Meter, Low	R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x4B	Noise Level Histogram Meter, High	R	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]

Table 11. Register Table (5 of 6)

Addr	Register Name	R/W	Bit Labels							
			7	6	5	4	3	2	1	0
0x4C	Bit Error Rate Meter, Low	R	D[7]	D[6]	D[5	D[4]	D[3]	D[2]	D[1]	D[0]
0x4D	Bit Error Rate Meter, High	R	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x4E	Symbol Histogram Meter	R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x50	Noise Level Meter, Low	R	D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]
0x51	Noise Level Meter, High	R	D[31]	D[30]	D[29]	D[28]	D[27]	D[26]	D[25]	D[24]
0x52	Timing Function Result, Low	R	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x53	Timing Function Result, High	R	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x5E	VCXO Frequency, Low	R/W	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]	D[15]
0x5F	VCXO Frequency, High	R/W	D[30]	D[29]	D[28]	D[27]	D[26]	D[25]	D[24]	D[23]
0x70	LEC Read Tap Select	R/W	—	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x71	LEC Write Tap Select	R/W	—	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x72	NEC Read Tap Select	R/W	—	—	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x73	NEC Write Tap Select	R/W	—	—	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x74	DFE Read Tap Select	R/W	—	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x75	DFE Write Tap Select	R/W	—	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x76	Transmitter Filter Read Tap Select	R/W	—	—	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x77	Transmitter Filter Write Tap Select	R/W	—	—	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x78	Equalizer Read Select	R/W	—	—	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x79	Equalizer Write Select	R/W	—	—	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

Table 11. Register Table (6 of 6)

Addr	Register Name	R/W	Bit Labels							
			7	6	5	4	3	2	1	0
0x7A	Equalizer Microcode Read Select	R/W	—	—	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x7B	Equalizer Microcode Write Select	R/W	—	—	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x7C	Access Data	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x7D	Access Data	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x7E	Access Data	R/W	D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]
0x7F	Access Data	R/W	D[31]	D[30]	D[29]	D[28]	D[27]	D[26]	D[25]	D[24]

NOTE: Addresses: 0x120, 0x139–0x13F, 0x140, 0x159–0x15F, 0x1A0, 0x1B9–0x1BF are used for signaling stack space. This space is accessible to the host MPU. However, accessing this space is not advised.

Electrical Specifications

Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 12. Absolute Maximum Ratings

Symbol	Parameter	Bt8958 (all grades)		Units
		Minimum	Maximum	
V_{Supply}	Supply Voltage(1)	−0.5	+7	V
V_I	Input Voltage on any Signal Pin(2)	−0.5	VDD2 + 0.5	V
T_{ST}	Storage Temperature	−65	+125	°C
T_{VSOL}	Vapor-Phase Soldering Temperature (1 minute)		+220	°C

Notes: (1). VDD1, VDD2, and VAA relative to VSS1, VSS2, and GND, respectively.
(2). Relative to VSS2.

Recommended Operating Conditions

Table 13. Recommended Operating Conditions

Symbol	Parameter	Bt8958 (all grades)			Units
		Minimum	Typical	Maximum	
V_{DD1}	Digital Core-Logic Supply Voltage	4.75	5.0	5.25	V
V_{DD2}	Digital I/O-Buffer Supply Voltage	4.75	5.0	5.25	V
V_{AA}	Analog Supply Voltage	4.75	5.0	5.25	V
VSS/GND	Digital/Analog Ground Offset Voltage(1)		0		V
V_{IH}	High-Level Input Voltage	2.0		VDD2 + 0.3	V
V_{IL}	Low-Level Input Voltage	–0.3		+0.8	V
V_{REF}	Analog Reference Voltage at pin XVREF		1.2		V
I_{FS}	Full-Scale DAC Output Current(2)		–1.0		mA
C_{COMP}	DAC Compensation Capacitance between pins VAA and XCOMP		0.1		µF
C_L	Output Capacitive Loading(3)			60	pF
T_A	Ambient Operating Temperature(4)	–40		+85	˚C

Notes: (1). VSS1, VSS2, and GND DC potentials must be maintained within the specified limits of one another.
(2). $I_{FS} = -(V_{REf} \div R_{FS})$, where R_{FS} is an external precision resistor placed between pin XFS and analog ground.
(3). Capacitive loading over which all digital output switching characteristics are guaranteed.
(4). Still-air temperature range over which all electrical characteristics and timing requirements/characteristics are guaranteed.

Electrical Characteristics

Table 14. Electrical Characteristics

Symbol	Parameter	Bt8958 (all grades)			Units
		Minimum	Typical	Maximum	
V_{OH}	High-Level Output Voltage @ I_{OH} = –400 µA (RCVCLK)	0.9 x V_{DD2}			V
V_{OH}	High-Level Output Voltage @ I_{OH} = –400 µA (All Other Outputs)	2.4			V
V_{OL}	Low-Level Output Voltage @ I_{OL} = 6 mA (IRQ*)			0.4	V
V_{OL}	Low-Level Output Voltage @ I_{OL} = 3 mA (All Other Outputs)			0.4	V
I_I	Input Leakage Current @ $V_{SS2} \le V_I \le V_{DD2}$			±10	µA
I_{OZ}	High-Impedence Output Leakage Current @ $V_{SS2} \le V_O \le V_{DD2}$			±10	µA
I_{PR}	Resistive Pullup Current @ $V_I = V_{SS2}$ (TMS)	–50		–800	µA
$I_{DD/AA}$	Total Supply Current @ F_{QCLK} = 1160 kHz(1)		285	340	mA
$I_{DD/AA}$	Total Supply Current @ F_{QCLK} = 776 kHz(1)		215	260	mA
I_{PD}	Total Power-Down Current @ F_{QCLK} = 1160 kHz(2)		160		mA
I_{PD}	Total Power-Down Current @ F_{QCLK} = 776 kHz(2)		120		mA
C_I	Input Capacitance		10		pF
C_{OZ}	High-Impedance Output Capacitance		10		pF

Note: Typical characteristics measured at nominal operating conditions: T_A = 25 °C; $V_{DD/AA}$ = 5.0 V. Minimum/maximum characteristics guaranteed over extreme operating conditions: min ≤ T_A ≤ max; min ≤ $V_{DD/AA}$ ≤ max.

Notes: (1). $I_{DD1} + I_{DD2} + I_{AA}$ during normal operation. Applicable only to devices of the appropriate speed grade.
(2). $I_{DD1} + I_{DD2} + I_{AA}$ during power-down operation. Applicable only to devices of the appropriate speed grade.

Clock Timing

Table 15. Master Clock Timing Requirements, Internal Clock Multiplier Enabled (X16/64 = 1)*

Symbol	Parameter	Bt8958EHJ50		Bt8958EHJ80		Units
		Minimum	Maximum	Minimum	Maximum	
1(T_{MCLK})	MCLK Period	80	160	53	160	ns
2	MCLK Pulse-Width Low	30		20		ns
3	MCLK Pulse-Width High	30		20		ns

Table 16. Master Clock Timing Requirements, Internal Clock Multiplier Bypassed (X16/64 = 0)*

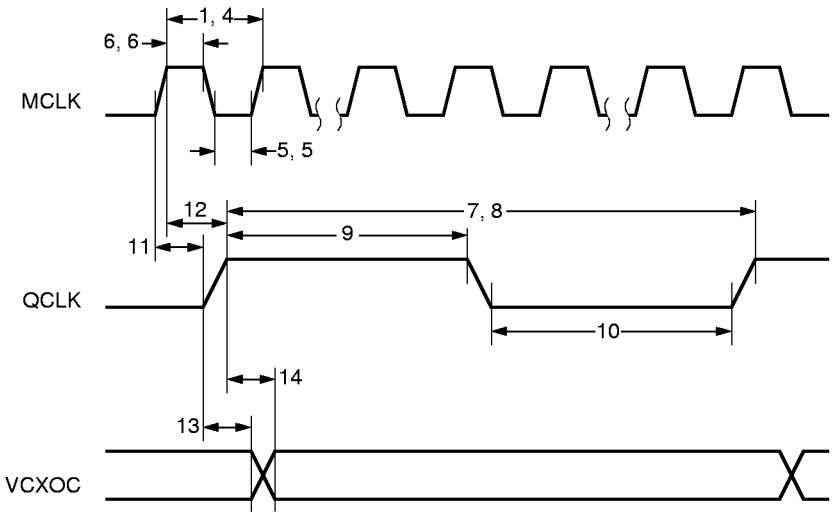
Symbol	Parameter	Bt8958EHJ50		Bt8958EHJ80		Units
		Minimum	Maximum	Minimum	Maximum	
4(T_{MCLK})	MCLK Period	39	500	39	500	ns
5	MCLK Pulse-Width Low	15		15		ns
6	MCLK Pulse-Width High	15		15		ns

Table 17. Symbol Clock and VCXO Control Switching Characteristics

Symbol	Parameter	Bt8958 (all grades)		Units
		Minimum	Maximum	
7(T_{QCLK})	QCLK Period w/ MCLK Multiplier Enabled (X16/64* = 1)	16 x T_{MCLK}	16 x T_{MCLK}	ns
8(T_{QCLK})	QCLK Period w/ MCLK Multiplier Bypassed (X16/64* = 0)	64 x T_{MCLK}	64 x T_{MCLK}	ns
9	QCLK Pulse-Width High	$T_{QCLK} \div 2 - 20$	$T_{QCLK} \div 2 + 20$	ns
10	QCLK Pulse-Width Low	$T_{QCLK} \div 2 - 20$	$T_{QCLK} \div 2 + 20$	ns
11	QCLK Hold after MCLK Rising Edge(1)	0		ns
12	QCLK Delay after MCLK High(1)		50	ns
13	VCXOC Hold after QCLK Rising Edge	–50		ns
14	VCXOC Delay after QCLK High		50	ns

Notes: (1). Applicable to both MCLK multiplier enabled and bypassed modes. Only the number of MCLK cycles (T_{MCLK}) between output transitions is affected by multiplier mode.

Figure 15. Clock and VCXO Control Timing



Analog Front End Interface Timing

Table 18. Analog Front End Timing Requirements

Symbol	Parameter	Bt8958 (all grades)		Units
		Minimum	Maximum	
15	RCV[15:0] Setup Prior to RCVCLK Rising Edge	50		ns
16	RCV[15:0] Hold after RCVCLK High	10		ns

Table 19. Analog Front End Switching Characteristics

Symbol	Parameter	Bt8958 (all grades)		Units
		Minimum	Maximum	
17	RCVCLK Period	T_{QCLK}	T_{QCLK}	
18	RCVCLK Pulse-Width High	$T_{QCLK} \div 16 - 20$	$T_{QCLK} \div 16 + 20$	ns
19	RCVCLK Pulse-Width Low	$T_{QCLK} \times 15 \div 16 - 20$	$T_{QCLK} \times 15 \div 16 + 20$	ns
20	RCVCLK Hold after MCLK Rising Edge(1)	0		ns
21	RCVCLK Delay after MCLK High(1)		50	ns
22	AGAIN[1] Hold after QCLK Rising Edge(2)	–50		ns
23	AGAIN[1] Delay after QCLK High(2)		50	ns
24	AGAIN[1], AGAIN[0] Hold after Write Strobe Rising Edge(3)	0		ns
25	AGAIN[1], AGAIN[0] Delay after Write Strobe High(3)		$T_{QCLK} \div 32$	

Notes: (1). Applicable to both MCLK multiplier enabled and bypassed modes. Only the number of MCLK cycles (T_{MCLK}) between output transitions is affected by multiplier mode.
(2). Only applies to continuous external AGC mode where AGAIN[1] is updated on the rising edge of QCLK.
(3). In fixed external AGC mode, AGAIN[1] and AGAIN[0] are updated after a write to the again[1,0] field of the ADC Gain Control Register using an internal clock running at 64 times the symbol rate. Write Strobe is defined as WR* or CS* in Intel mode, and DS* or CS* when R/W* is low in Motorola mode.

Figure 16. Receive Clock and Data Timing

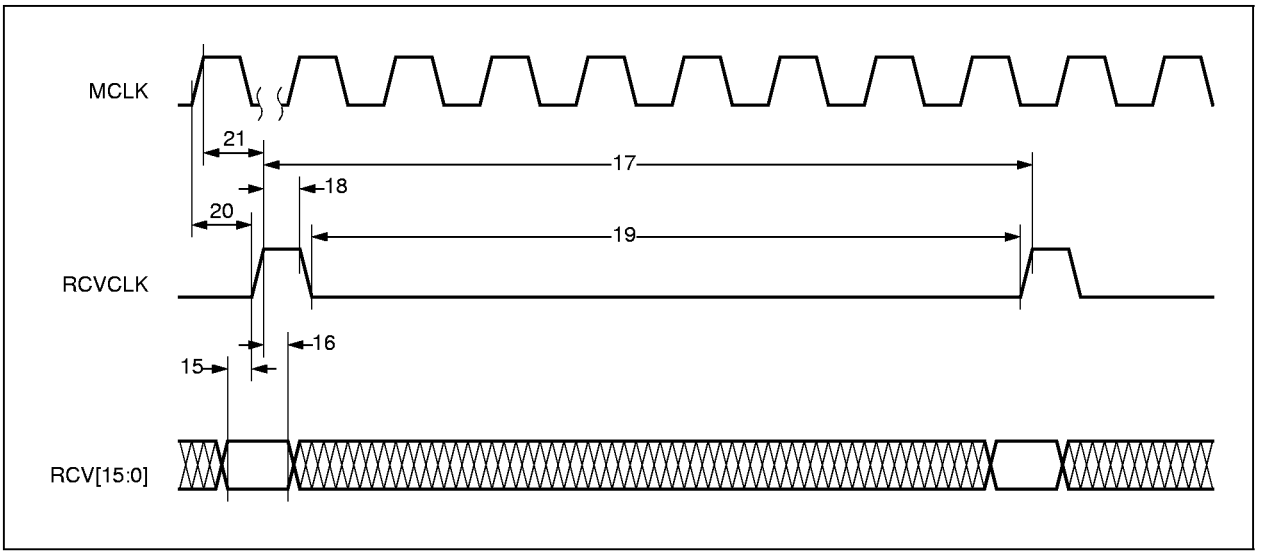


Figure 17. AGAIN[1] Timing in Continuous External AGC Mode

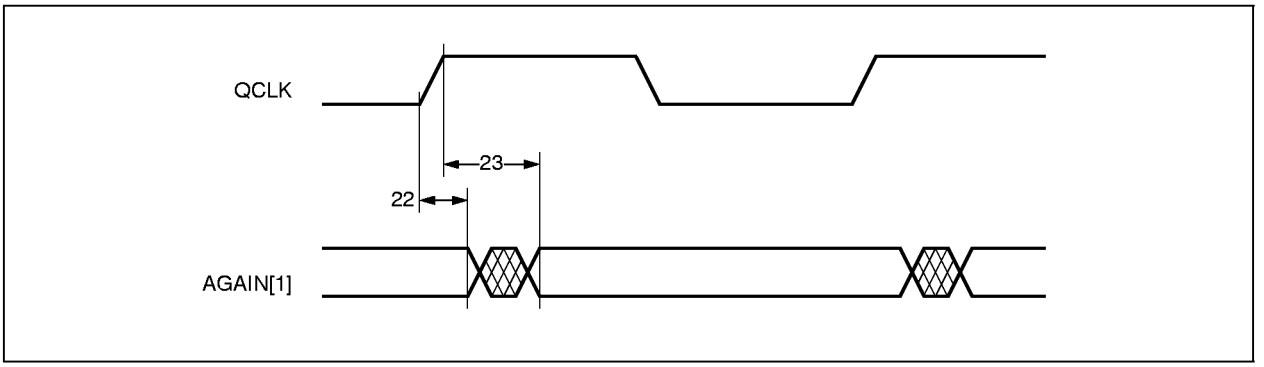
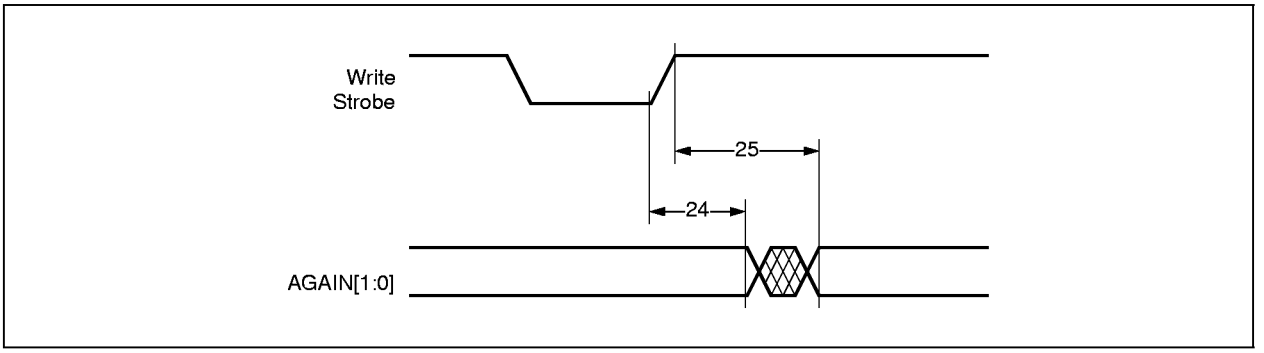


Figure 18. AGAIN[1,0] Timing in Fixed External AGC Mode



Channel Unit Interface Timing

Table 20. Channel Unit Interface Timing Requirements, Parallel Master Mode

Symbol	Parameter	Bt8958 (all grades)		Units
		Minimum	Maximum	
26	TQ[1,0] Setup Prior to QCLK Falling Edge	100		ns
27	TQ[1,0] Hold After QCLK Low	25		ns

Table 21. Channel Unit Interface Switching Characteristics, Parallel Master Mode

Symbol	Parameter	Bt8958 (all grades)		Units
		Minimum	Maximum	
28	RQ[1,0] Hold after QCLK Rising Edge	–50		ns
29	RQ[1,0] Delay after QCLK High		50	ns

Figure 19. Channel Unit Interface Timing, Parallel Master Mode

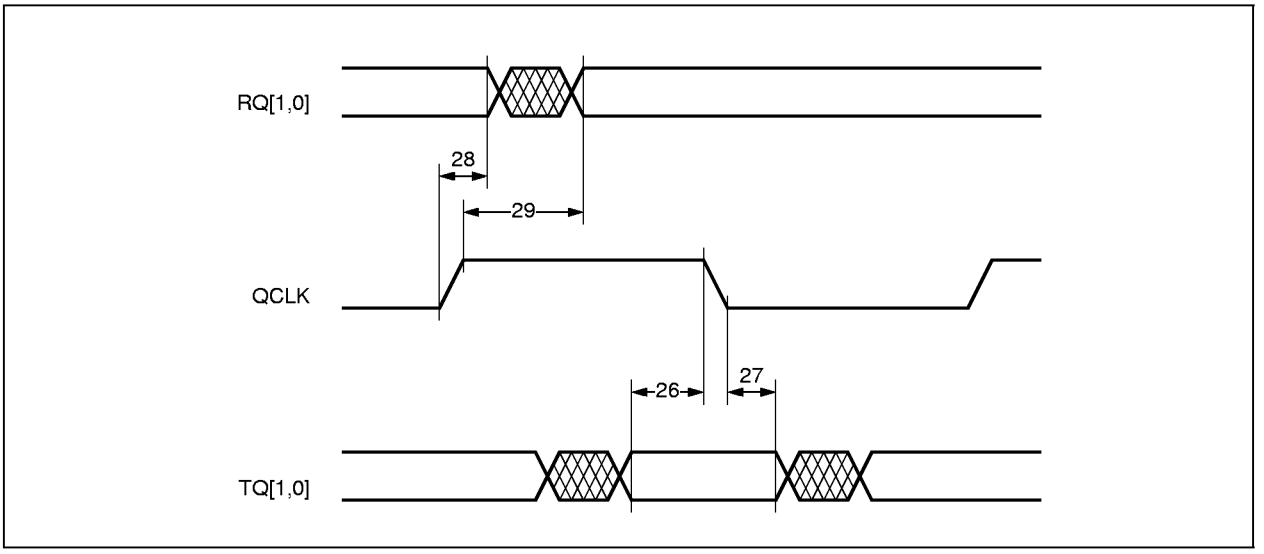


Table 22. Channel Unit Interface Timing Requirements, Parallel Slave Mode

Symbol	Parameter	Bt8958 (all grades)		Units
		Minimum	Maximum	
30	TBCLK, RBCLK Period(1)	T_{QCLK}	T_{QCLK}	
31	TBCLK, RBCLK Pulse-Width High	$T_{QCLK} \div 4$		
32	TBCLK, RBCLK Pulse-Width Low	$T_{QCLK} \div 4$		
33	TQ[1,0] Setup Prior to TBCLK Active Edge(2)	25		ns
34	TQ[1,0] Hold after TBCLK High/Low(2)	25		ns

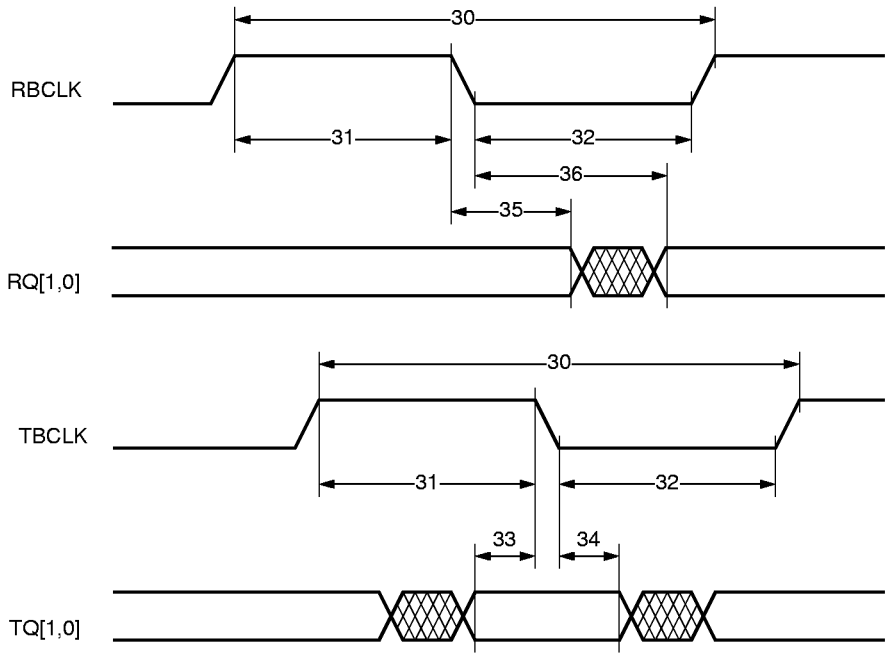
Notes: (1). TBCLK and RBCLK must be frequency locked to QCLK though they may have independent phase relationships to QCLK and to one another.
(2). TBCLK polarity (edge sensitivity) is programmable through the Channel Unit Interface Unit Register [0x06].

Table 23. Channel Unit Interface Switching Characteristics, Parallel Slave Mode

Symbol	Parameter	Bt8958 (all grades)		Units
		Minimum	Maximum	
35	RQ[1,0] Hold after RBCLK Active Edge(1)	0		ns
36	RQ[1,0] Delay after RBCLK High/Low(1)		100	ns

Notes: (1). RBCLK polarity (edge sensitivity) is programmable through the Channel Unit Interface Modes Register [0x06]

Figure 20. Channel Unit Interface Timing, Parallel Slave Mode



Note: TBCLK and RBCLK polarities are programmable through the CU Interface Modes Register [0x06]. The figure depicts both clocks programmed to falling-edge active.

Table 24. Channel Unit Interface Timing Requirements, Serial Mode

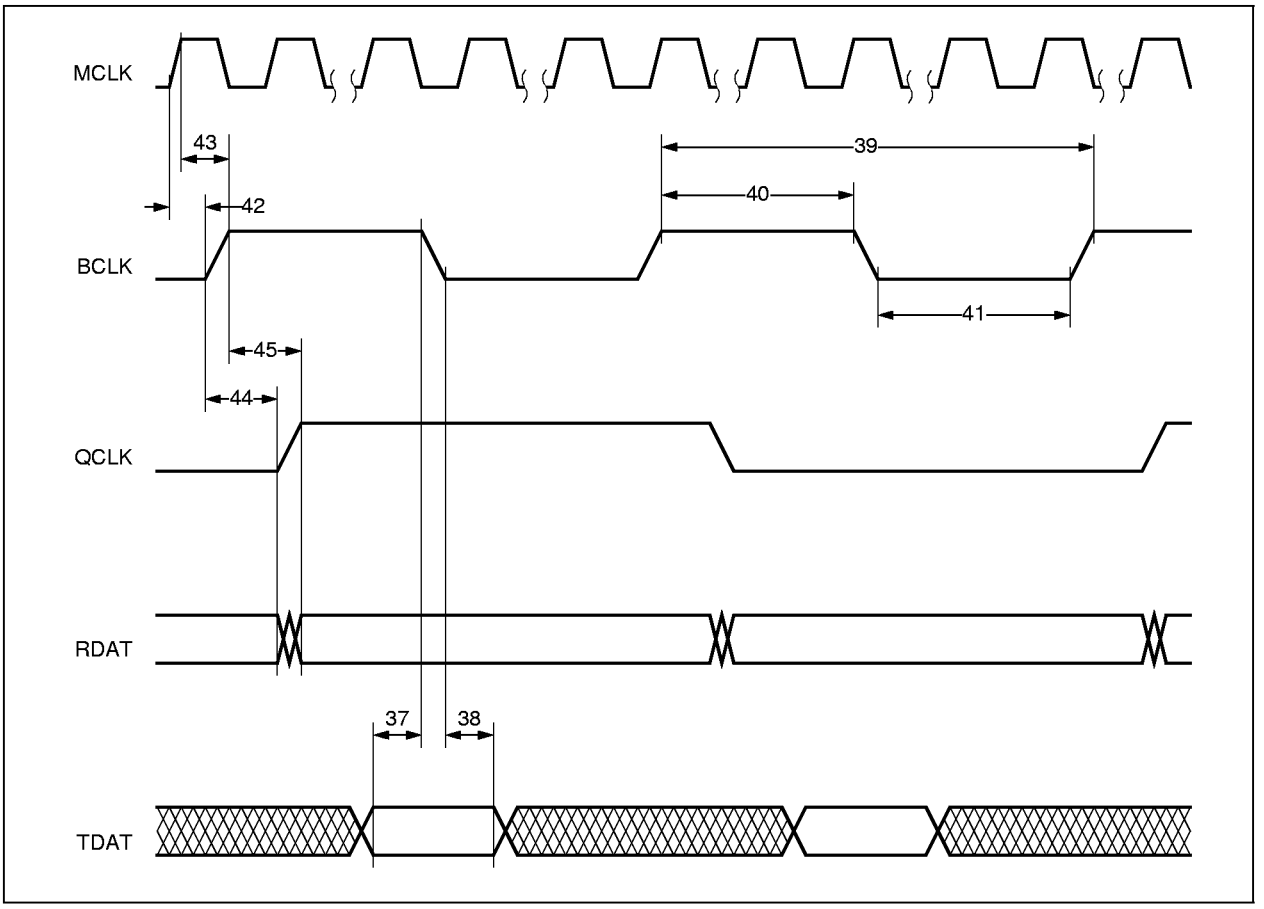
Symbol	Parameter	Bt8958 (all grades)		Units
		Minimum	Maximum	
37	TDAT Setup Prior to BCLK Falling Edge	100		ns
38	TDAT Hold After BCLK Low	25		ns

Table 25. Channel Unit Interface Switching Characteristics, Serial Mode

Symbol	Parameter	Bt8958 (all grades)		Units
		Minimum	Maximum	
39	BCLK Period	$T_{QCLK} \div 2$	$T_{QCLK} \div 2$	
40	BCLK Pulse-Width High	$T_{QCLK} \div 4 - 20$	$T_{QCLK} \div 4 + 20$	ns
41	BCLK Pulse-Width Low	$T_{QCLK} \div 4 - 20$	$T_{QCLK} \div 4 + 20$	ns
42	BCLK Hold after MCLK Rising Edge(1)	0		ns
43	BCLK Delay after MCLK High(1)		50	ns
44	RDAT, QCLK Hold after BCLK Rising Edge	–50		ns
45	RDAT, QCLK Delay after BCLK High		50	ns

Notes: (1). Applicable to both MCLK multiplier enabled and bypassed modes. Only the number of MCLK cycles (T_{MCLK}) between output transitions is affected by multiplier mode.

Figure 21. Channel Unit Interface Timing, Serial Mode



Microcomputer Interface Timing

Table 26. Microcomputer Interface Timing Requirements

Symbol	Parameter	Bt8958 (all grades)		Units
		Minimum	Maximum	
46	ALE Pulse-Width High	30		ns
47	Address Setup Prior to ALE Falling Edge	15		ns
48	Address Hold after ALE Low	5		ns
49	ALE low prior to Write Strobe Falling Edge(1)	20		ns
50	Write Strobe Pulse-Width Low(1)	40		ns
51	Read Strobe Pulse-Width Low(2)	50		ns
52	Data In Setup prior to Write Strobe Rising Edge(1)	30		ns
53	Data In Hold after Write Strobe High(1)	5		ns
54	R/W* Setup prior to Read/Write Strobe Falling Edge	10		ns
55	R/W* Hold after Read/Write Strobe High	10		ns
56	RST* Pulse-Width Low	50		ns

Notes: (1). In Intel mode, Write Strobe is defined as WR* or CS*. In Motorola mode, it is defined as DS* or CS* when R/W* is low.
(2). In Intel mode, Read Strobe is defined as RD* or CS*. In Motorola mode, it is defined as DS* or CS* when R/W* is high.

Table 27. Microcomputer Interface Switching Characteristics

Symbol	Parameter	Bt8958 (all grades)		Units
		Minimum	Maximum	
57	Data Out Enable (Low Z) after Read Strobe Falling Edge(1)	2		ns
58	Data Out Valid after Read Strobe Low(1)		50	ns
59	Data Out Hold after Read Strobe Rising Edge(1)	2		ns
60	Data Out Disable (High Z) after Read Strobe High(1)		25	ns
61	IRQ* Hold after Write Strobe Rising Edge(2,3)	0		ns
62	IRQ* Delay after Write Strobe High(2,3)		$T_{QCLK} \div 32 + 20$	ns
63	Internal Register Delay after Write Strobe High(3,4)		$T_{QCLK} \div 32$	
64	Internal RAM Delay after Write Strobe High(3,5)		$2 \times T_{QCLK}$	
65	Access Data Register Delay after Write Strobe High(3,6)		$2 \times T_{QCLK}$	

Notes:
(1). Read Strobe is defined as RD* or CS* in Intel mode, and DS* or CS* when R/W* is high in Motorola mode.
(2). When writing an interrupt mask or status register.
(3). Write Strobe is defined as WR* or CS* in Intel mode, and DS* or CS* when R/W* is low in Motorola mode.
(4). Writes to internal registers are synchronized to an internal 64-times symbol-rate clock. Data is available for reading after the specified time. This parameter may extend the overall read access time from internal register locations under high bus speed/low symbol rate conditions.
(5). When performing an indirect write to RAM-based locations using a write select register [odd addr. 0x71–0x7B] and the Access Data Register [addr. 0x7C–0x7F]. Subsequent writes to any read/write select register or the Access Data Register, as initiated by a Write Strobe falling edge, is prohibited for the specified time. This parameter will extend the overall write access time to RAM-based locations under normal bus speed/symbol rate conditions.
(6). When performing an indirect read from RAM-based locations using a read select register [even addr. 0x70–0x7A] and the Access Data Register [addr. 0x7C–0x7F]. Subsequent writes to any read/write select register, as initiated by a Write Strobe falling edge, is prohibited for the specified time. Data is available for reading from the Access Data Register after the specified time. This parameter will extend the overall read access time from RAM-based locations under normal bus speed/symbol rate conditions. Direct writes to the Access Data Register are as specified for internal registers.

Figure 22. MCI Write Timing, Intel Mode (MOTEL = 0)

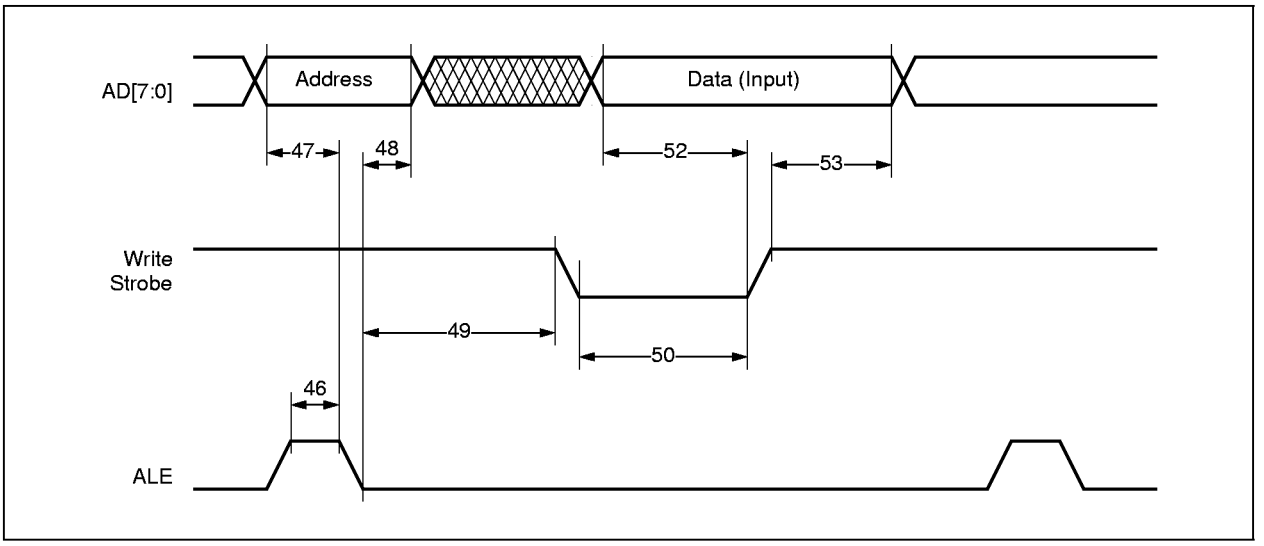


Figure 23. MCI Write Timing, Motorola Mode (MOTEL = 1)

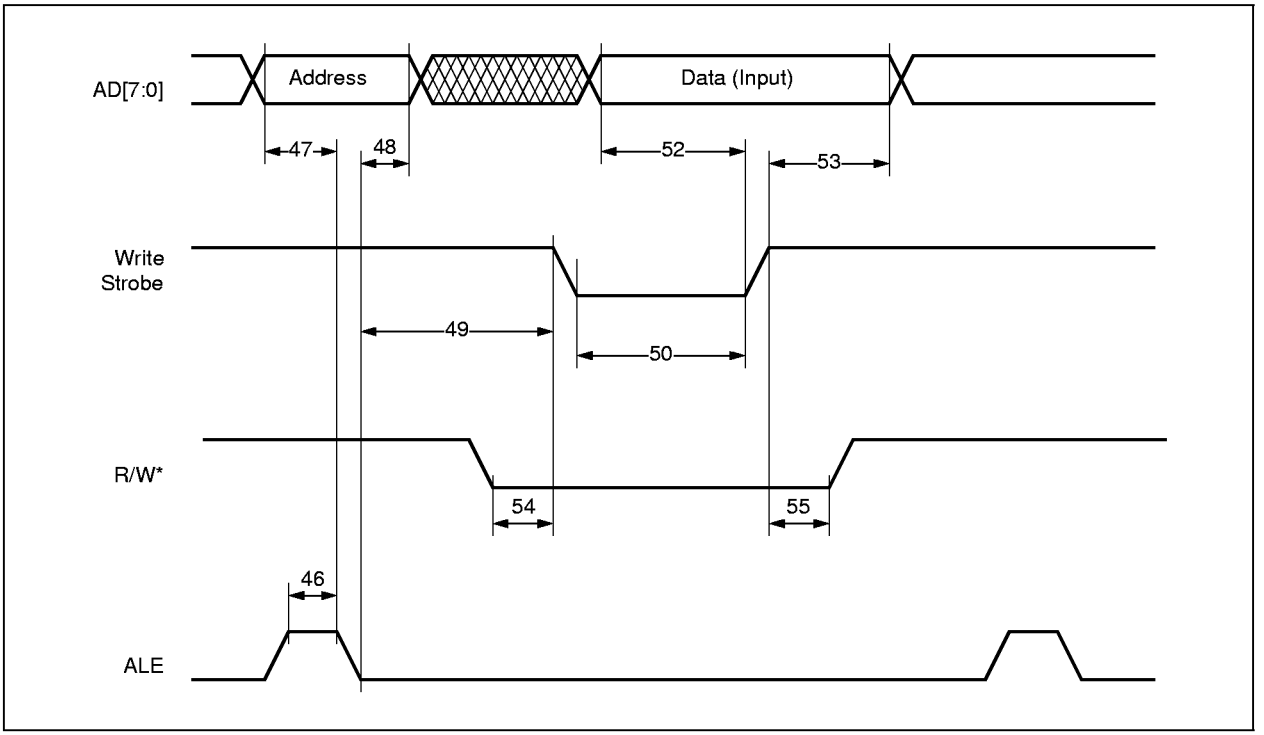


Figure 24. MCI Read Timing, Intel Mode (MOTEL = 0)

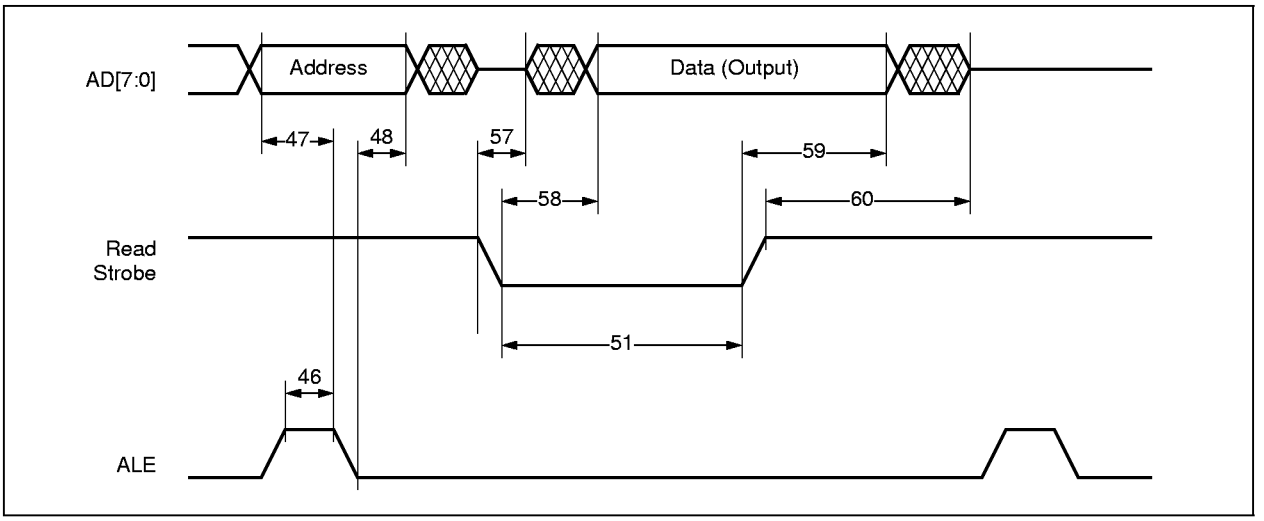


Figure 25. MCI Read Timing, Motorola Mode (MOTEL = 1)

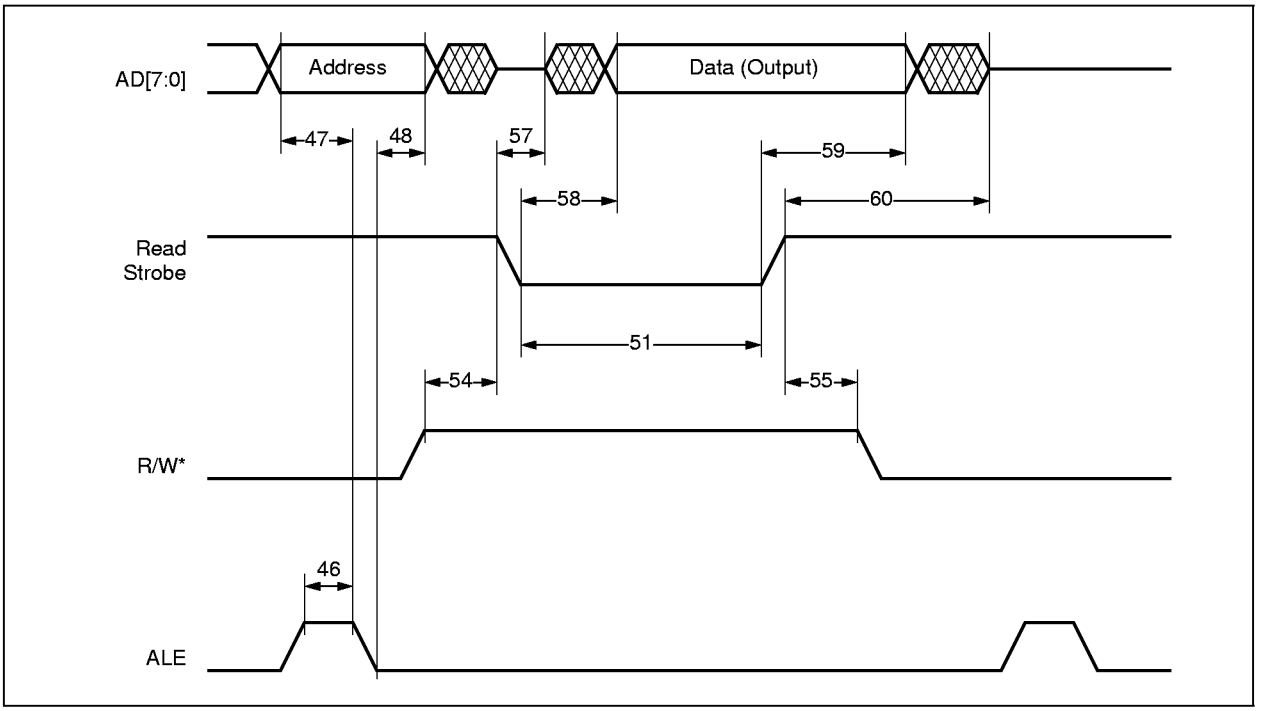
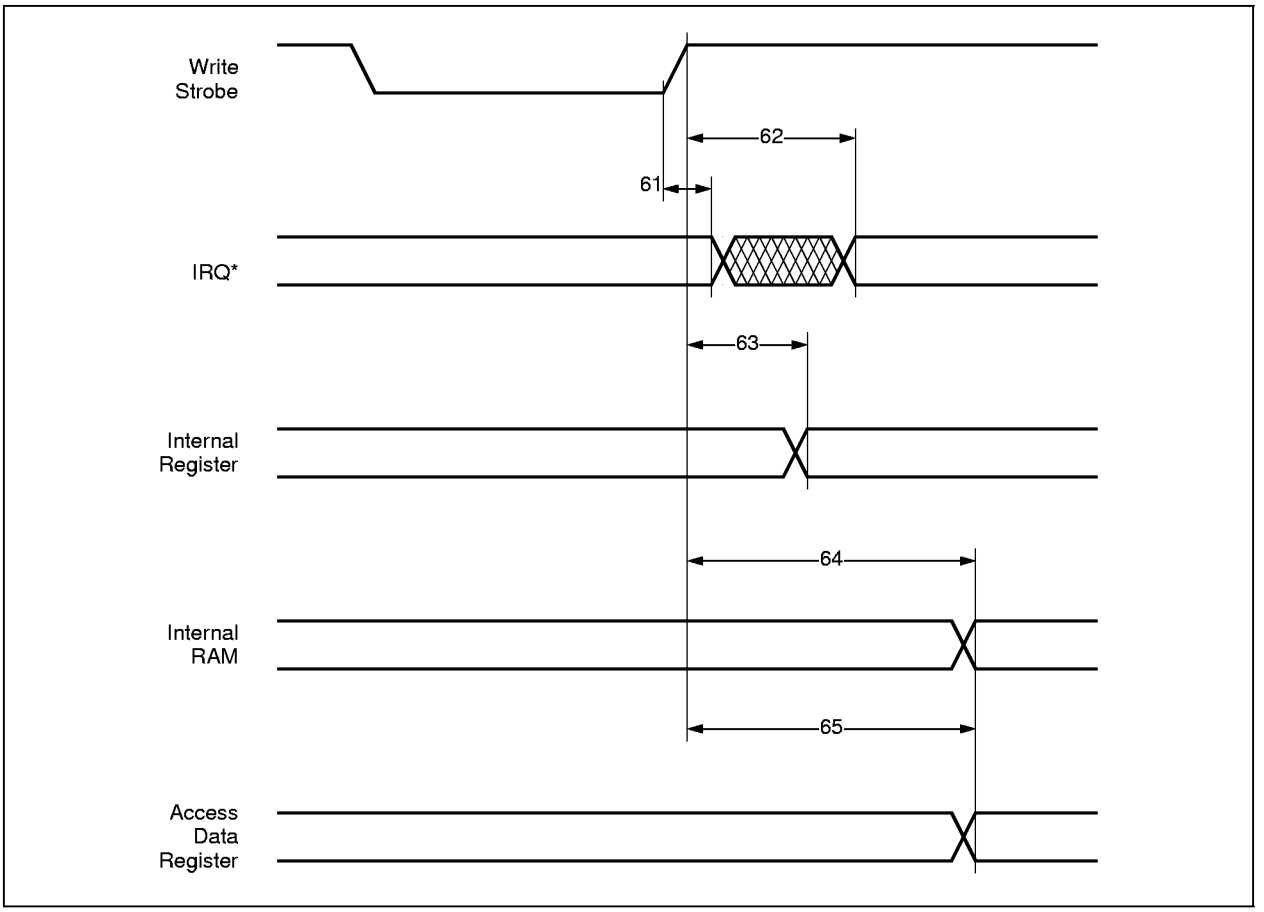


Figure 26. Internal Write Timing



Test and Diagnostic Interface Timing

Table 28. Test and Diagnostic Interface Timing Requirements

Symbol	Parameter	Bt8958 (all grades)		Units
		Minimum	Maximum	
66	TCK Pulse-Width High	80		ns
67	TCK Pulse-Width Low	80		ns
68	TMS, TDI Setup Prior to TCK Rising Edge(1)	20		ns
69	TMS, TDI Hold after TCK High(1)	20		ns
Notes: (1). Also applies to functional inputs for SAMPLE/PRELOAD and EXTEST instructions.				

Table 29. Test and Diagnostic Interface Switching Characteristics

Symbol	Parameter	Bt8958 (all grades)		Units
		Minimum	Maximum	
70	TDO Hold after TCK Falling Edge(1)	0		ns
71	TDO Delay after TCK Low(1)		50	ns
72	TDO Enable (Low Z) after TCK Falling Edge(1)	0		ns
73	TDO Disable (High Z) after TCK Low(1)		60	ns
74	SMON Hold after MCLK Rising Edge(2)	0		ns
75	SMON Delay after MCLK High(2)		50	ns
Notes: (1). Also applies to functional outputs for the EXTEST instruction. (2). Applicable to both MCLK multiplier enabled and bypassed modes. Only the number of MCLK cycles (T_{MCLK}) between output transitions is affected by multiplier mode.				

Figure 27. JTAG Interface Timing

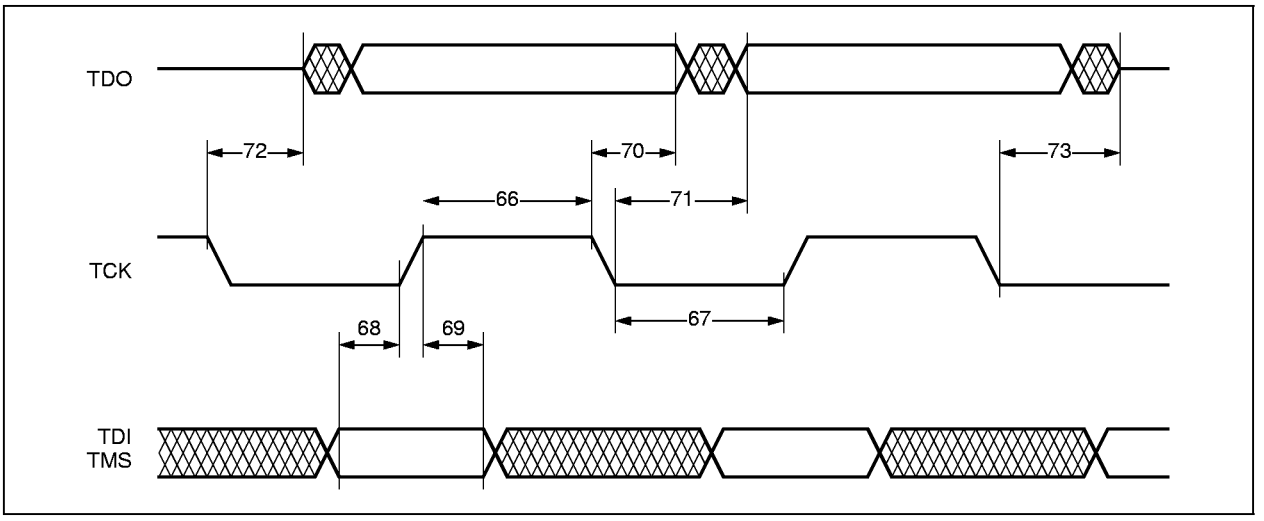


Figure 28. SMON Timing

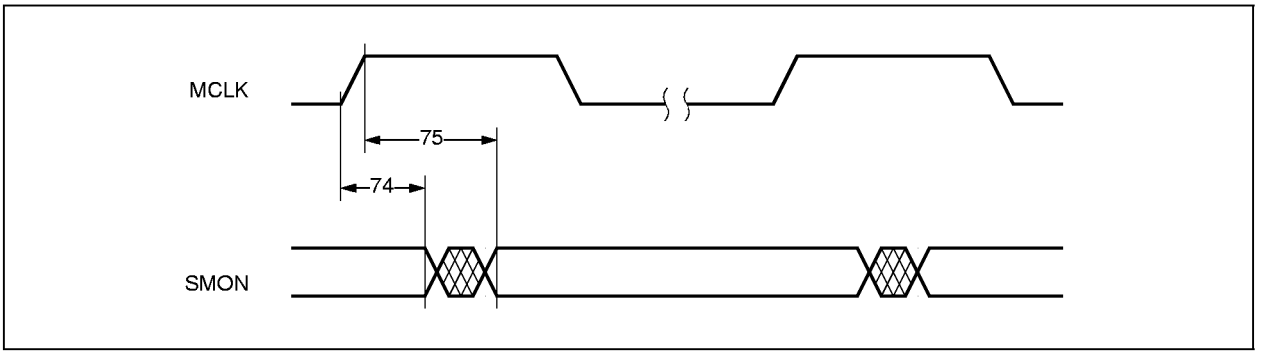


Table 30. Transmitter DAC Electrical Characteristics

Symbol	Parameter	Bt8958 (all grades)		Units
		Minimum	Maximum	
	Linearity	70		dB
	Gain Error(1)		±2	%

Notes: (1). Assuming an ideal I_{FS} of 1.0 mA. Total XMIT/XMITB output gain error is the product of I_{FS} error and transmit DAC gain error.

Figure 29. Standard Output Load (Totem Pole and Three-State Outputs)

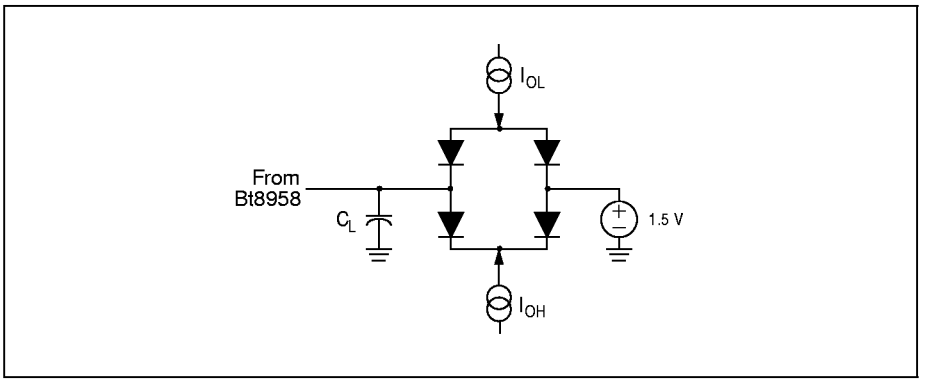


Figure 30. Open Drain Output Load (IRQ)*

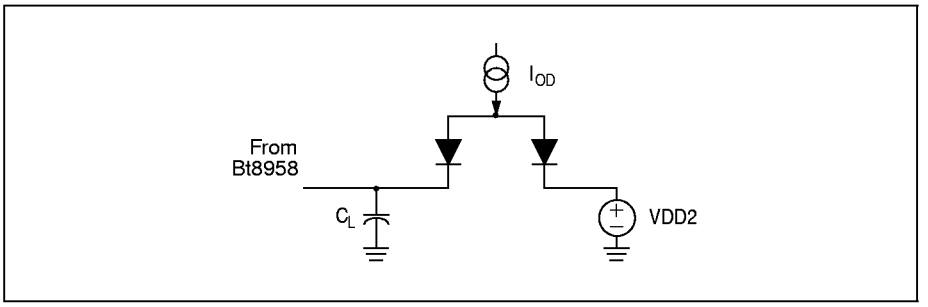
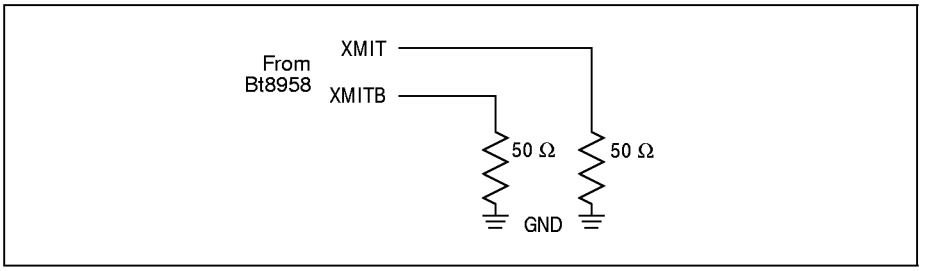
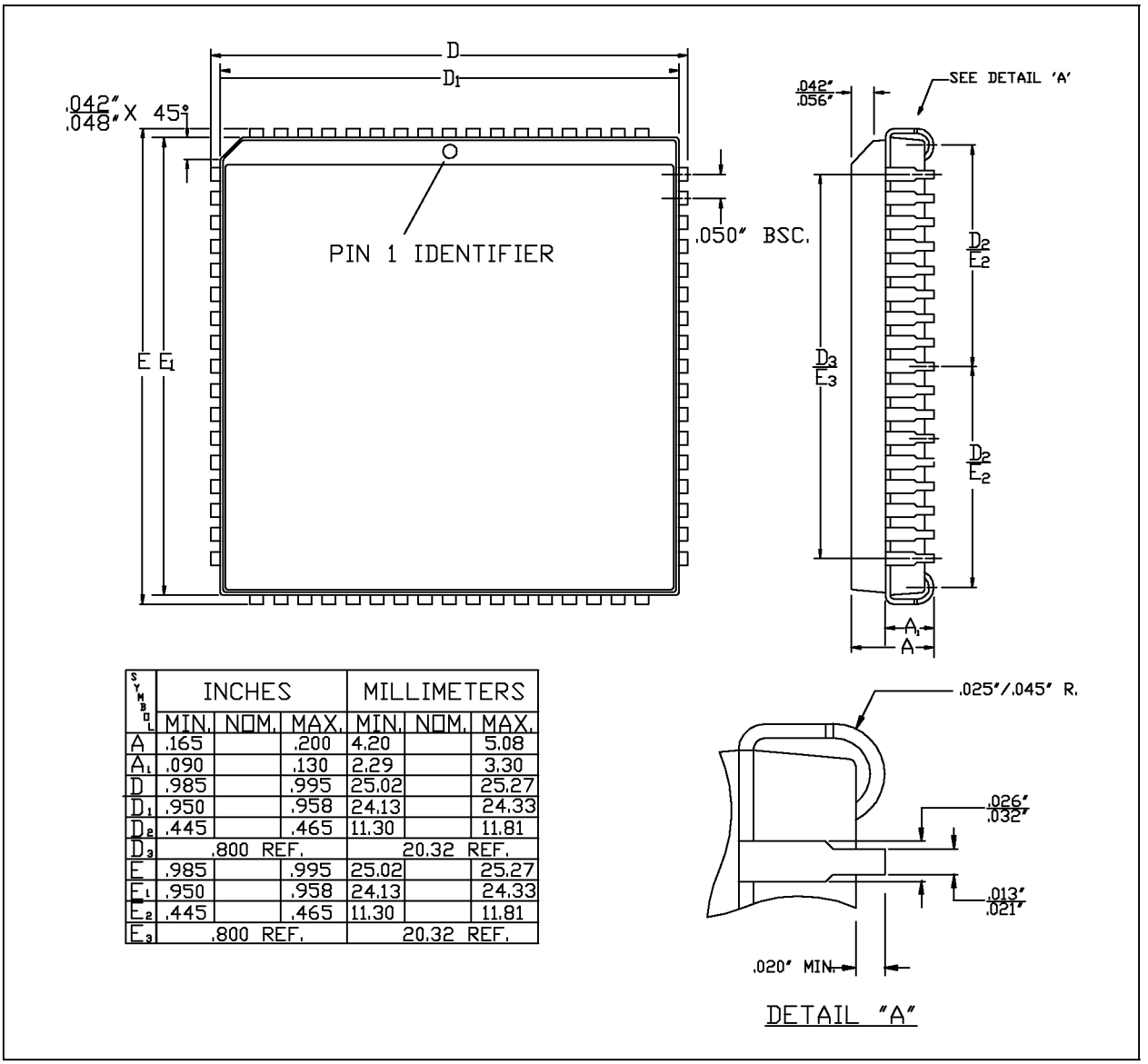


Figure 31. Transmit DAC Output Load (XMIT, XMITB)



Mechanical Specifications

Figure 32. 68-Pin Plastic Leaded Chip Carrier (PLCC)



SYMBOL	INCHES			MILLIMETERS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	.165		.200	4.20		5.08
A_1	.090		.130	2.29		3.30
D	.985		.995	25.02		25.27
D_1	.950		.958	24.13		24.33
D_2	.445		.465	11.30		11.81
D_3	.800 REF.			20.32 REF.		
E	.985		.995	25.02		25.27
E_1	.950		.958	24.13		24.33
E_2	.445		.465	11.30		11.81
E_3	.800 REF.			20.32 REF.		

Appendix A

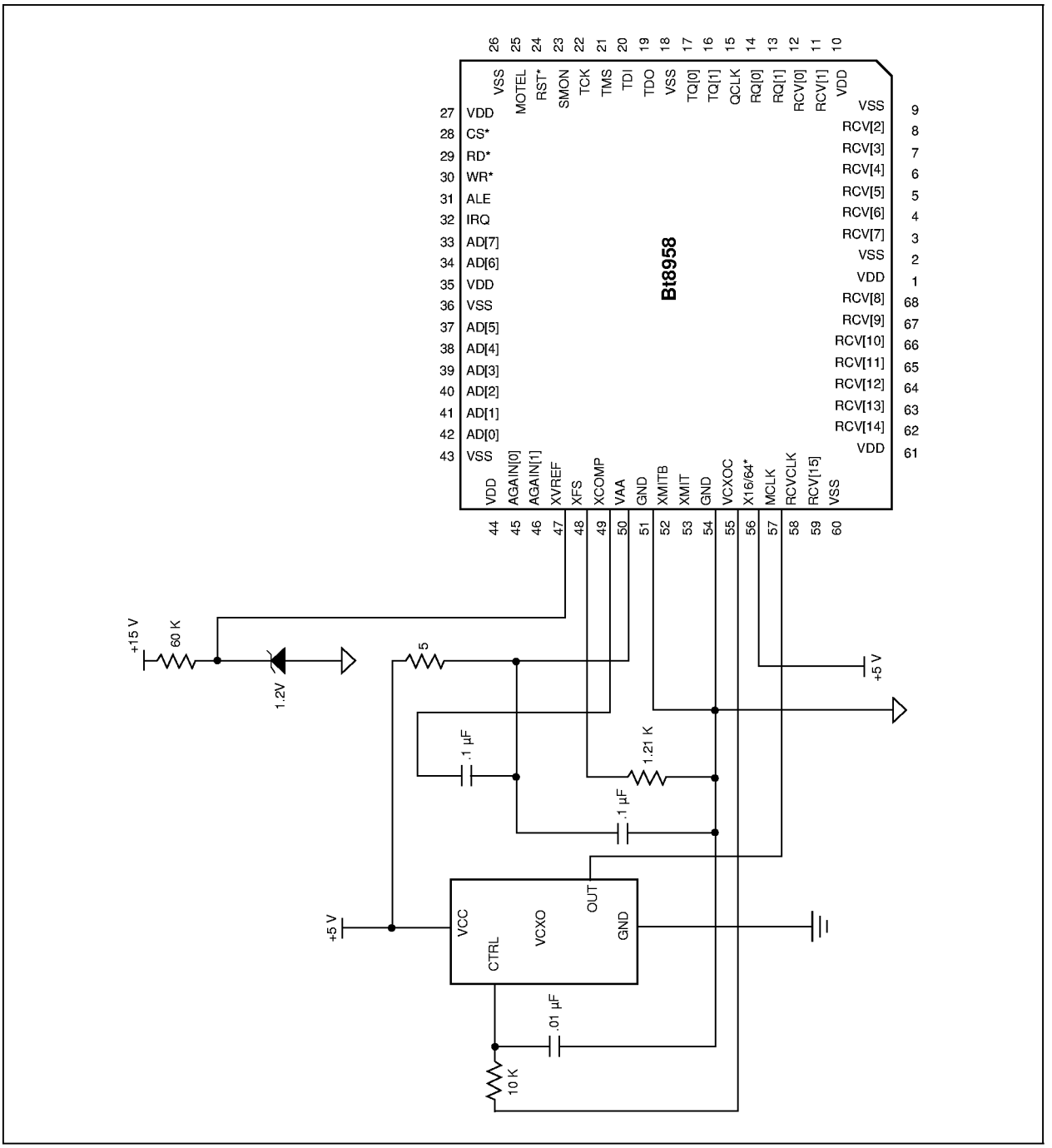
This section provides additional information on channel unit interface and analog front-end connections, and custom HDSL analog components.

Electrical Connections

Clock Recovery

In an HTU-R terminal, the recovered clock frequency from the incoming 2B1Q waveform must be used to synchronize transmission back to the HTU-C. This is accomplished inside the transceiver with a Phase Lock Loop (PLL) circuit that requires connection to an external Voltage-Controlled Crystal Oscillator (VCXO). The control voltage for the VCXO is generated by an on-chip sigma-delta DAC. The sigma-delta scheme requires only a simple RC reconstruction filter between the transceiver's VCXOC output pin and the VCXO. This connection along with a number of other analog connections, is detailed in Figure A-1 for the case where the VCXO frequency provided is 16 times the desired symbol clock rate. This is the required configuration for single-pair HDSL systems.

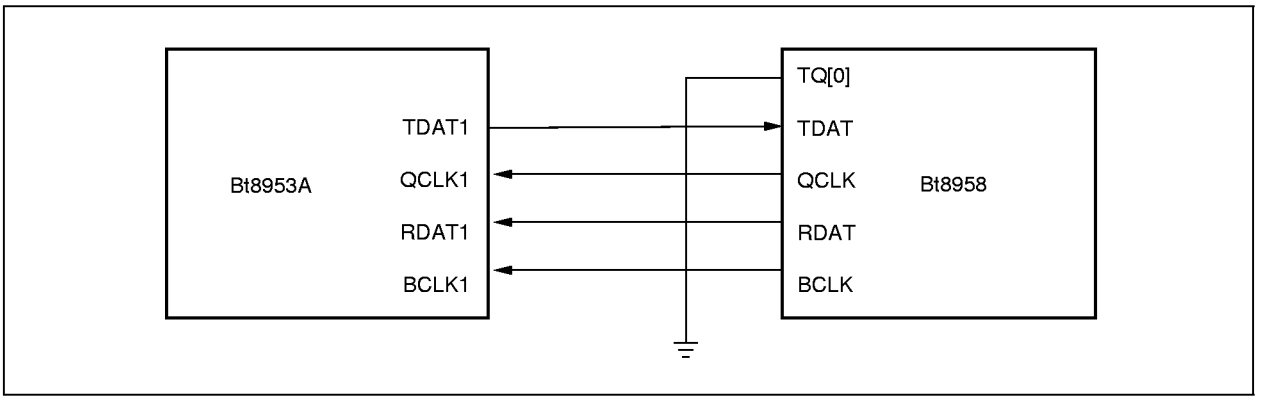
Figure A–1. Analog Connections



Channel Unit Connection

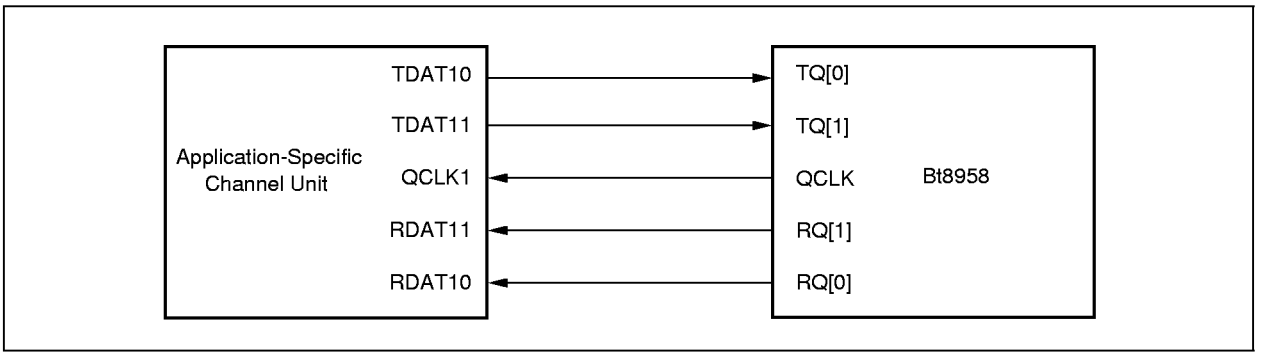
Four different interface protocols are supported for connecting to HDSL channel units/framers: two parallel modes, referred to as parallel master and parallel slave; and two serial modes, referred to as serial sign first and serial magnitude first. Brooktree's Bt8953A Channel Unit device supports the serial sign first mode. Figure A-2 illustrates the connection between a single Bt8958 and the Bt8953A in this mode.

Figure A–2. Bt8953A Channel Unit Connection, Serial Sign First Mode



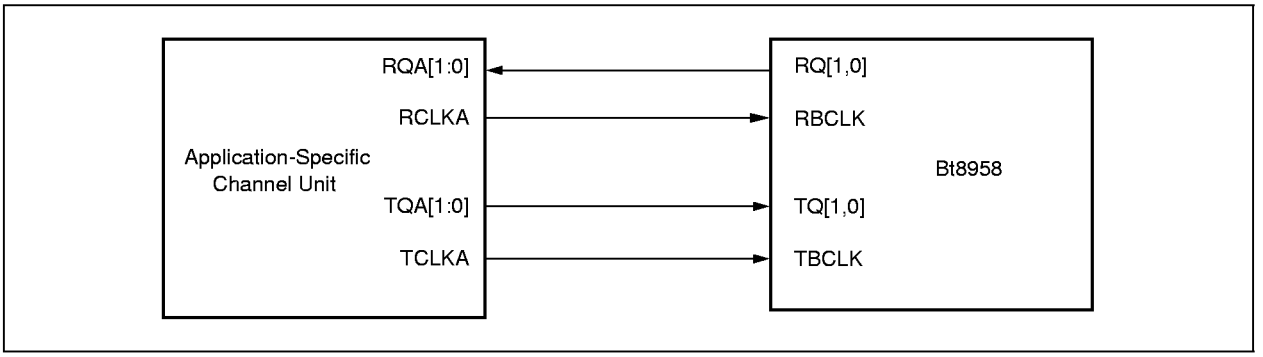
The two parallel interface modes may be used with application-specific HDSL channel unit/framer devices. In the parallel master mode, the single QCLK output from the Bt8958 is used to synchronize both transmit- and receive-quat interfaces. Figure A-3 shows typical connections for the parallel master mode.

Figure A–3. Application-Specific Channel Unit Connection, Parallel Master Mode



In parallel slave mode, two alternate pin functions, RBCLK and TBCLK, are used to synchronize the transmit/receive quat interfaces. RBCLK is an input used to strobe receive symbols out of the Bt8958 onto the RQ[1,0] interface. TBCLK is an input used to latch transmit symbols off the TQ[1,0] interface into the Bt8958. Connections for the parallel slave interface mode are shown in Figure A-4.

Figure A–4. Application-Specific Channel Unit Connection, Parallel Slave Mode



NOTE: In parallel slave mode, small FIFOs are included in both the transmit and receive paths to ease timing constraints at the interface. However, RBCLK and TBCLK must still be running at exactly the same frequency as the symbol clock, QCLK. After starting the transceivers, the FIFO's pointers must be reset to their initial positions using fifos_mode [bit 2] of the Channel Unit Interface Modes Register [cu_interface_modes; 0x06]. This maximizes the amount of phase offset allowed between TBCLK, RBCLK, and QCLK.

Analog Front End

The Analog Front-End (AFE) provides analog automatic gain control, filtering, and receive hybrid functions on the receive side, as well as DAC current-to-voltage conversion, reconstruction filtering, and power amplification on the transmit side. There are a number of ways of implementing this function which trade off performance, power, cost, size, etc. The best solution for any given system depends upon the particular design requirements and constraints unique to that system design.

Brooktree is putting together complete reference designs for HDSL terminals conforming to the proposed single-pair ETSI and ANSI specifications. We will offer complete Evaluation Systems (EVMs) for each of these reference designs. A set of schematics showing our design for the AFE, as well as all other required circuitry, is available at no cost. Please contact your local sales representative for information and availability.

Component Specifications

XO and VCXO Specification

Table A–1 specifies Crystal Oscillator (XO) and Voltage-Controlled Crystal Oscillator (VCXO) characteristics for use with the Bt8958. Brooktree has identified the following vendors for both components.

Connor-Winfield Corp.
2111 Comprehensive Dr.
Aurora, Il. 60505
TEL: (708) 851-4722
FAX: (708) 851-5040

FOX Electronics
5842 Corporation Circle
Fort Meyers, FL 33905
TEL: (813) 693-0099
FAX: (813) 693-1554

General Electronic Devices
352 "c" Rancheros Drive
San Marcos, Ca 92069
TEL: (619) 591-4170
FAX: (619) 591-4164

Table A–1. Crystal Oscillator/Voltage-Controlled Crystal Oscillator Specification

Parameter	Requirement
Center Frequency @ 1552 kbps Operation(1)	12.416 MHz
Center Frequency @ 2320 kbps Operation(2)	18.560 MHz
XO Accuracy/Stability(3)	±32 ppm
VCXO Frequency Pull Range	±50 to ±100 ppm
VCXO Control Voltage Range	0.1 x V_{DD} to 0.9 x VDD
VCXO Control Voltage Input Impedance	≥50 kΩ
V_{OH}	2.4 V min
V_{OL}	0.4 V max
Temperature Range	–40° to 85° C

Notes: (1). Using the internal MCLK multiplier (X16/64* = 1). Supports single-pair ANSI applications.
(2). Using the internal MCLK multiplier (X16/64* = 1). Supports single-pair ETSI applications.
(3). Must be maintained over temperature, supply voltage, aging extremes. May also apply to a VCXO at the center control voltage (VDD ÷ 2) if used as a fixed oscillator in central-office applications.

HDSL Transformer Specification

Table A–2 lists the HDSL transformed specification. Table A–5 illustrates the HDSL transformer. HDSL transformer target characteristics for single-pair operation are under development at the time of this printing. Details will be provided as they become available. Brooktree has identified the following vendors for HDSL transformers.

Schott
1000 Parkers Lake Road
Minneapolis, MN 55391
TEL: (612) 475-1173
FAX: 612) 475-1786

Pulse
P. O. Box 12235
San Diego, CA 92112
TEL: (619) 674-8125
FAX: (619) 674-4486

Midcom
P. O. Box 1330
Watertown, SD 57201
TEL: (800) 643-2661
FAX: (605) 886-4486

Table A–2. HDSL Transformer Specifications

Parameter	1552 kbps Operation	2320 kbps Operation
General Requirements		
Turns Ratio (Line Side: Circuit Side)	2.5 Split: 1	2.5 Split: 1
Line-Side OCL (±5%)	2 mH	1 mH
Maximum Total Harmonic Distortion (measured across circuit side; R_L = 50 Ω; I_L = min DC current; R_S = 21 Ω; V_S = 4.0 V_{p-p} @ 80 kHz)	–TBD dB	–TBD dB
Maximum Insertion Loss R_L = 135 Ω; R_S = 21 Ω	0.5 dB 80 – 400 kHz –20 dB/Decade below 80 kHz 20 dB/Decade above 400 kHz	0.5 dB 80 – 600 kHz –20 dB/Decade below 80 kHz 20 dB/Decade above 600 kHz
Minimum Line-Side Return Loss R_{REF} = 135 Ω; R_S = 21 Ω	21 dB 80 – 400 kHz 20 dB/Decade below 80 kHz –20 dB/Decade above 400 kHz	17 dB 80 – 600 kHz 20 dB/Decade below 80 kHz –20 dB/Decade above 600 kHz
Minimum Line-Side Longitudinal Balance R_L = 135 Ω; R_S = 21 Ω	53 dB to 400 kHz –20 dB/Decade above 400 kHz	53 dB to 600 kHz –20 dB/Decade above 600 kHz
Application-Specific Requirements		
Operating Temperature Range	–40° to +85° C	–40° to +85° C
Minimum DC Current	60 mA	60 mA
Minimum Dielectric Strength	2500 V	2500 V
Minimum Creepage and Clearance	–	–

Figure A-5. HDSL Transformer