International
IOR Rectifier

SERIES B25RIA/B25H2S

SCR **Power Modules**

25A

Features

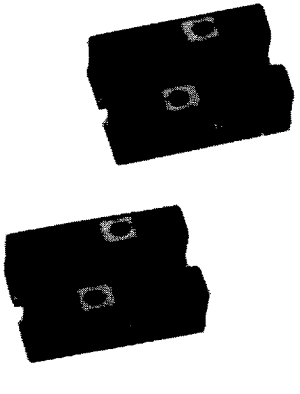
- Glass passivated junctions for greater reliability
- Electrically isolated base plate (3500V RMS)
- Available up to 1200 V_{RRM}, V_{DRM}
- High surge capability
- Large creepage distances
- Simplified mechanical designs, rapid assembly
- B-package case style
- UL E78996 approved

Description

The B25RIA../B25H2S.. series of B-modules consist of power thyristors in single and split configuration in single package. With their isolating base plate, mechanical designs are greatly simplified giving advantages of cost reduction and reduced size.
Applications include power supplies, control circuits, light dimmers and battery chargers.

Major Ratings and Characteristics

Parameters		B25RIA/B25H2S	Units
$I_{T(AV)}$		25	A
	@ T_C	70	°C
I_{TSM}	50Hz	390	A
	60Hz	410	A
I^2t	50Hz	770	A^2s
	60Hz	700	A^2s
$I^2\sqrt{t}$		7700	$A^2\sqrt{s}$
V_{RRM}	range	100 to 1200	V
T_J		-40 to 125	°C



ELECTRICAL SPECIFICATIONS

Voltage Ratings

Part number	Voltage Code	I_{RRM}, I_{DRM} max peak reverse and off-state leakage current at V_{RRM}, V_{DRM}, T_J = 125 °C, gate open circuit mA	V_{RRM}, V_{DRM} maximum repetitive peak reverse and off-state voltage gate open circuit V	V_{RSM} maximum non-repetitive peak reverse voltage V
B25 RIA B25 H2S	10	10	100	150
	20	10	200	300
	40	10	400	500
	60	10	600	700
	80	10	800	900
	100	10	1000	1100
	120	10	1200	1300

On-state Conduction

Parameter		Value	Units	Conditions		
$I_{T(AV)}$	Max. average on-state current	25	A	180° conduction half sine wave @ T_C = 70°C		
$I_{T(RMS)}$	Max. RMS on-state current	40	A			
I_{TSM}	Maximum peak one half cycle non repetitive surge current	390	A	10ms	No voltage reapplied	Sinusoidal half Wave Initial T_J=125°C
		410	A	8.3ms		
		330	A	10ms	100% V_{RRM} reapplied	Sinusoidal half Wave Initial T_J=125°C
		345	A	8.3ms		
I^2t	Maximum I^2t for fusing	770	A^2s	10ms	No voltage reapplied	Initial T_J=125°C
		700	A^2s	8.3ms		
		545	A^2s	10ms	100% V_{RRM} reapplied	Initial T_J=125°C
		490	A^2s	8.3ms		
$I^2\sqrt{t}$	Maximum $I^2\sqrt{t}$ for fusing (1)	7700	$A^2\sqrt{s}$	t=0 to 10ms, no voltage reapplied, Initial T_J=125°C		
V_{TM}	Maximum peak on-state voltage	1.6	V	T_J=25°C, I_{TM}=$I_{T(AV)}$ x π, tp=400 µs, 180° conduction		
$V_{T(TO)}$	Max. value of threshold voltage	0.90	V	Low level (3)	T_J=T_J max (2)	
		1.15	V	High level (4)		
r_t	Max. value of on-state slope resistance	12.5	mΩ	Low level (3)	T_J=T_J max (2)	
		9.7	mΩ	High level (4)		
I_H	Maximum holding current	100	mA	T_J=25°C anode supply=6V, resistive load, gate open, Initial I_T=1A		
I_L	Maximum latching current	200	mA	T_J=25°C anode supply=6V, resistive load		
$di/_{dt}$	Maximum rate of rise of off-state voltage					
	V_{DRM} ≤600V	200	A/µs	T_J=125°C, from 0.67 V_{DRM}		
	V_{DRM} =800V	180	A/µs	I_{TM} = π x $I_{T(AV)}$, I_g = 500mA		
	V_{DRM} =1000V	160	A/µs	t_r < 0.5 µs, t_p > 6 µs		
	V_{DRM} >=1100V	150	A/µs			

(1) I^2t for time t_x = $I^2\sqrt{t}$ x $\sqrt{t_x}$

(2) Average power = $V_{T(TO)}$ x $I_{T(AV)}$ + r_t x $(I_{T(RMS)})^2$

(3) 16.7% x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$

(4) π x $I_{T(AV)}$ < I < 20 x π x $I_{T(AV)}$

ELECTRICAL SPECIFICATIONS

Triggering

	Parameter	B25RIA/B25H2S	Units	Conditions
P_{GM}	Maximum peak gate power	8.0	W	
$P_{G(AV)}$	Maximum average gate power	2.0	W	
$+I_{GM}$	Maximum peak gate current	1.5	A	
$-V_{GM}$	Maximum peak negative gate voltage	10	V	
V_{GT}	Maximum required DC gate current to trigger	3.0	V	T_J=-65°C, Anode supply = 6V, resistive load
		2.0	V	T_J= 25°C, Anode supply = 6V, resistive load
		1.0	V	T_J= 125°C, Anode supply = 6V, resistive load
I_{GT}	Maximum required DC gate current to trigger	90	mA	T_J=-65°C, Anode supply = 6V, resistive load
		60	mA	T_J= 25°C, Anode supply = 6V, resistive load
		35	mA	T_J= 125°C, Anode supply = 6V, resistive load
V_{GD}	Maximum gate voltage that will not trigger	0.2	V	@ T_J=125°C, rated V_{DRM} applied
I_{GD}	Maximum gate current that will not trigger	2.0	mA	@ T_J=125°C, rated V_{DRM} applied

Switching

t_{gd}	Typical turn-on time	0.9	µs	T_J= 25°C
t_{rr}	Typical reverse recovery time	4	µs	T_J= 125°C (5)
t_q	Typical turn-off time	110	µs	T_J= 125°C (6)

Blocking

dv/dt	Minimum critical rate-of-rise of off-state voltage	100	V/µs	T_J= 125°C, Linear to 100% rated V_{DRM}
		300	V/µs	T_J= 125°C, Linear to 67% rated V_{DRM}
I_{RRM} I_{DRM}	Maximum peak reverse and off-state leakage current at V_{RRM}, V_{DRM}	10	mA	T_J=125°C, gate open circuit
I_{RM}	Max. peak reverse leakage current	100	µA	T_J = 25°C
V_{INS}	RMS isolation voltage	3500	V	50Hz, circuit to base, all terminals shorted T_J = 25°C, t = 1 s

Thermal and Mechanical Specifications

T_J	Junction temperature range	-40 to 125	°C	
T_{stg}	Storage temperature range	-40 to 125	°C	
R_{thJC}	Maximum thermal resistance, junction to case	1.05	K/W	Per junction - DC operation
R_{thC-S}	Max. thermal resistance case to heatsink	0.10/0.20	K/W	Mounting surface smooth flat and greased Per module/Per junction
T	Mounting torque±10% Module to heatsink	1.7	Nm	M4 mounting screws (7) Non-lubricated threads
	Module Terminals	0.45	Nm	M3 screw terminals; Non-lubricated threads
wt	Approximate weight	40	g	
	Case style	"B" Type		See outline table

(5) I_{TM} = rated $I_{T(AV)}$ for at least 200 µs, $di_{R/dt}$ - 10 A/µs

(6) I_{TM} = rated $I_{T(AV)}$ for at least 200 µs. Min. V_R during turn-off = 100V, reapplied $dv_{/dt}$ = 20 V/µs linear to 0.80 V_{DRM} - Gate bias 0V, 100 Ω

(7) A mounting compound is recommended and the torque should be rechecked after a period of about 3 hours to allow for the spread of the compound

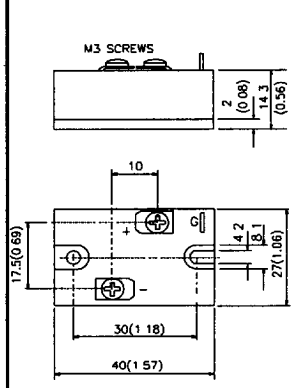
ΔR Conduction (per Junction)

(The following table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC)

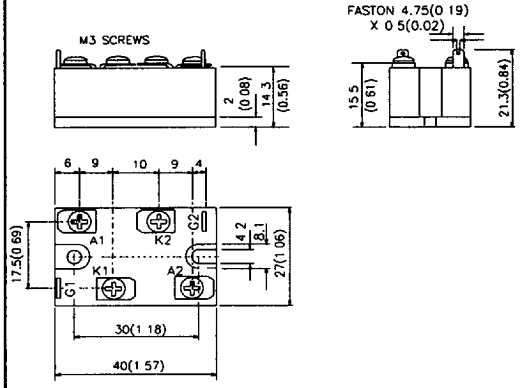
Conduction angle	Sinusoidal	Rectangular	Units
180°	0.25	0.18	K/W
120°	0.30	0.30	K/W
90°	0.38	0.41	K/W
60°	0.55	0.58	K/W
30°	0.95	0.96	K/W

Outlines Table

B25RIA



B25H2S



All dimensions in millimeters (inches)

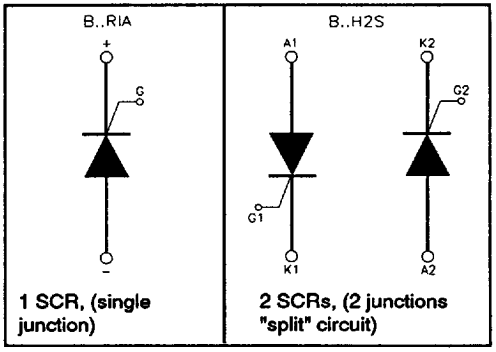
Ordering Information Table

Device Code

1	2	3	4	5	6
B	25	RIA	120	K	L

1 - Module type
2 - Average current
3 - Circuit configuration * *
4 - Voltage code (See Voltage ratings table)
5 - dv/dt code:
No letter = 300V/µs
D = 500V/µs
K = 1000V/µs
6 - Terminal type:
No letter = Screw terminal
L = Fast on

Circuit configuration * *



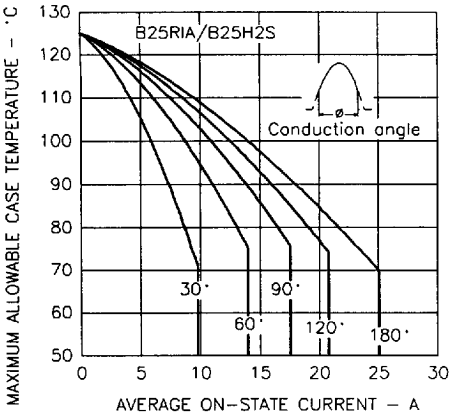


Fig. 1 - Current Ratings Characteristics

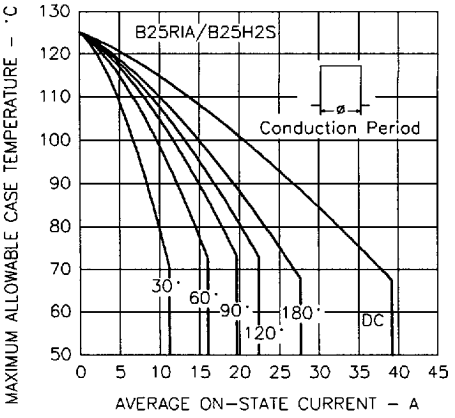


Fig. 2 - Current Ratings Characteristics

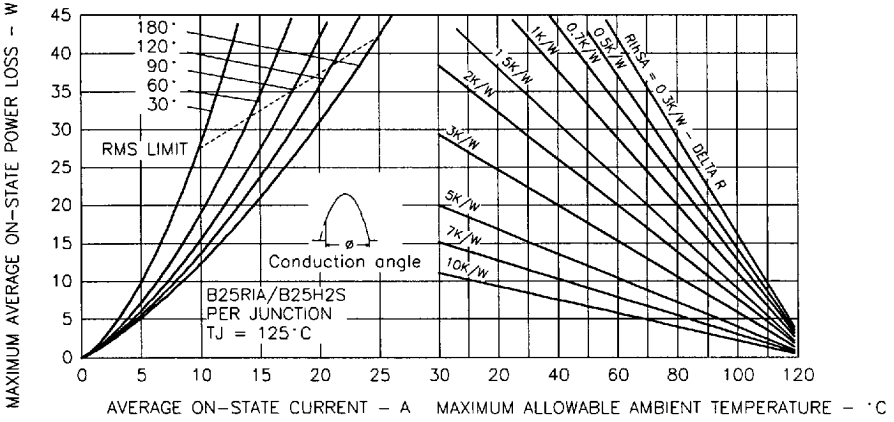


Fig. 3 - On-state Power Loss Characteristics

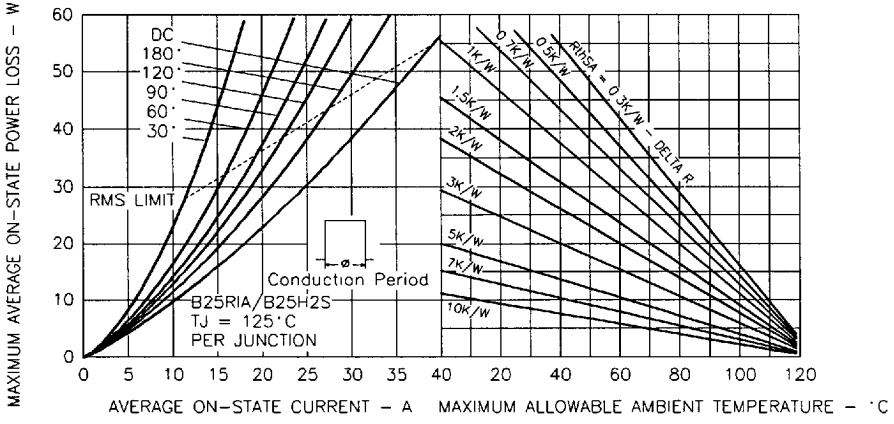


Fig. 4 - On-state Power Loss Characteristics

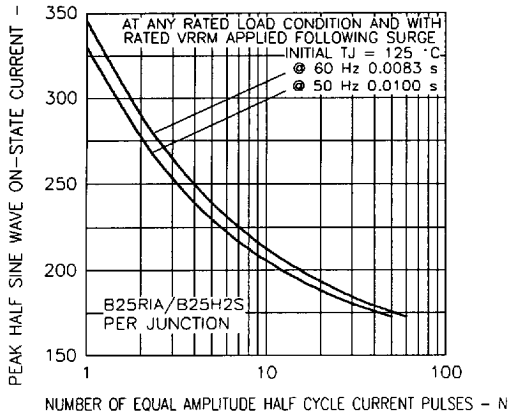


Fig. 5 - Maximum Non-Repetitive Surge Current

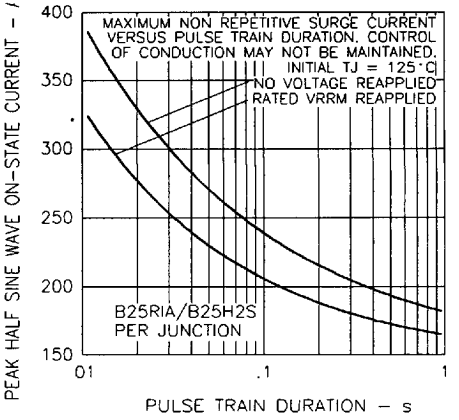


Fig. 6 - Maximum Non-Repetitive Surge Current

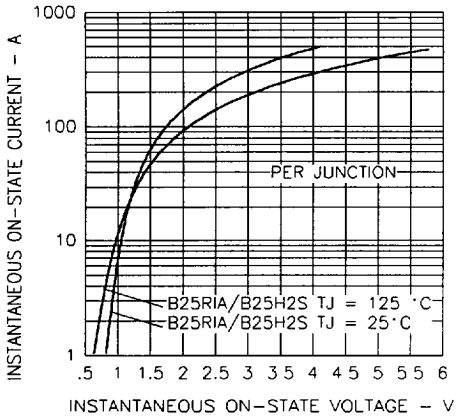


Fig. 7 - On-state Power Loss Characteristics

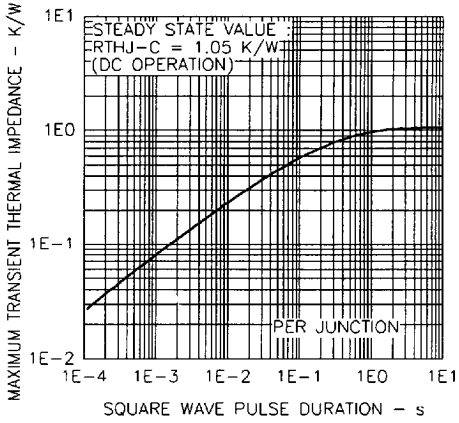


Fig. 8 - Thermal Impedance ZthJC Characteristics

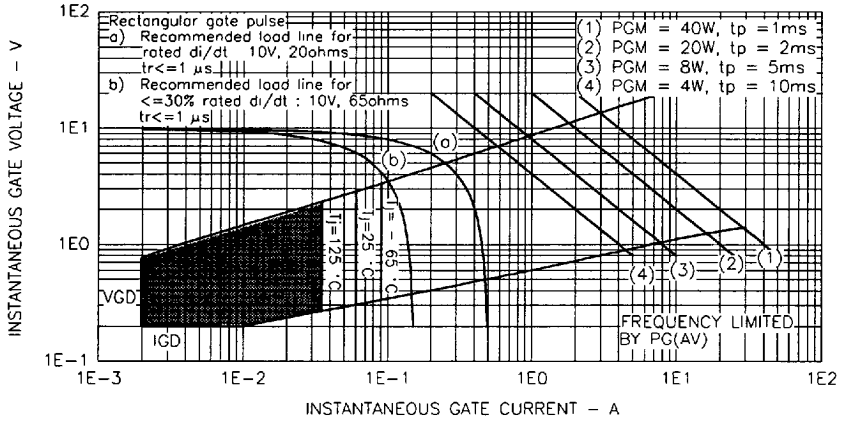


Fig. 9 - Gate Characteristics