128K X 8 SRAM

FEATURES

- Access times of 15,20 ns
- Fast output enable (t_{DOE}) for cache applications
- Low active power: 500 mW (Typical)
- Drives a 50 pF load vs. 30 pF Industry-standard load
- Low standby power
- Fully static operatio n, no clock or refresh required
- TTL Compatible Inputs and Outputs
- Single +5V power supply
- Package in Industry-standard 32-pin SOJ and 32-pin TSOP[1]
- Industrial and military temperature range

FUNCTIONAL DESCRIPTION

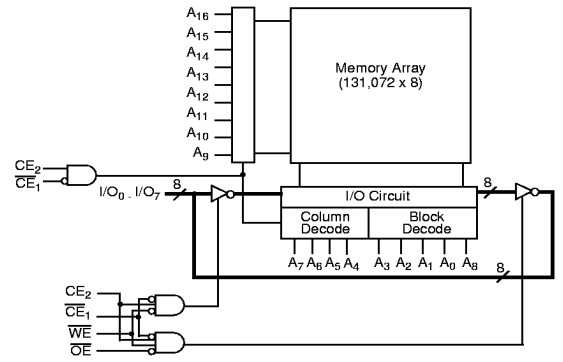
The ASI AS5C1008DJ is a high speed, low power, 128K word by 8-bit CMOS static RAM. It is fabricated using ASI's high performance CMOS, double metal technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 15ns (Max).

When Chip Enable ($\overline{CE}$) is HIGH, the device assumes a standby mode at which the power dissipation can be reduced down to 75mW (max) at CMOS input levels.

Easy memory expansion is provided by using asserted LOW $\overline{CE}$ and asserted HIGH CE_2 and asserted LOW write enable ($\overline{WE}$) controls both writing and reading of the memory.

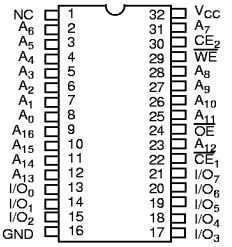
The AS5C1008DJ is pin-compatible with other 128K X 8 SRAM's in the SOJ, and TSOP package.

Block Diagram

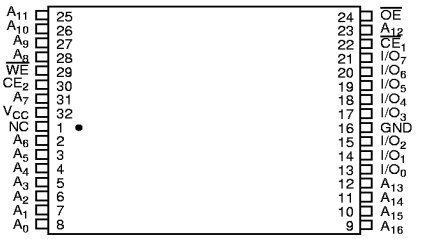


Pin Configurations

32-Pin SOJ
TOP VIEW



32-Pin TSOP
TOP VIEW



Selection Guide

	AS5C1008DJ-15	AS5C1008DJ-20
Maximum Access Time (ns)	15	20
Maximum Operating Current (mA)	140	130
Maximum Standby Current (mA)	25	25

Note:
1. 10 ns device available in SOJ, only.

ABSOLUTE MAXIMUM RATINGS

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....-65°C to +150°C

Ambient Temperature with Power Applied.....-55°C to +125°C

Vcc Supply Relative to GND.....-1.0V to +7.0V

Voltage on Any Pin Relative to GND.....-0.5V to Vcc +0.5V

Short Circuit Output Current[2].....±50mA

Power Dissipation.....1.0 W

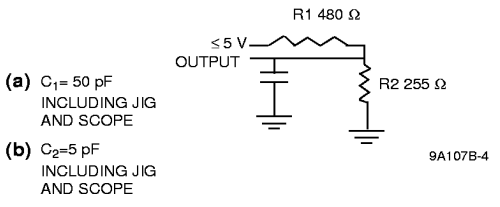
Electrical Characteristics Over the operating Range (-40°C ≤ TA ≤ 85°C, V_{CC}=5V ± 10%) - *Industrial*

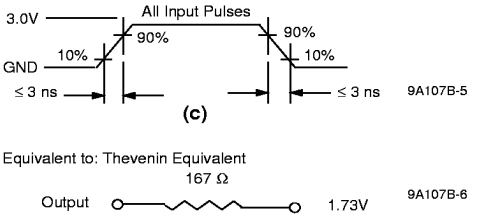
Symbol	Parameter	Test Conditions	AS5C1008DJ-15		AS5C1008DJ-20		Unit
			Min.	Max.	Min.	Max.	
I_{CC1}	Dynamic Operating Current	V_{CC} = Max., I_{OUT} = mA, $\overline{CE}_1$ = V_{IL} and CE_2 = V_{IH}, f = fmax		115		110	mA
I_{CC2}	Operating Current	V_{CC} = Max., I_{OUT} = mA, $\overline{CE}_1$ = V_{IL} and CE_2 = V_{IH}, f = 0		90		90	mA
I_{SB1}	TTL Standby Current -TTL Inputs	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL}, $\overline{CE}_1$ V_{IH} or CE_2 = V_{IL}, f=fmax		30		30	mA
I_{SB2}	CMOS Standby Current -CMOS Inputs	V_{CC} = Max., $\overline{CE}_1$ ≥ V_{CC} -0.2V, or CE_2 ≤ 0.2V, V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V , f = 0		15		15	mA
I_{LI}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}	-1	1	-1	1	µA
I_{LO}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC} Output Disabled	-1	1	-1	1	µA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4.0 mA	2.4		2.4		V
V_{OL}	Output Low Voltate	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input High Voltage		2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	V
V_{IL}	Input Low Voltage[3]		-0.5	0.8	-0.5	0.8	V

Capacitance[4]

Symbol	Description	Max.	Unit
C_{IN}	Input Capacitance	5	pF
C_{IO}	I/O Capacitance	5	pF

AC Test Loads and Waveforms [5, 6]





Notes:

2. No more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
3. V_{IL} = -3.0 V for pulse width less than 3 ns.
4. Tested initially and after any design or process changes that may effect these parameters.
5. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 - 3.0 V and output loading specified in AC Test Loads and Waveforms *Figure (a)*.
6. Tested with the load in AC Test Loads and Waveforms *Figure (b)*. Transition is measured ±500mV from steady state voltage.

Electrical Characteristics Over the operating Range (-55°C ≤ TA ≤ 125°C, V_{CC}=5V ± 10%) -*Military Temps.*

Symbol	Parameter	Test Conditions	AS5C1008DJ-15		AS5C1008DJ-20		Unit
			Min.	Max.	Min.	Max.	
I_{CC1}	Dynamic Operating Current	V_{CC} = Max., I_{OUT} = mA, $\overline{CE}_1$ = V_{IL} and CE_2 = V_{IH}, f = fmax		140		130	mA
I_{CC2}	Operating Current	V_{CC} = Max., I_{OUT} = mA, $\overline{CE}_1$ = V_{IL} and CE_2 = V_{IH}, f = 0		100		100	mA
I_{SB1}	TTL Standby Current -TTL Inputs	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL}, $\overline{CE}_1$ V_{IH} or CE_2 = V_{IL}, f=fmax		40		40	mA
I_{SB2}	CMOS Standby Current -CMOS Inputs	V_{CC} = Max., $\overline{CE}_1 \geq V_{CC}$ -0.2V, or $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$, f = 0		25		25	mA
I_{LI}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}	-1	1	-1	1	µA
I_{LO}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC} Output Disabled	-1	1	-1	1	µA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4.0 mA	2.4		2.4		V
V_{OL}	Output Low Voltate	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input High Voltage		2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	V
V_{IL}	Input Low Voltage[3]		-0.5	0.8	-0.5	0.8	V

Switching Characteristics Over the Operating Range [7,8,9,10]

Parameter	Description	AS5C1008DJ-15		AS5C1008DJ-20		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	15		20		ns
t_{AA}	Address Access Time		15		20	ns
t_{OHA}	Output Hold Time	3		3		ns
t_{ACE1}, t_{ACE2}	$\overline{CE}_1$, CE_2 Access Time		15		20	ns
t_{DOE}	$\overline{OE}$ Access Time		7		8	ns
t_{LZOE}	$\overline{OE}$ to Low-Z Output	0		0		ns
t_{HZOE}[6]	$\overline{OE}$ to High-Z Output		6		7	ns
t_{LZCE1}, t_{LZCE2}	$\overline{CE}_1$, CE_2 to Low-Z Output	3		3		ns
t_{HZCE1}, t_{HZCE2}	$\overline{CE}_1$, CE_2 to High-Z Output		8		9	ns
t_{PU}	$\overline{CE}_1$, CE_2 to Power Up	0		0		ns
t_{PD}	$\overline{CE}_1$, CE_2 to Power Down		15		20	ns
Write Cycle[11]						
t_{wc}	Write Cycle Time	15		20		ns
t_{SCE1}, t_{SCE2}	$\overline{CE}_1$, CE_2 to Write End	10		12		ns
t_{AW}	Address to Set-up Time to Write End	10		12		ns
t_{HA}	Address Hold to Write End	0		0		ns
t_{SA}	Address Set-up Time	0		0		ns
t_{pwe1}[12]	$\overline{WE}$ Pulse Width ($\overline{OE}$ = HIGH)	10		12		ns
t_{pwe2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW)	12		15		ns
t_{SD}	Data Set-up to Write End	7		10		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}[6]	$\overline{WE}$ LOW to High-Z Output		7		9	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z Output	2		2		ns

Notes:
7. $\overline{WE}$ is HIGH for a Read Cycle.
8. The device is continuously selected. $\overline{OE}$, $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.
9. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.
10. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.
11. The internal write time is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a write, but any signal can be deasserted to terminate the write. The Data Input Set-up and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
12. Tested with $\overline{OE}$ HIGH.

Pin Descriptions

A_0 - A_{16}: Address Inputs

These 17 address inputs select one of the 131,072 8-bit words in the RAM.

$\overline{CE}_1$: Chip Enable 1 Input

$\overline{CE}_1$ is asserted LOW. The Chip Enable 1 is asserted LOW to read from or write to the device. If Chip Enable 1 is deasserted, the device is deselected and is in a standby power mode. The I/O pins will be in the high-impedance state when the device is deselected.

CE_2: Chip Enable 2 Input

CE_2 is asserted HIGH. The Chip Enable 2 is asserted HIGH to read from or write to the device. If Chip Enable 2 is deasserted, the device is deselected and is in a standby power mode. The I/O pins will be in the high-impedance state when the device is deselected.

$\overline{OE}$: Output Enable Input

The Output Enable input is asserted LOW. If the Output Enable is asserted LOW while $\overline{CE}_1$ is asserted (LOW) and CE_2 is asserted (HIGH) and $\overline{WE}$ is deasserted (HIGH), data from the SRAM will be present on the I/O pins. The I/O pins will be in the high-impedance state when $\overline{OE}$ is deasserted.

$\overline{WE}$: Write Enable Input

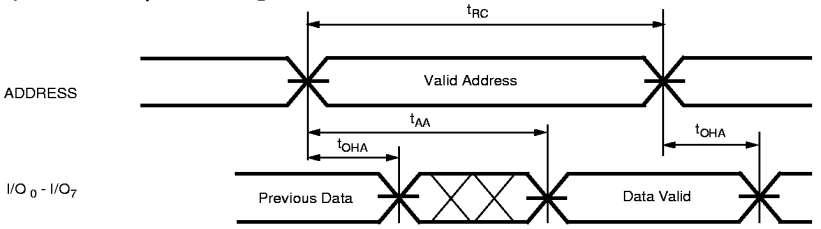
The Write Enable input is asserted LOW and controls read and write operations. When $\overline{CE}_1$ and $\overline{WE}$ are both asserted (LOW) and CE_2 is asserted (HIGH) input data present on the I/O pins will be written into the selected memory location.

I/O_0 - I/O_7: Common Input/Output Pins

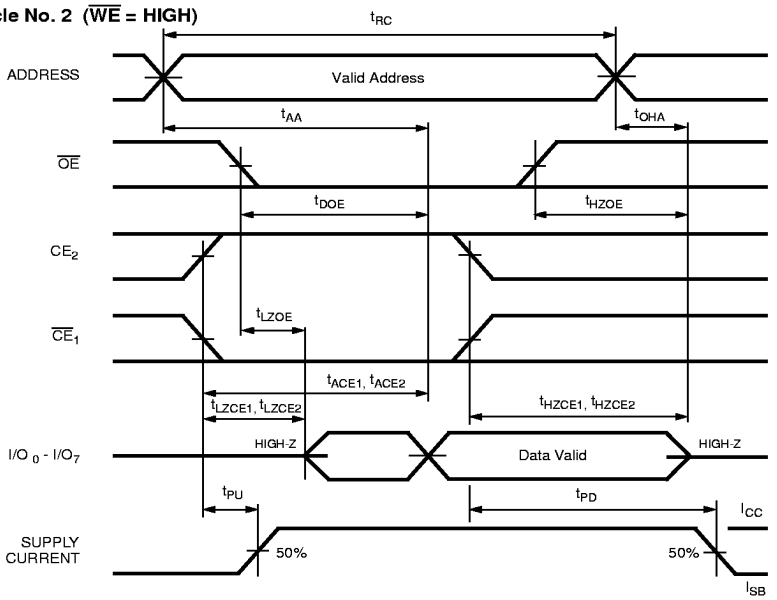
GND: Ground

Switching Waveforms

Read Cycle No. 1 ($\overline{CE}_1$ = LOW, CE_2 = HIGH, $\overline{OE}$ = LOW, $\overline{WE}$ = HIGH)

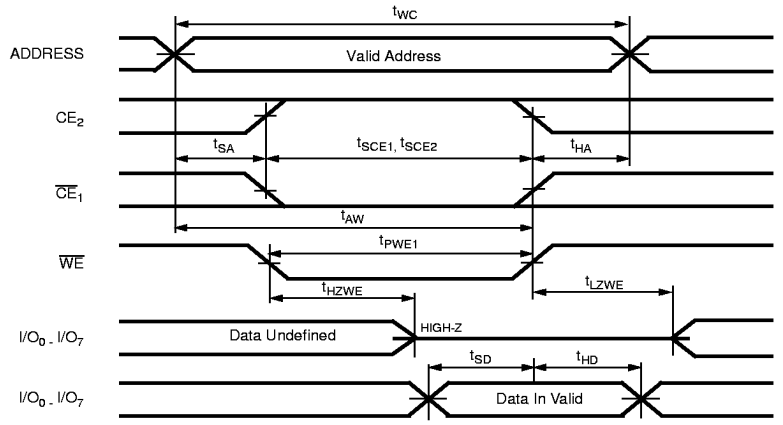


Read Cycle No. 2 ($\overline{WE}$ = HIGH)

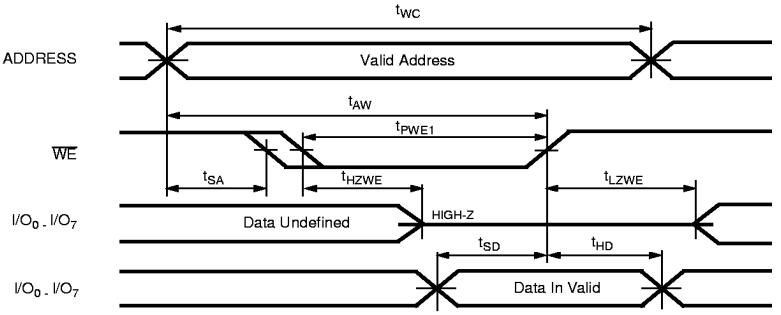


Switching Waveforms (continued)

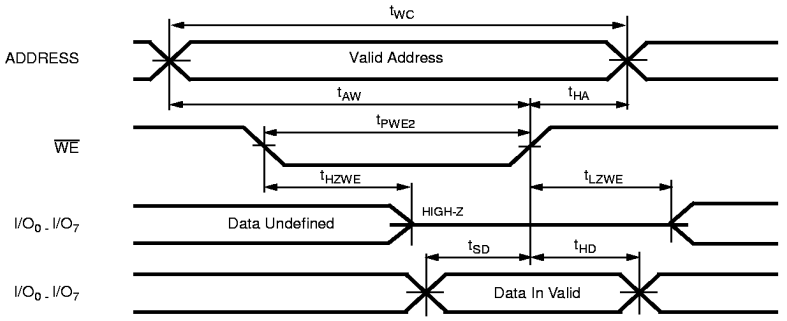
Write Cycle No.1 ($\overline{CE}_1$, or CE_2 controlled, $\overline{OE}$ is HIGH or LOW: $\overline{CE}_1$ or CE_2 Terminates Write)



Write Cycle No.2 ($\overline{WE}$ controlled, $\overline{OE}$ is HIGH, $\overline{CE}_1$ is LOW, and CE_2 is HIGH: $\overline{WE}$ Terminates Write)



Write Cycle No.3 ($\overline{WE}$ controlled, $\overline{OE}$ is LOW, CE_2 is HIGH, $\overline{CE}_1$ is LOW: $\overline{WE}$ Terminates Write)

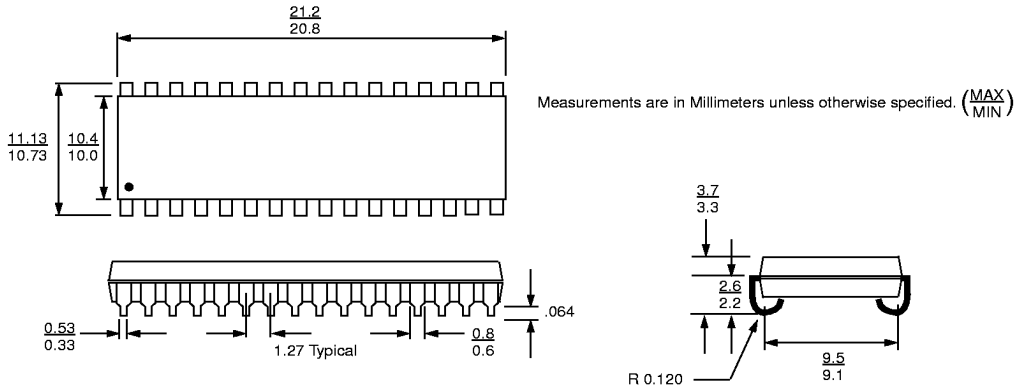


Truth Table

Mode	$\overline{WE}$	$\overline{CE}_1$	CE_2	$\overline{OE}$	I/O	I_{CC}
Standby	X	H	X	X	High-Z	I_{SB1}, I_{SB2}
Standby	X	X	L	X	High-Z	I_{SB1}, I_{SB2}
Selected/Output Disabled	H	L	H	H	High-Z	I_{CC1}, I_{CC2}
Read	H	L	H	L	D_{OUT}	I_{CC1}, I_{CC2}
Write	L	L	H	X	D_{IN}	I_{CC1}, I_{CC2}

Package Diagrams

32-Pin (400-Mil) Small Outline J-Bend (SOJ)



32-Pin Thin Small Outline Package (TSOP)