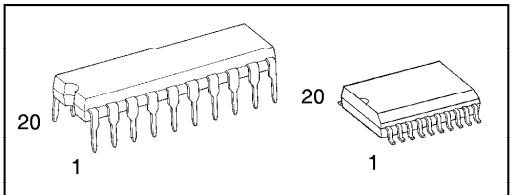
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74ACT573P, TC74ACT573F, TC74ACT573FW, TC74ACT573FT

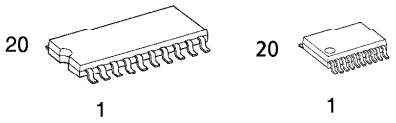
OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

(Note) The JEDEC SOP (FW) is not available in Japan.

The TC74ACT573 is an advanced high speed CMOS OCTAL LATCH fabricated with silicon gate and double-layer metal wiring C^2MOS technology.
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
These 8-bit D-type latches are controlled by a latch enable (LE) and a output enable input ($\overline{OE}$).
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



P (DIP20-P-300-2.54A) Weight : 1.30g (Typ.)
FW (SOL20-P-300-1.27) Weight : 0.46g (Typ.)

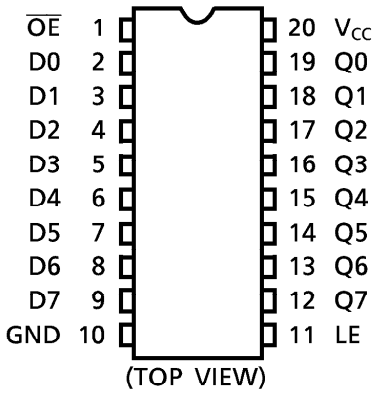


F (SOP20-P-300-1.27) Weight : 0.22g (Typ.)
FT (TSSOP20-P-0044-0.65) Weight : 0.08g (Typ.)

FEATURES :

- High Speed ..... t_{pd} = 5.5ns (typ.) at V_{CC} = 5V
- Low Power Dissipation ..... I_{CC} = 8μA(Max.) at Ta = 25°C
- Compatible with TTL outputs .... V_{IL} = 0.8V (Max.)
  V_{IH} = 2.0V (Min.)
- Symmetrical Output Impedance ... $|I_{OH}| = I_{OL}$ = 24mA (Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \simeq t_{pHL}$
- Pin and Function Compatible with 74F573

PIN ASSIGNMENT

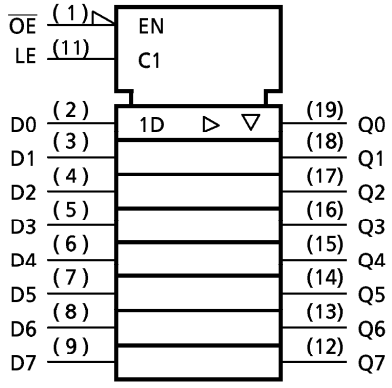


TRUTH TABLE

INPUTS			OUTPUTS
$\overline{OE}$	LE	D	Q
H	X	X	Z
L	L	X	Q_n
L	H	L	L
L	H	H	H

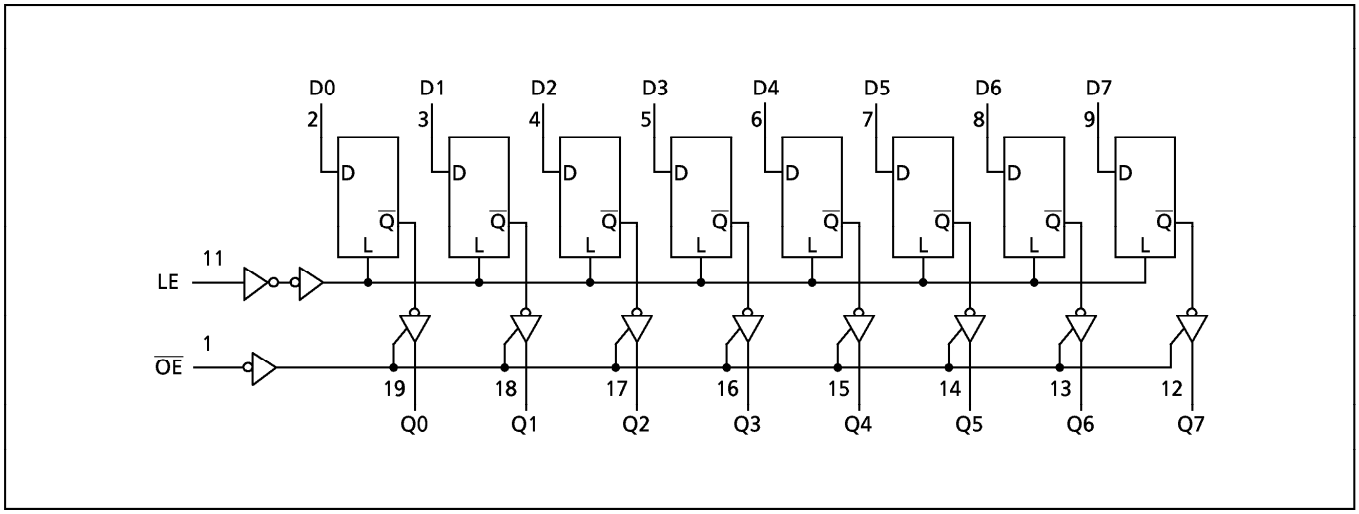
X : Don't Care
Z : High Impedance
Q_n : Q outputs are latched at the time when the LE input is taken to a low logic level.

IEC LOGIC SYMBOL



961001EBA2

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500 (DIP)*/ 180 (SOP/TSSOP)	mW
Storage Temperature	T_{stg}	−65~150	°C

*500mW in the range of Ta= −40°C~65°C. From Ta=65°C to 85°C a derating factor of −10mW/°C should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dV	0~10	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V_{IL}			4.5 ~ 5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	4.5	4.4	4.5	—	4.4	—	V
			I_{OH} = −24mA	4.5	3.94	—	—	3.80	—	
			I_{OH} = −75mA*	5.5	—	—	—	3.85	—	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	4.5	—	0.0	0.1	—	0.1	V
			I_{OL} = 24mA	4.5	—	—	0.36	—	0.44	
			I_{OL} = 75mA*	5.5	—	—	—	—	1.65	
3 - State Output Off - State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.5	—	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	±0.1	—	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	8.0	—	80.0	
	I_C	PER INPUT : V_{IN} = 3.4V OTHER INPUT : V_{CC} or GND		5.5	—	—	1.35	—	1.5	mA

* : This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C	Ta = −40~85°C	UNIT
				LIMIT	LIMIT	
Minimum Pulse Width (LE)	$t_{W(H)}$		5.0 ± 0.5	5.0	5.0	ns
Minimum Set - up Time	t_s		5.0 ± 0.5	3.0	3.0	
Minimum Hold Time	t_h		5.0 ± 0.5	2.0	2.0	

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, R_L = 500Ω, Input $t_r = t_f$ = 3ns)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = −40~85°C		UNIT
		V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (LE−Q)	t_{pLH} t_{pHL}	5.0 ± 0.5	−	6.3	10.5	1.0	12.0	ns
Propagation Delay Time (Dn−Q)	t_{pLH} t_{pHL}	5.0 ± 0.5	−	6.2	9.6	1.0	11.0	
Output Enable Time	t_{pZL} t_{pZH}	5.0 ± 0.5	−	6.5	10.0	1.0	11.5	
Output Disable Time	t_{pLZ} t_{pHZ}	5.0 ± 0.5	−	6.5	8.8	1.0	10.0	
Input Capacitance	C_{IN}		−	5	10	−	10	pF
Output Capacitance	C_{OUT}		−	10	−	−	−	
Power Dissipation Capacitance	C_{PD} (1)		−	22	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

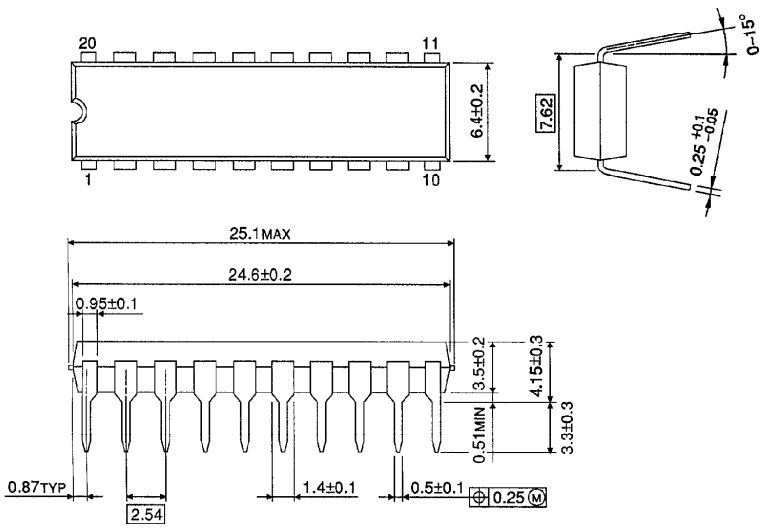
Average operating current can be obtained by the equation :

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per Latch)}$$

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation:

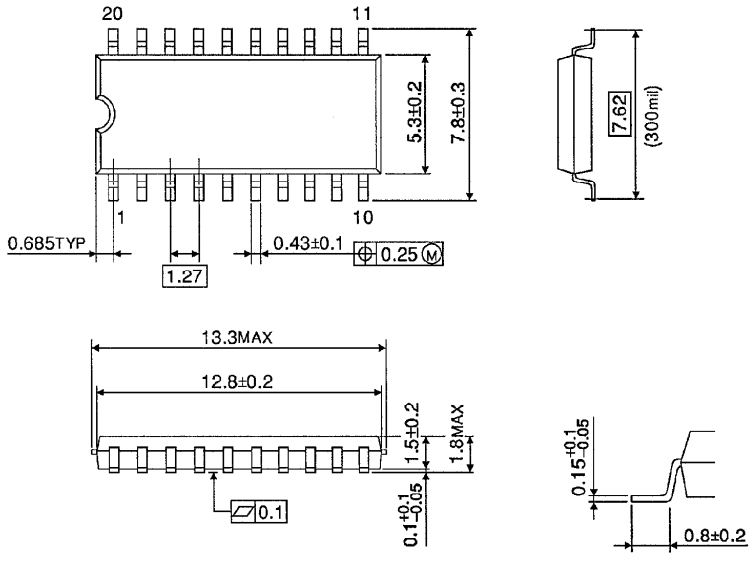
$$C_{PD}(total) = 6 + 16 \cdot n$$

DIP 20PIN OUTLINE DRAWING (DIP20-P-300-2.54A) Unit in mm



Weight : 1.30g (Typ.)

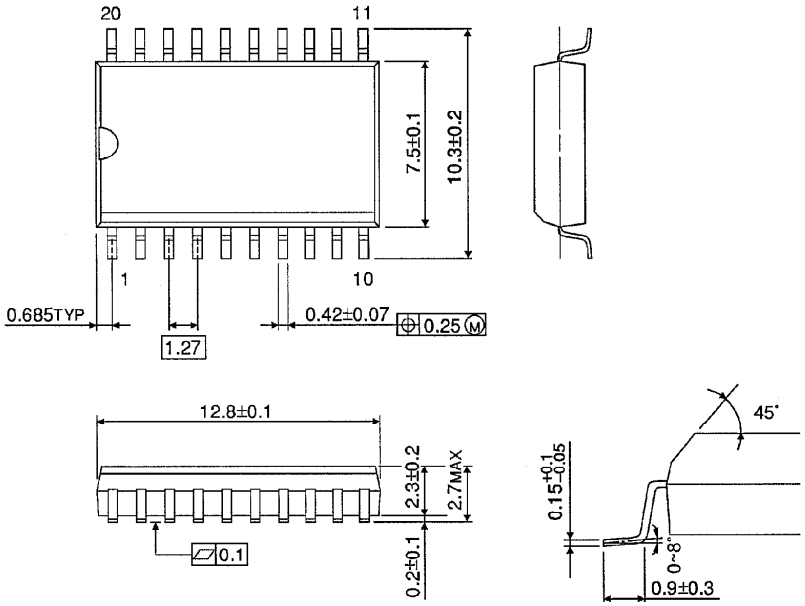
SOP 20PIN (200mil BODY) OUTLINE DRAWING (SOP20-P-300-1.27) Unit in mm



Weight : 0.22g (Typ.)

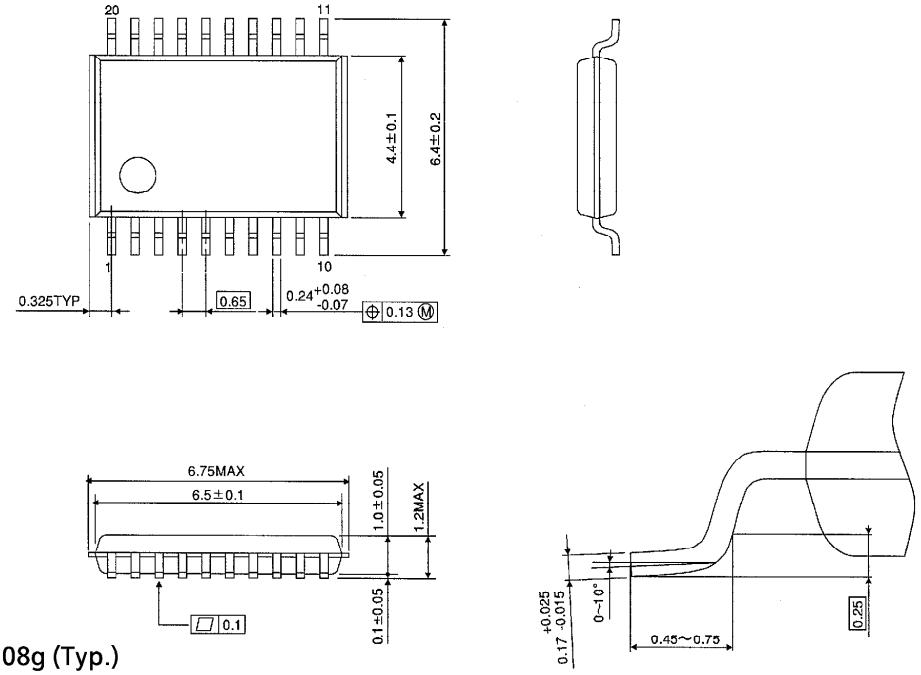
SOP 20PIN (300mil BODY) OUTLINE DRAWING (SOL20-P-300-1.27) Unit in mm

(Note) This package is not available in Japan.



Weight : 0.46g (Typ.)

TSSOP 20PIN OUTLINE DRAWING (TSSOP20-P-0044-0.65) Unit in mm



Weight : 0.08g (Typ.)