NCP4555, NCP4586

100 mA and 150 mA CMOS LDOs with Shutdown and $\overline{\text{Error}}$ Output

The NCP4555 and NCP4586 are high accuracy (typically ±0.5%) CMOS upgrades for older (bipolar) low dropout regulators. Designed specifically for battery–operated systems, the devices' CMOS construction eliminates wasted ground current, significantly extending battery life. Total supply current is typically 50 μA at full load (20 to 60 times lower than in bipolar regulators).

The devices' key features include ultra low noise operation, very low dropout voltage – typically 180 mV (NCP4555) and 270 mV (NCP4586) at full load – and fast response to step changes in load. An error output ($\overline{\text{ERROR}}$) is asserted when the devices are out–of–regulation (due to a low input voltage or excessive output current). $\overline{\text{ERROR}}$ can be used as a low battery warning or as a processor $\overline{\text{RESET}}$ signal (with the addition of an external RC network). Supply current is reduced to 0.5 μA (max) and both V_{OUT} and $\overline{\text{ERROR}}$ are disabled when the shutdown input is low. The devices incorporate both over–temperature and over–current protection.

The NCP4555 and NCP4586 are stable with an output capacitor of only 1.0 μF and have a maximum output current of 100 mA and 150 mA, respectively. For higher output current regulators, please see the NCP4569 (I_{OUT} = 300 mA) data sheet.

Features

- Zero Ground Current for Longer Battery Life
- Very Low Dropout Voltage
- Guaranteed 100 mA and 150 mA Output (NCP4555 and NCP4586 Respectively)
- High Output Voltage Accuracy
- Standard or Custom Output Voltages
- Power–Saving Shutdown Mode
- $\overline{\text{ERROR}}$ Output Can Be Used as a Low Battery Detector, or Processor Reset Generator
- Over–Current and Over–Temperature Protection
- Space–Saving 5–Pin SOT–23A Package
- Pin Compatible Upgrades for Bipolar Regulators

Applications

- Battery–Operated Systems
- Portable Computers
- Medical Instruments
- Instrumentation
- Cellular/GSMS/PHS Phones
- Linear Post–Regulators for SMPS
- Pagers

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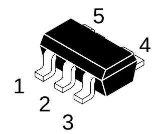
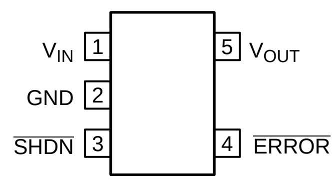


SOT–23
SN SUFFIX
CASE 1212

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 11 of this data sheet.

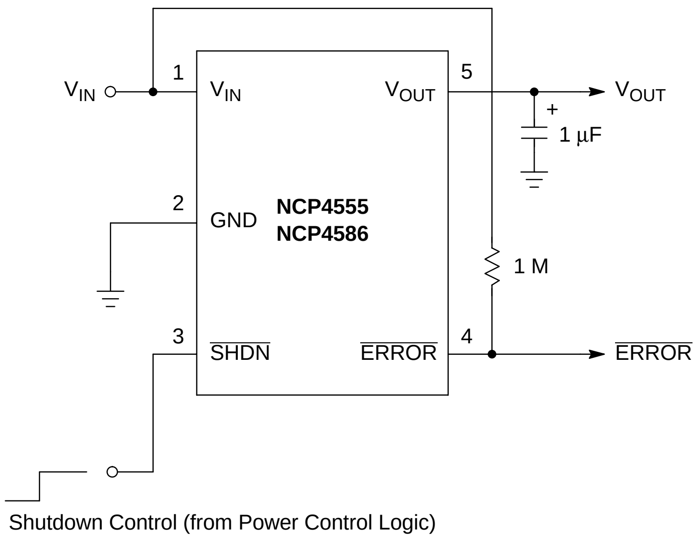


Figure 1. Typical Application

ABSOLUTE MAXIMUM RATINGS*

Rating		Symbol	Value	Unit
Input Voltage		–	6.5	V
Output Voltage		–	–0.3 to V_{IN} + 0.3	V
Power Dissipation		–	Internally Limited	–
Operating Temperature Range		T_A	–40 < T_J < 125	°C
Storage Temperature		T_{stg}	–65 to +150	°C
Maximum Voltage on any Pin		–	V_{IN} + 0.3 to – 0.3	V
Lead Temperature (Soldering, 10 Sec.)		–	+260	°C
ESD Withstand Voltage	Human Body Model (Note 1.)	V_{ESD}	> 2000	V
Latch–Up Performance (Note 2.)	Positive Negative	$I_{LATCH–UP}$	250 > 500	mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

1. Tested to EIA/JESD22–A114–A
2. Tested to EIA/JESD78

ELECTRICAL CHARACTERISTICS ($V_{IN} = V_{OUT} + 1.0$ V, $I_L = 100$ µA, $C_L = 3.3$ µF, $\overline{SHDN} > V_{IH}$, $T_A = 25°C$, unless otherwise noted. **Boldface** type specifications apply for junction temperatures of –40°C to +125°C.)

Characteristics	Test Conditions	Symbol	Min	Typ	Max	Unit
Input Operating Voltage	–	V_{IN}	–	–	**6.0**	V
Maximum Output Current NCP4555 NCP4586	–	I_{OUTMAX}	 **100** **150**	 – –	 – –	mA
Output Voltage	Note 3.	V_{OUT}	**V_R – 2.5%**	$V_R \pm 0.5\%$	**V_R + 2.5%**	V
V_{OUT} Temperature Coefficient	Note 4.	TCV_{OUT}	– –	20 **40**	– –	ppm/°C
Line Regulation	$(V_R + 1.0\text{ V}) \le V_{IN} \le 6.0$ V	$\Delta V_{OUT}/\Delta V_{IN}$	–	0.05	**0.35**	%
Load Regulation NCP4555 NCP4586	 I_L = 0.1 mA to I_{OUTMAX} I_L = 0.1 mA to I_{OUTMAX} Note 5.	$\Delta V_{OUT}/V_{OUT}$	 – –	 0.5 0.5	 **2.0** **3.0**	%
Dropout Voltage NCP4555, NCP4586 NCP4586	I_L = 100 µA I_L = 20 mA I_L = 50 mA I_L = 100 mA I_L = 150 mA Note 6.	$V_{IN} - V_{OUT}$	– – – – –	2.0 65 85 180 270	– – **120** **250** **400**	mV
Supply Current (Note 10.)	$\overline{SHDN} = V_{IH}$, $I_L = 0$	I_{IN}	–	50	**80**	µA
Shutdown Supply Current	$\overline{SHDN}$ = 0 V	I_{INSD}	–	0.05	**0.5**	µA
Power Supply Rejection Ratio	$F_{RE} \le 1.0$ kHz	PSRR	–	64	–	dB
Output Short Circuit Current	V_{OUT} = 0 V	I_{OUTSC}	–	300	450	mA
Thermal Regulation	Notes 7., 8.	$\Delta V_{OUT}/\Delta P_D$	–	0.04	–	V/W
Thermal Shutdown Die Temperature	–	T_{SD}	–	160	–	°C
Thermal Shutdown Hysteresis	–	ΔT_{SD}	–	10	–	°C
Output Noise	$I_L = I_{OUTMAX}$ 470 pF from Bypass to GND	eN	–	260	–	$nV/\sqrt{Hz}$

$\overline{SHDN}$ Input

$\overline{SHDN}$ Input High Threshold	V_{IN} = 2.5 V to 6.5 V	V_{IH}	45	–	–	$\%V_{IN}$
$\overline{SHDN}$ Input Low Threshold	V_{IN} = 2.5 V to 6.5 V	V_{IL}	–	–	15	$\%V_{IN}$

$\overline{ERROR}$ Output

Minimum V_{IN} Operating Voltage	–	V_{INMIN}	1.0	–	–	V
Output Logic Low Voltage	1.0 mA Flows to $\overline{ERROR}$	V_{OL}	–	–	400	mV
$\overline{ERROR}$ Threshold Voltage	See Figure 3	V_{TH}	–	0.95 x V_R	–	V
$\overline{ERROR}$ Positive Hysteresis	Note 9.	V_{HYS}	–	50	–	mV

3. V_R is the regulator output voltage setting. For example: V_R = 2.5 V, 2.7 V, 2.85 V, 3.0 V, 3.3 V, 3.6 V, 4.0 V, 5.0 V.
4. $T_C\,V_{OUT} = \dfrac{(V_{OUTMAX} - V_{OUTMIN}) \times 10^6}{V_{OUT} \times \Delta T}$
5. Regulation is measured at a constant junction temperature using low duty cycle pulse testing. Load regulation is tested over a load range from 0.1 mA to the maximum specified output current. Changes in output voltage due to heating effects are covered by the thermal regulation specification.
6. Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below its nominal value.
7. Thermal Regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, exduding load or line regulation effects. Specifications are for a current pulse equal to I_{LMAX} at V_{IN} = 6.0 V for T = 10 msec.
8. The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature, and the thermal resistance from junction–to–air (i.e. T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation causes the device to initiate thermal shutdown. Please see *Thermal Considerations* section of this data sheet for more details.
9. Hysteresis voltage is referenced by V_R.
10. Apply for Junction Temperatures of –40°C to +85°C.

PIN DESCRIPTION

Pin Number	Symbol	Description
1	V_{IN}	Unregulated supply input.
2	GND	Ground terminal.
3	$\overline{SHDN}$	Shutdown control input. The regulator is fully enabled when a logic high is applied to this input. The regulator enters shutdown when a logic low is applied to this input. During shutdown, output voltage falls to zero, $\overline{ERROR}$ is open circuited and supply current is reduced to 0.5 μA (max).
4	$\overline{ERROR}$	Out–of–Regulation Flag. (Open drain output). This output goes low when V_{OUT} is out–of–tolerance by approximately –5.0%.
5	V_{OUT}	Regulated voltage output.

DETAILED DESCRIPTION

The NCP4555 and NCP4586 are precision fixed output voltage regulators. Unlike bipolar regulators, the NCP4555 and NCP4586 supply current does not increase with load current. In addition, V_{OUT} remains stable and within regulation at very low load currents (an important consideration in RTC and CMOS RAM battery back–up applications).

Figure 2 shows a typical application circuit. The regulator is enabled any time the shutdown input ($\overline{SHDN}$) is at or above V_{IH}, and shutdown (disabled) when $\overline{SHDN}$ is at or below V_{IL}. $\overline{SHDN}$ may be controlled by a CMOS logic gate, or I/O port of a microcontroller. If the $\overline{SHDN}$ input is not required, it should be connected directly to the input supply. While in shutdown, supply current decreases to 0.05 μA (typical), V_{OUT} falls to zero volts, and $\overline{ERROR}$ is open–circuited.

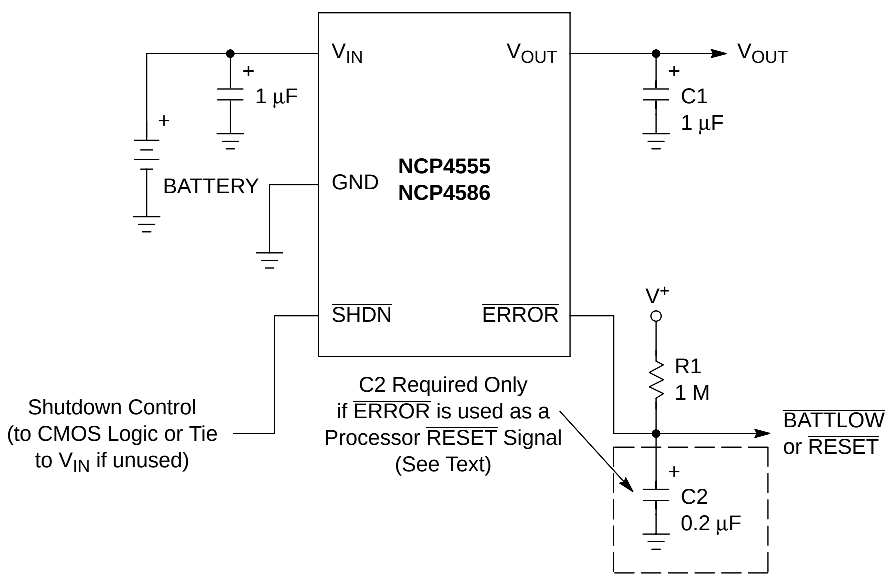


Figure 2. Typical Application Circuit

$\overline{ERROR}$ Open Drain Output

ERROR is driven low whenever V_{OUT} falls out of regulation by more than –5.0% (typical). This condition may be caused by low input voltage, output current limiting, or thermal limiting. The $\overline{ERROR}$ threshold is 5.0% below rated V_{OUT} regardless of the programmed output voltage value (e.g. $\overline{ERROR}$ = V_{OL} at 4.75 V (typ.) for a 5.0 V regulator and 2.85 V (typ.) for a 3.0 V regulator). $\overline{ERROR}$ output operation is shown in Figure 3.

Note that $\overline{ERROR}$ is active when V_{OUT} falls to V_{TH}, and inactive when V_{OUT} rises above V_{TH} by V_{HYS}.

As shown in Figure 2, $\overline{ERROR}$ can be used as a battery low flag, or as a processor $\overline{RESET}$ signal (with the addition of timing capacitor C2). R1 x C2 should be chosen to maintain $\overline{ERROR}$ below V_{IH} of the processor $\overline{RESET}$ input for at least 200 msec to allow time for the system to stabilize. Pull–up resistor R1 can be tied to V_{OUT}, V_{IN} or any other voltage less than (V_{IN} + 0.3 V).

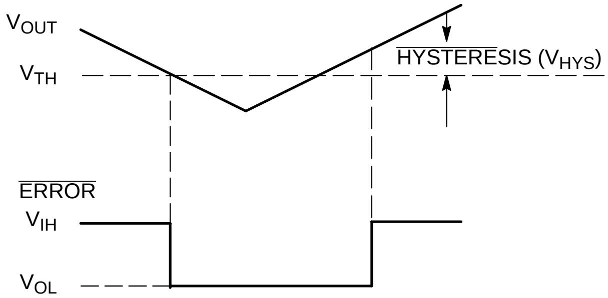


Figure 3. ERROR Output Operation

Output Capacitor

A 1.0 μF (min) capacitor from V_{OUT} to ground is recommended. The output capacitor should have an effective series resistance of 5.0 Ω or less, and a resonant frequency above 1.0 MHz. A 1.0 μF capacitor should be connected from V_{IN} to GND if there is more than 10 inches of wire between the regulator and the AC filter capacitor, or if a battery is used as the power source. Aluminum electrolytic or tantalum capacitor types can be used. (Since many aluminum electrolytic capacitors freeze at approximately –30°C, solid tantalums are recommended for applications operating below –25°C.) When operating from sources other than batteries, supply–noise rejection and transient response can be improved by increasing the value of the input and output capacitors and employing passive filtering techniques.

Thermal Considerations

Thermal Shutdown

Integrated thermal protection circuitry shuts the regulator off when die temperature exceeds 160°C. The regulator remains off until the die temperature drops to approximately 150°C.

Power Dissipation

The amount of power the regulator dissipates is primarily a function of input and output voltage, and output current. The following equation is used to calculate worst case *actual* power dissipation:

$$P_D \approx (V_{INMAX} - V_{OUTMIN}) I_{LOADMAX}$$

Where: P_D = worst case actual power dissipation
V_{INMAX} = maximum voltage on V_{IN}
V_{OUTMIN} = minimum regulator output voltage
$I_{LOADMAX}$ = maximum output (load) current

(eq. 1)

The maximum *allowable* power dissipation (Equation 2) is a function of the maximum ambient temperature (T_{AMAX}), the maximum allowable die temperature (125°C), and the thermal resistance from junction–to–air (θ_{JA}). The 5–Pin SOT–23 package has a θ_{JA} of approximately **200°C/Watt** when mounted on a single layer FR4 dielectric copper clad PC board.

$$P_{DMAX} = \frac{(T_{JMAX} - T_{AMAX})}{\theta_{JA}}$$

Where all terms are previously defined. (eq. 2)

Equation 1 can be used in conjunction with Equation 2 to ensure regulator thermal operation is within limits. For example:

GIVEN: $V_{INMAX} = 3.0\ V \pm 5.0\%$
$V_{OUTMIN} = 2.7\ V - 2.5\%$
$I_{LOAD} = 40\ mA$
$T_{AMAX} = 55°C$

FIND: 1. Actual power dissipation.
2. Maximum allowable dissipation.

Actual power dissipation:

$$P_D \approx (V_{INMAX} - V_{OUTMIN}) I_{LOADMAX}$$
$$= [(3.0 \times 1.05) - (2.7 \times .975)]\ 40 \times 10^{-3}$$
$$= \underline{20.7\ mW}$$

Maximum allowable power dissipation:

$$P_{DMAX} = \frac{(T_{JMAX} - T_{AMAX})}{\theta_{JA}}$$
$$= \frac{(125 - 55)}{220}$$
$$= \underline{318\ mW}$$

In this example, the NCP4555 dissipates a maximum of only 20.7 mW; far below the allowable limit of 318 mW. In a similar manner, Equation 1 and Equation 2 can be used to calculate maximum current and/or input voltage limits.

Layout Considerations

The primary path of heat conduction out of the package is via the package leads. Therefore, layouts having a ground plane, wide traces at the pads, and wide power supply bus lines combine to lower θ_{JA} and, therefore, increase the maximum allowable power dissipation limit.

TYPICAL CHARACTERISTICS

(Unless otherwise specified, all parts are measured at Temperature = 25°C)

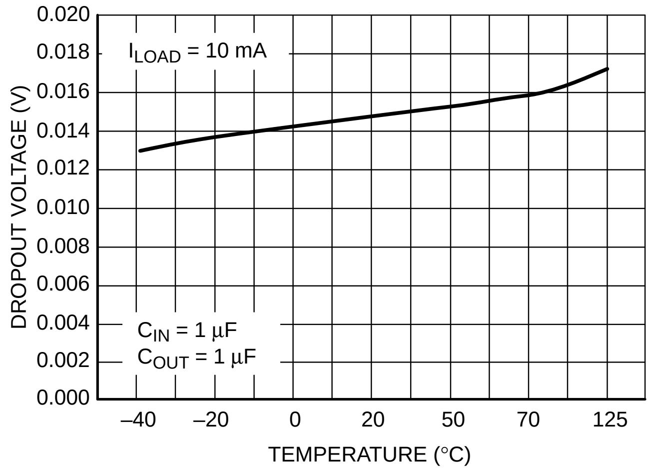


Figure 4. Dropout Voltage vs. Temperature (V_{OUT} = 3.3 V)

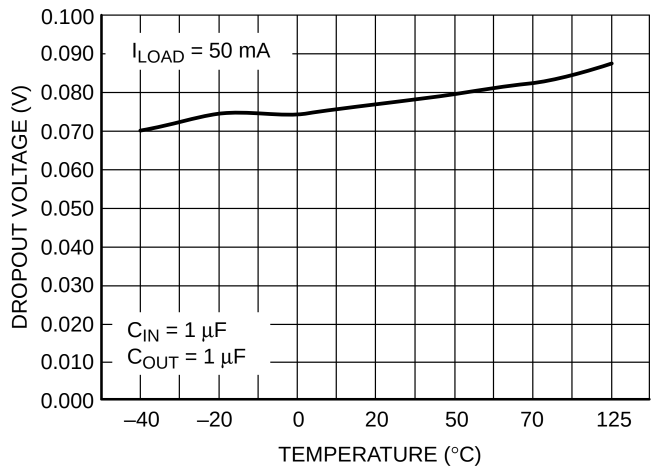


Figure 5. Dropout Voltage vs. Temperature (V_{OUT} = 3.3 V)

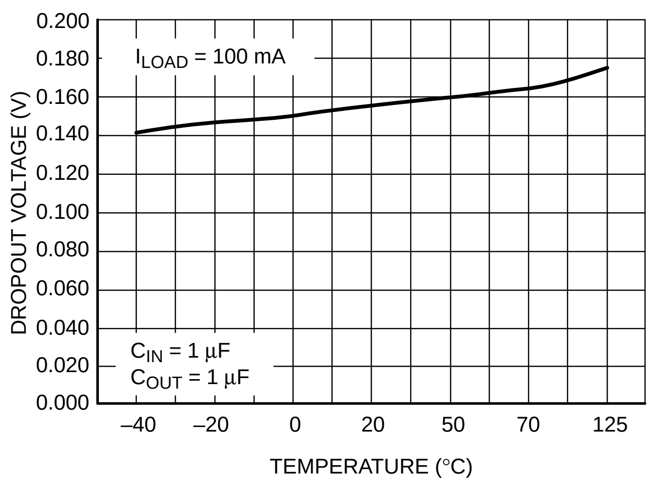


Figure 6. Dropout Voltage vs. Temperature (V_{OUT} = 3.3 V)

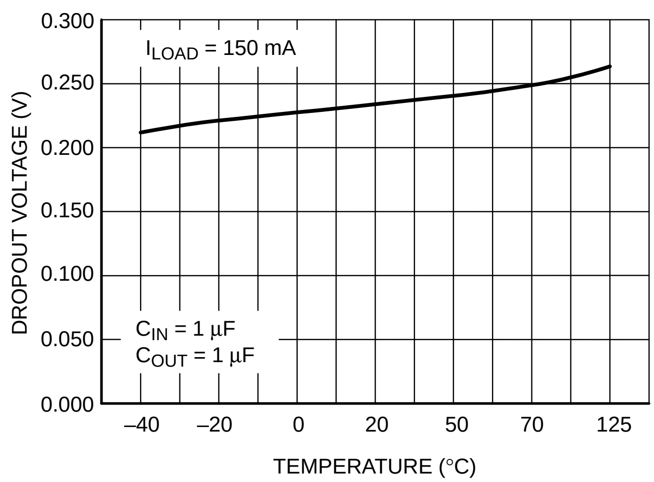


Figure 7. Dropout Voltage vs. Temperature (V_{OUT} = 3.3 V)

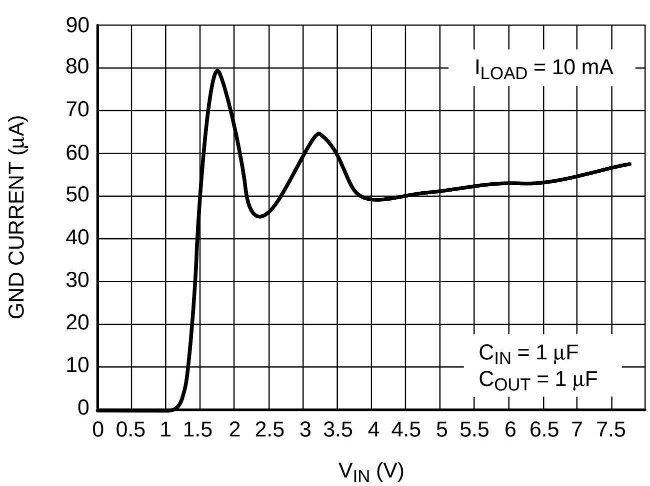


Figure 8. Ground Current vs. V_{IN} (V_{OUT} = 3.3 V)

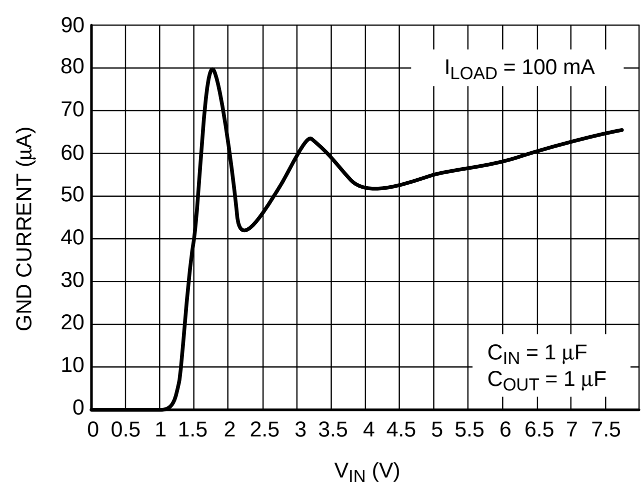


Figure 9. Ground Current vs. V_{IN} (V_{OUT} = 3.3 V)

TYPICAL CHARACTERISTICS

(Unless otherwise specified, all parts are measured at Temperature = 25°C)

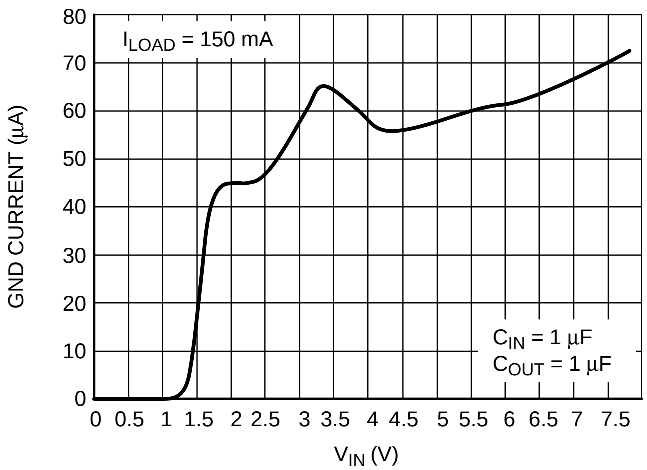


Figure 10. Ground Current vs. V_{IN} (V_{OUT} = 3.3 V)

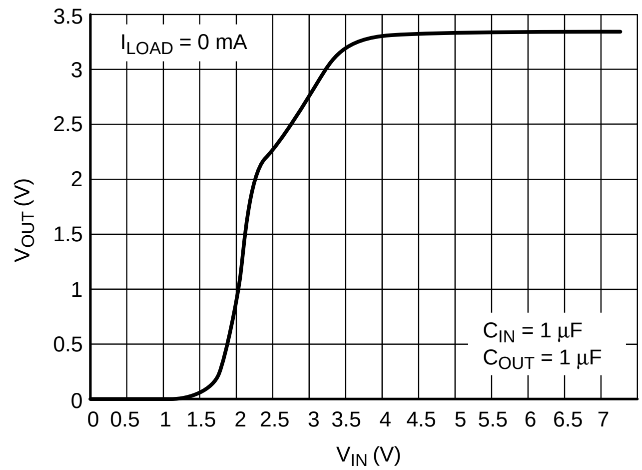


Figure 11. V_{OUT} vs. V_{IN} (V_{OUT} = 3.3 V)

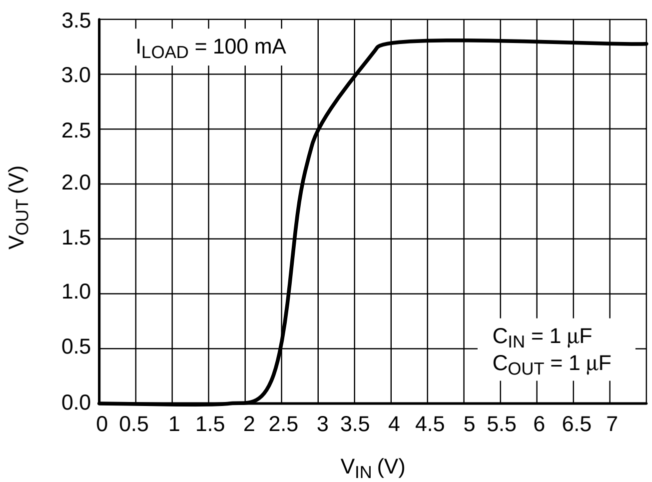


Figure 12. V_{OUT} vs. V_{IN} (V_{OUT} = 3.3 V)

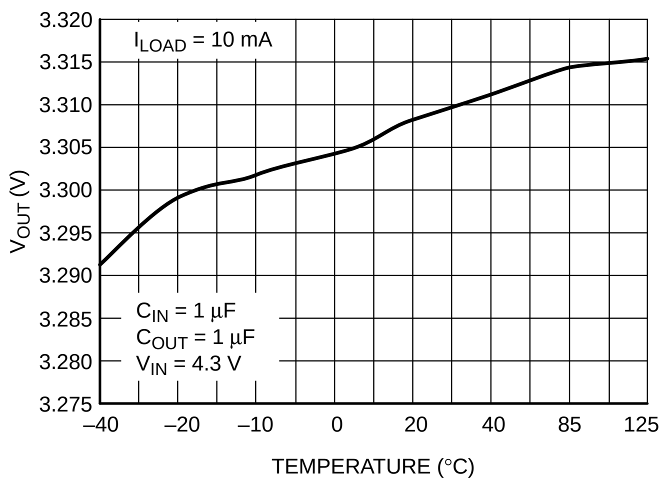


Figure 13. Output Voltage vs. Temperature (V_{OUT} = 3.3 V)

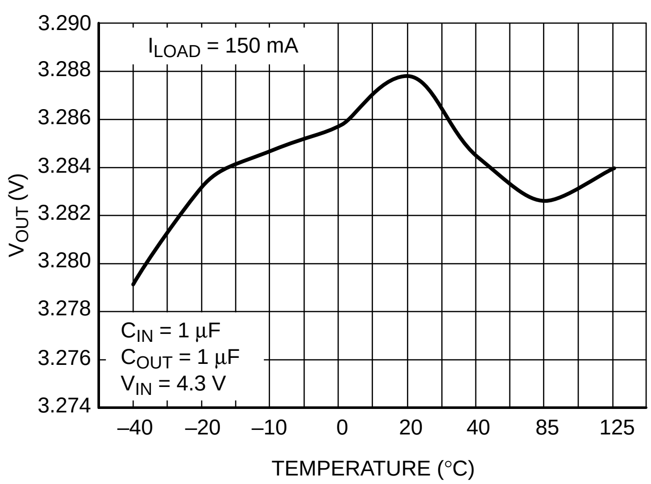


Figure 14. Output Voltage vs. Temperature (V_{OUT} = 3.3 V)

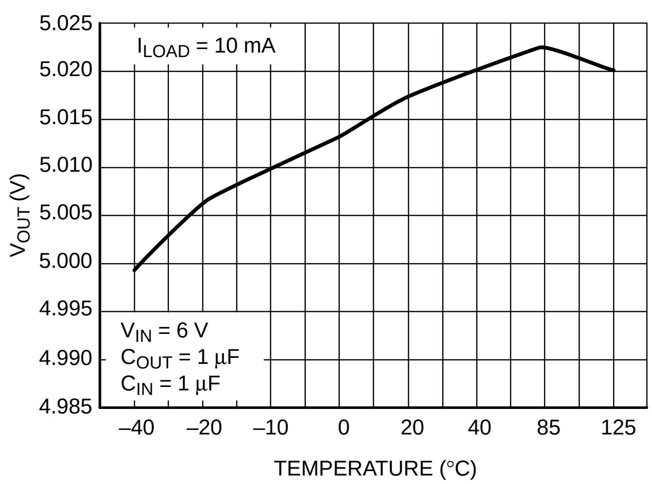


Figure 15. Output Voltage vs. Temperature (V_{OUT} = 5 V)

TYPICAL CHARACTERISTICS

(Unless otherwise specified, all parts are measured at Temperature = 25°C)

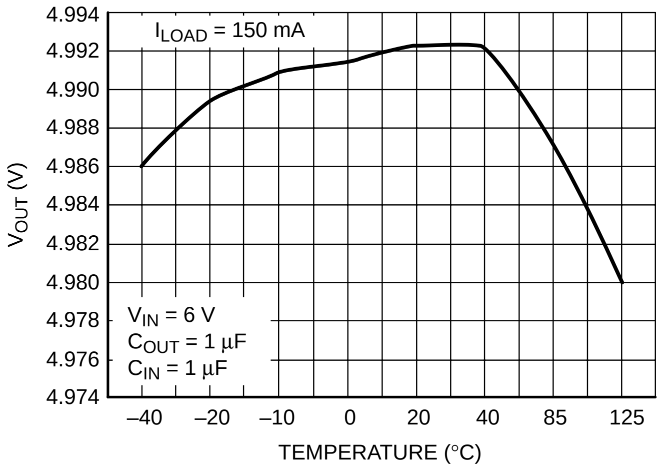


Figure 16. Output Voltage vs. Temperature (V_{OUT} = 5 V)

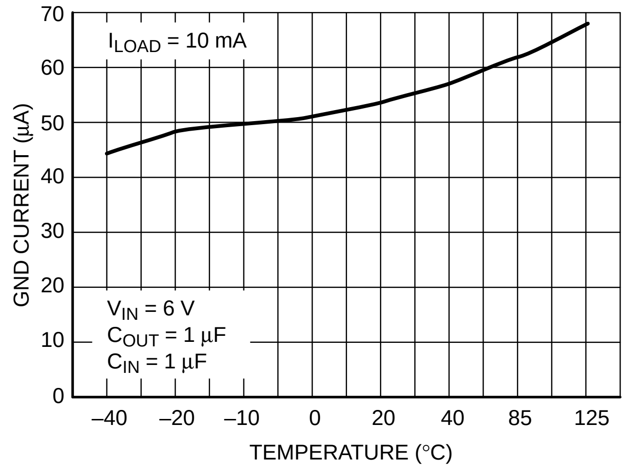


Figure 17. Temperature vs. Quiescent Current (V_{OUT} = 5 V)

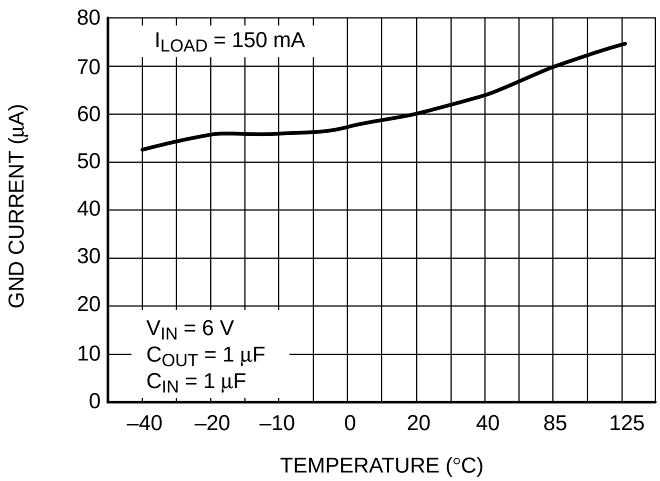


Figure 18. Temperature vs. Quiescent Current (V_{OUT} = 5 V)

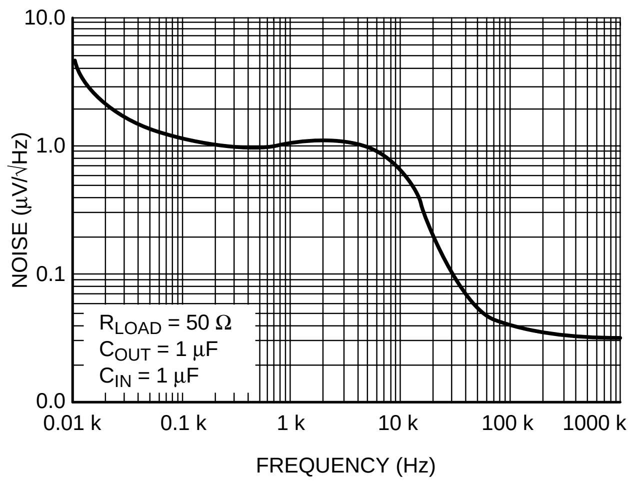


Figure 19. Output Noise vs. Frequency

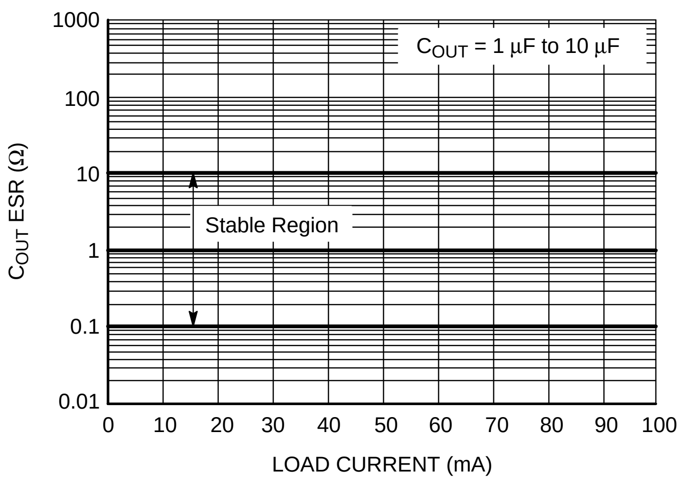


Figure 20. Stability Region vs. Load Current

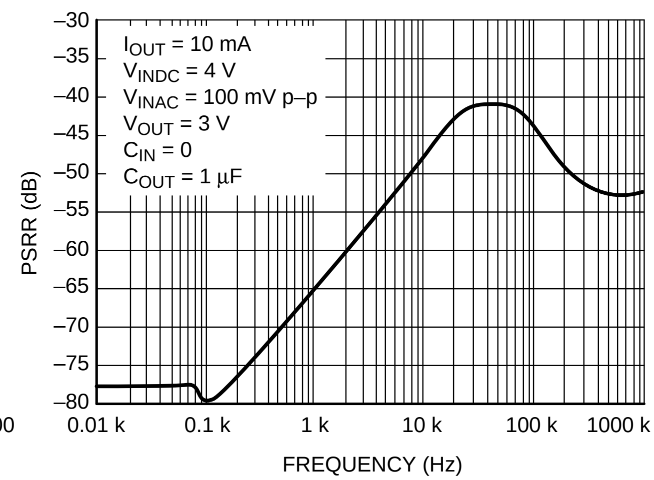
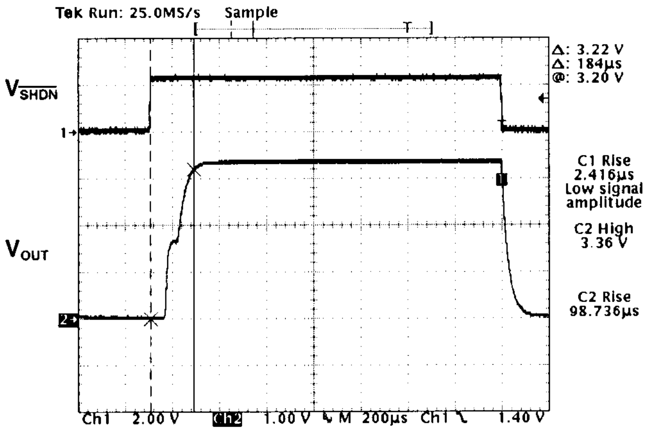
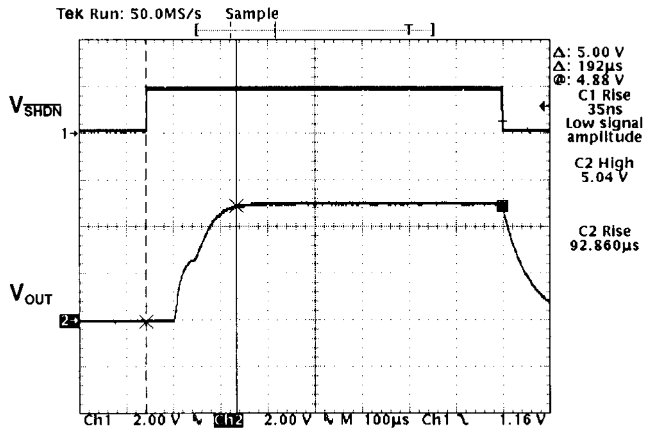


Figure 21. Power Supply Rejection Ratio



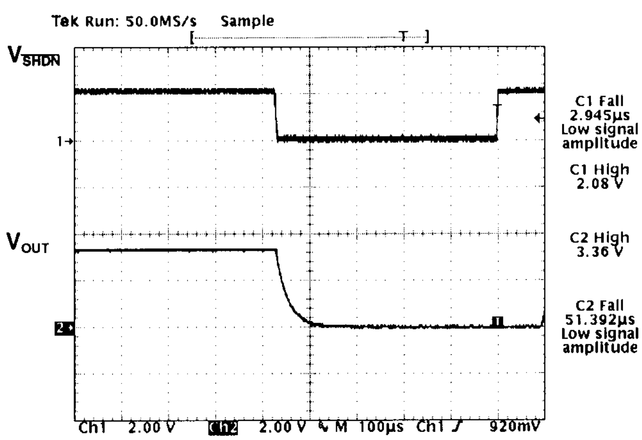
Conditions:
C_{IN} = 1 µF, C_{OUT} = 1 µF, I_{LOAD} = 100 mA,
V_{IN} = 4.3 V, Temp = 25°C, Rise Time = 184 µS

Figure 22. Measure Rise Time of 3.3 V LDO



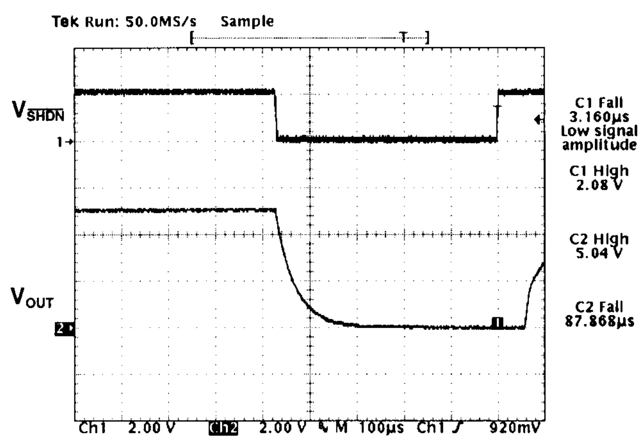
Conditions:
C_{IN} = 1 µF, C_{OUT} = 1 µF, I_{LOAD} = 100 mA
V_{IN} = 6 V, Temp = 25°C, Rise Time = 192 µS

Figure 23. Measure Rise Time of 5.0 V LDO



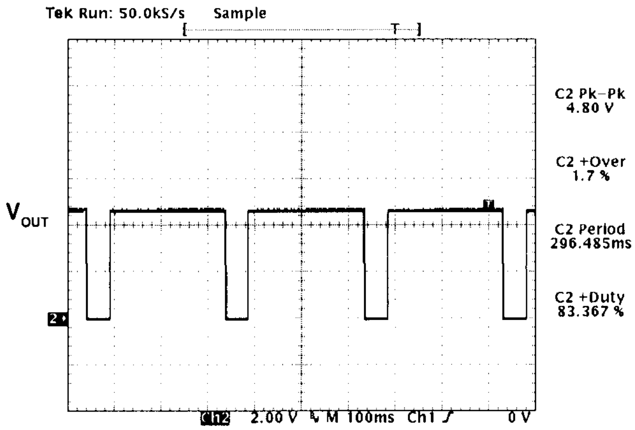
Conditions:
C_{IN} = 1 µF, C_{OUT} = 1 µF, I_{LOAD} = 100 mA
V_{IN} = 4.3 V, Temp = 25°C, Fall Time = 52 µS

Figure 24. Measure Fall Time of 3.3 V LDO



Conditions:
C_{IN} = 1 µF, C_{OUT} = 1 µF, I_{LOAD} = 100 mA
V_{IN} = 6 V, Temp = 25°C, Fall Time = 88 µS

Figure 25. Measure Fall Time of 5.0 V LDO

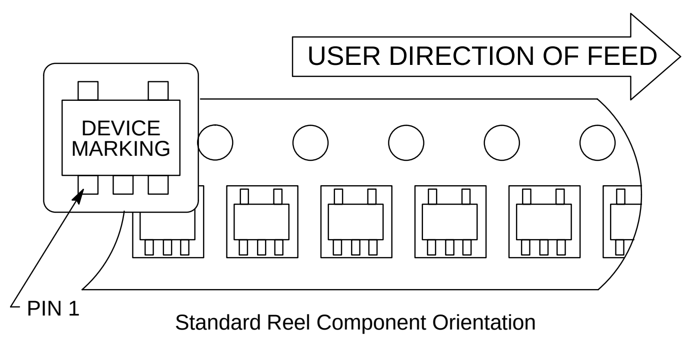


Conditions:
V_{IN} = 6 V, C_{IN} = 0 μF, C_{OUT} = 1 μF

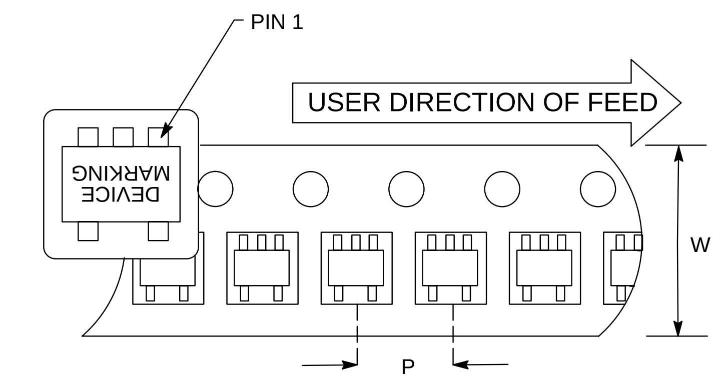
Figure 26. Thermal Shutdown Response of 5.0 V LDO

I_{LOAD} was increased until temperature of die reached about 160°C, at which time integrated thermal protection circuitry shuts the regulator off when die temperature exceeds approximately 160°C. The regulator remains off until die temperature drops to approximately 150°C.

Component Taping Orientation for 5–Pin SOT–23 Devices



Standard Reel Component Orientation
TR Suffix Device
(Mark Right Side Up)

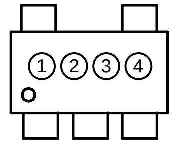


Reverse Reel Component Orientation
RT Suffix Device
(Mark Upside Down)

Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
SOT–23	8 mm	4 mm	3000	7 inches

MARKING DIAGRAM



(1) and (2) = Two Letter Part Number Codes + Temperature Range and Voltage

(3) = Year and Quarter Code

(4) = Lot ID Number

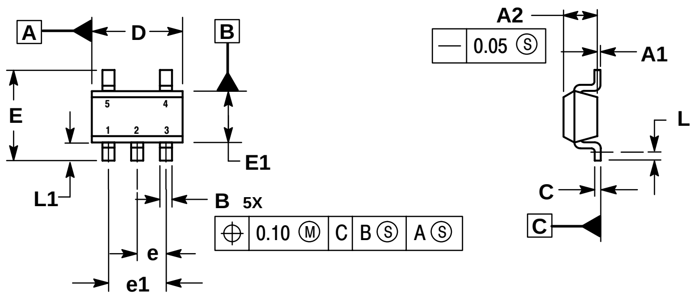
ORDERING INFORMATION

Device	Voltage Option*	Marking (1) and (2)	Package	Junction Temperature Range	Shipping
NCP4555SNxxT1	1.8	DY	SOT–23	–40°C to + 125°C	3000 Tape & Reel
	2.8	DZ			
	2.85	D8			
	3.0	D3			
	3.3	D5			
NCP4586SNxxT1	2.5	P1			
	2.7	P2			
	2.8	PZ			
	2.85	P8			
	3.0	P3			
	3.3	P5			
	3.6	P9			
	4.0	P0			
	5.0	P7			

xx Indicates Output Voltages
*Other output voltages are available. Please contact ON Semiconductor for details.

PACKAGE DIMENSIONS

SOT–23
SN SUFFIX
CASE 1212–01
ISSUE O



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM C IS A SEATING PLANE.

	MILLIMETERS	
DIM	MIN	MAX
A1	0.00	0.10
A2	1.00	1.30
B	0.30	0.50
C	0.10	0.25
D	2.80	3.00
E	2.50	3.10
E1	1.50	1.80
e	0.95 BSC	
e1	1.90 BSC	
L	0.20	---
L1	0.45	0.75

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JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031
Phone: 81–3–5740–2700
Email: r14525@onsemi.com

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