

# MC74LVX257

## Quad 2-Channel Multiplexer with 3-State Outputs

The MC74LVX257 is an advanced high speed CMOS quad 2-channel multiplexer fabricated with silicon gate CMOS technology.

It consists of four 2-input digital multiplexers with common select (S) and enable ( $\overline{OE}$ ) inputs. When ( $\overline{OE}$ ) is held High, selection of data is inhibited and all the outputs go Low.

The select decoding determines whether the A or B inputs get routed to the corresponding Y outputs.

The inputs tolerate voltages up to 7 V, allowing the interface of 5 V systems to 3 V systems.

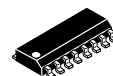
- High Speed:  $t_{PD} = 4.5$  ns (Typ) at  $V_{CC} = 3.3$  V
- Low Power Dissipation:  $I_{CC} = 4$   $\mu$ A (Max) at  $T_A = 25^\circ$ C
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\%$   $V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 5.5 V Operating Range
- Low Noise:  $V_{OLP} = 0.8$  V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: FETs = 100; Equivalent Gates = 25



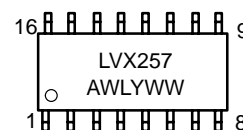
**ON Semiconductor**

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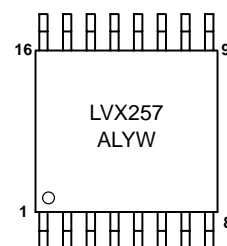
### MARKING DIAGRAMS



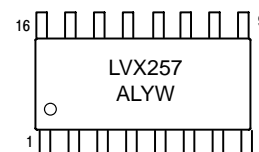
**SO-16**  
**D SUFFIX**  
**CASE 751B**



**TSSOP-16**  
**DT SUFFIX**  
**CASE 948F**



**EIAJ SO-16**  
**M SUFFIX**  
**CASE 966**



A = Assembly Location  
L, WL = Wafer Lot  
Y = Year  
W, WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC74LVX257D	SO-16	48 Units/Rail
MC74LVX257DR2	SO-16	2500 Tape & Reel
MC74LVX257DT	TSSOP-16	96 Units/Rail
MC74LVX257DTR2	TSSOP-16	2500 Tape & Reel
MC74LVX257M	EIAJ SO-16	50 Units/Rail
MC74LVX257MEL	EIAJ SO-16	2000 Tape & Reel

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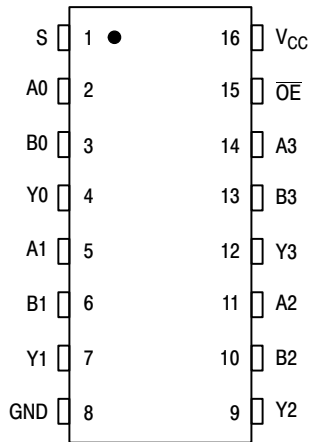


Figure 1. Pin Assignment

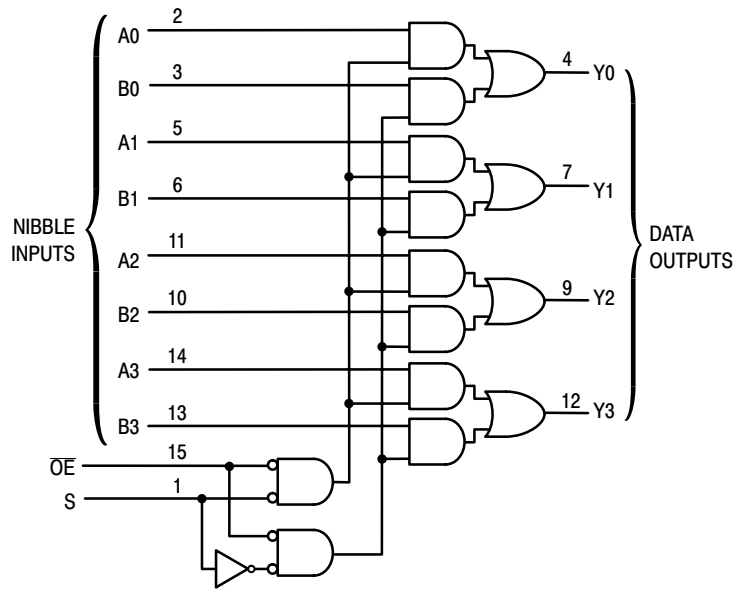


Figure 2. Expanded Logic Diagram

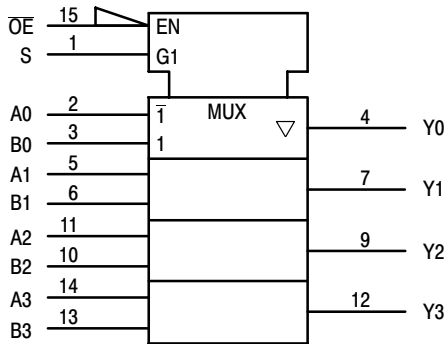


Figure 3. IEC Logic Symbol

## FUNCTION TABLE

Inputs		Outputs Y0 – Y3
$\overline{OE}$	S	
H	X	L
L	L	A0–A3
L	H	B0–B3

A0 – A3, B0 – B3 = the levels of the respective Data-Word Inputs.

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This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ .  
 Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ).  
 Unused outputs must be left open.

## MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Value	Unit
$V_{CC}$	Positive DC Supply Voltage	-0.5 to +7.0	V
$V_{IN}$	Digital Input Voltage	-0.5 to +7.0	V
$V_{OUT}$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	Input Diode Current	-20	mA
$I_{OK}$	Output Diode Current	$\pm 20$	mA
$I_{OUT}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 75$	mA
$P_D$	Power Dissipation in Still Air	SOIC Package 200 TSSOP 180	mW
$T_{STG}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
$V_{ESD}$	ESD Withstand Voltage	Human Body Model (Note 2.) >2000 Machine Model (Note 3.) >200 Charged Device Model (Note 4.) >2000	V
$I_{LATCH-UP}$	Latch-Up Performance	Above $V_{CC}$ and Below GND at 125 $^{\circ}C$ (Note 5.)	$\pm 300$ mA
$\theta_{JA}$	Thermal Resistance, Junction to Ambient	SOIC Package 143 TSSOP 164	$^{\circ}C/W$

1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
2. Tested to EIA/JESD22-A114-A
3. Tested to EIA/JESD22-A115-A
4. Tested to JESD22-C101-A
5. Tested to EIA/JESD78

## RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
$V_{CC}$	DC Supply Voltage	2.0	3.6	V
$V_{IN}$	DC Input Voltage	0	5.5	V
$V_{OUT}$	DC Output Voltage	0	$V_{CC}$	V
$T_A$	Operating Temperature Range, all Package Types	-40	85	$^{\circ}C$
$t_r, t_f$	Input Rise or Fall Time			ns/V
	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0	100	

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## DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			-40°C ≤ T <sub>A</sub> ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	Minimum High-Level Input Voltage		2.0 3.0 3.6	0.75 V <sub>CC</sub> 0.7 V <sub>CC</sub> 0.7 V <sub>CC</sub>			0.75 V <sub>CC</sub> 0.7 V <sub>CC</sub> 0.7 V <sub>CC</sub>		V
V <sub>IL</sub>	Maximum Low-Level Input Voltage		2.0 3.0 3.6			0.25 V <sub>CC</sub> 0.3 V <sub>CC</sub> 0.3 V <sub>CC</sub>		0.25 V <sub>CC</sub> 0.3 V <sub>CC</sub> 0.3 V <sub>CC</sub>	V
V <sub>OH</sub>	High-Level Output Voltage	I <sub>OH</sub> = -50 μA I <sub>OH</sub> = -50 μA I <sub>OH</sub> = -4 mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V <sub>OL</sub>	Low-Level Output Voltage	I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 4 mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I <sub>OZ</sub>	Maximum 3-State Leakage Current	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND	3.6			±0.1		±1.0	μA
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = 5.5 V or GND	0 to 3.6			±0.1		±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per package)	V <sub>IN</sub> = V <sub>CC</sub> or GND	3.6	1.0	1.0	2.0			μA

## AC ELECTRICAL CHARACTERISTICS Input t<sub>r</sub> = t<sub>f</sub> = 3.0 ns

Symbol	Parameter	Test Conditions	T <sub>A</sub> = 25°C			-40°C ≤ T <sub>A</sub> ≤ 85°C		Unit
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, A or B to Y	V <sub>CC</sub> = 2.7 V    C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF		6.5 9.5	10.0 14.0	1.0 1.0	15.0 18.5	ns
		V <sub>CC</sub> = 3.3 V ± 0.3 V    C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF		4.5 7.5	8.0 12.0	1.0 1.0	10.0 13.5	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, S to Y	V <sub>CC</sub> = 2.7 V    C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF		8.0 10.5	12.0 15.5	1.0 1.0	17.0 20.0	ns
		V <sub>CC</sub> = 3.3 V ± 0.3 V    C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF		6.0 8.5	10.0 13.5	1.0 1.0	12.0 15.5	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Output Enable, Time, OE to Y	V <sub>CC</sub> = 2.7 V    C <sub>L</sub> = 15pF R <sub>L</sub> = 1 kΩ    C <sub>L</sub> = 50pF		7.5 10.5	11.5 15.0	1.0 1.0	16.5 18.0	ns
		V <sub>CC</sub> = 3.3 V ± 0.3 V    C <sub>L</sub> = 15pF R <sub>L</sub> = 1 kΩ    C <sub>L</sub> = 50pF		5.5 8.5	9.5 13.0	1.0 1.0	11.5 15.0	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Output Disable, Time, OE to Y	V <sub>CC</sub> = 2.7 V    C <sub>L</sub> = 50pF R <sub>L</sub> = 1 kΩ		13.0	17.0	1.0	18.0	ns
		V <sub>CC</sub> = 3.3 V ± 0.3 V    C <sub>L</sub> = 50pF R <sub>L</sub> = 1 kΩ		12	17.0	1.0	18.0	
C <sub>IN</sub>	Maximum Input Capacitance			4	10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 6.)	Typical @ 25°C, V <sub>CC</sub> = 3.3 V						pF
		20						

6. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>. C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

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**NOISE CHARACTERISTICS** Input  $t_r = t_f = 3.0$  ns,  $C_L = 50$  pF,  $V_{CC} = 3.3$  V

Symbol	Characteristic	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
$V_{OLP}$	Quiet Output Maximum Dynamic $V_{OL}$	0.3	0.5	V
$V_{OLV}$	Quiet Output Minimum Dynamic $V_{OL}$	-0.3	-0.5	V
$V_{IHD}$	Minimum High Level Dynamic Input Voltage		2.0	V
$V_{ILD}$	Maximum Low Level Dynamic Input Voltage		0.8	V

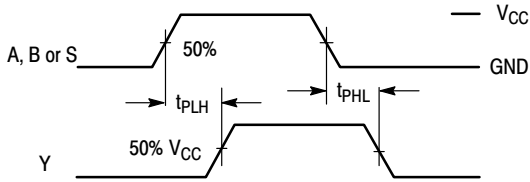


Figure 4. Switching Waveform

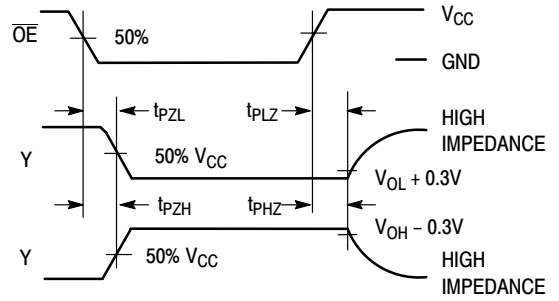
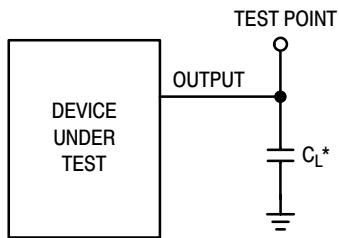
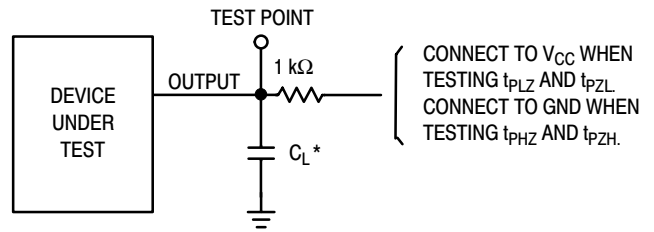


Figure 5. Switching Waveform



\*Includes all probe and jig capacitance

Figure 6. Test Circuit



\*Includes all probe and jig capacitance

Figure 7. Test Circuit

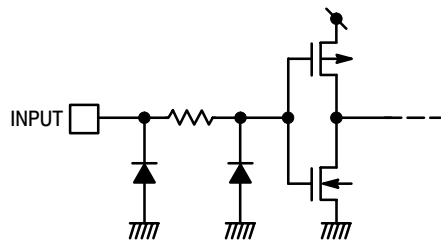
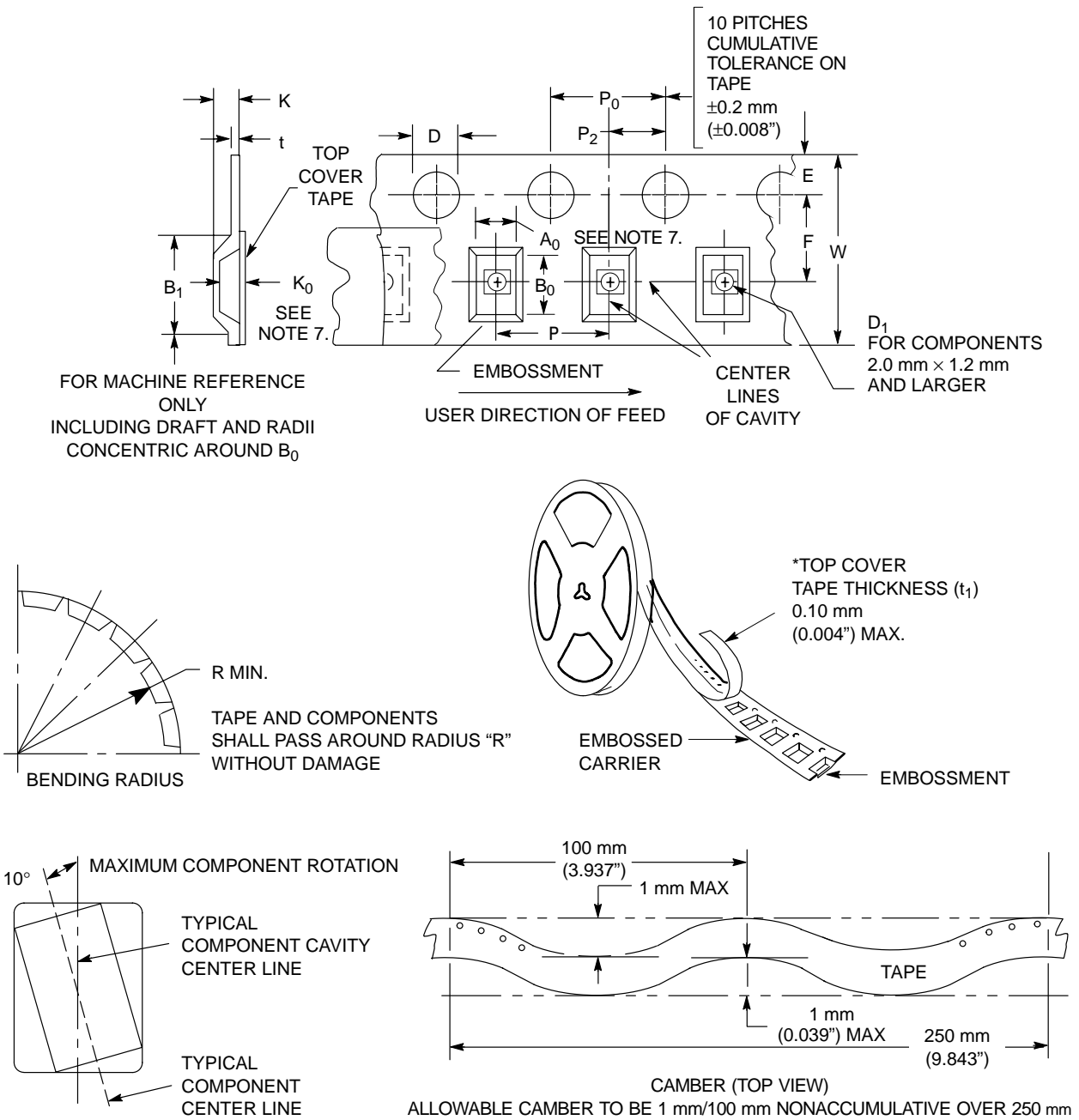


Figure 8. Input Equivalent Circuit

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7.  $A_0$ ,  $B_0$ , and  $K_0$  are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

**Figure 9. Carrier Tape Specifications**

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## EMBOSSED CARRIER DIMENSIONS (See Notes 8. and 9.)

Tape Size	B <sub>1</sub> Max	D	D <sub>1</sub>	E	F	K	P	P <sub>0</sub>	P <sub>2</sub>	R	T	W
8 mm	4.35 mm (0.179")	1.5 mm + 0.1 -0.0 (0.059" +0.004 -0.0)	1.0 mm Min (0.179")	1.75 mm ±0.1 (0.069 ±0.004")	3.5 mm ±0.5 (1.38 ±0.002")	2.4 mm Max (0.094")	4.0 mm ±0.10 (0.157 ±0.004")	4.0 mm ±0.1 (0.157 ±0.004")	2.0 mm ±0.1 (0.079 ±0.004")	25 mm (0.98")	0.6 mm (0.024)	8.3 mm (0.327)
12 mm	8.2 mm (0.323")		1.5 mm Min (0.060)		5.5 mm ±0.5 (0.217 ±0.002")	6.4 mm Max (0.252")	4.0 mm ±0.10 (0.157 ±0.004") 8.0 mm ±0.10 (0.315 ±0.004")			30 mm (1.18")		12.0 mm ±0.3 (0.470 ±0.012")
16 mm	12.1 mm (0.476")				7.5 mm ±0.10 (0.295 ±0.004")	7.9 mm Max (0.311")	4.0 mm ±0.10 (0.157 ±0.004") 8.0 mm ±0.10 (0.315 ±0.004") 12.0 mm ±0.10 (0.472 ±0.004")					16.3 mm (0.642)
24 mm	20.1 mm (0.791")				11.5 mm ±0.10 (0.453 ±0.004")	11.9 mm Max (0.468")	16.0 mm ±0.10 (0.63 ±0.004")					24.3 mm (0.957)

8. Metric Dimensions Govern—English are in parentheses for reference only.

9. A<sub>0</sub>, B<sub>0</sub>, and K<sub>0</sub> are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

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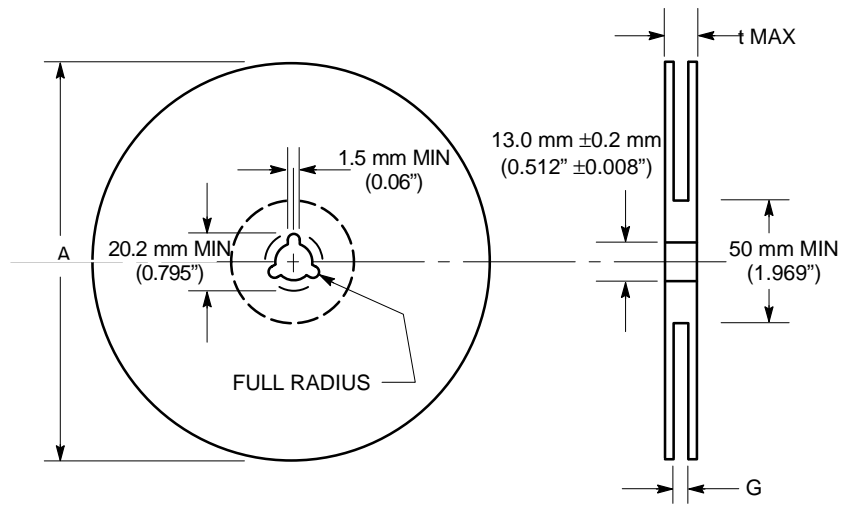


Figure 10. Reel Dimensions

## REEL DIMENSIONS

Tape Size	T&R Suffix	A Max	G	t Max
8 mm	T1, T2	178 mm (7")	8.4 mm, +1.5 mm, -0.0 (0.33" + 0.059", -0.00)	14.4 mm (0.56")
8 mm	T3, T4	330 mm (13")	8.4 mm, +1.5 mm, -0.0 (0.33" + 0.059", -0.00)	14.4 mm (0.56")
12 mm	R2	330 mm (13")	12.4 mm, +2.0 mm, -0.0 (0.49" + 0.079", -0.00)	18.4 mm (0.72")
16 mm	R2	360 mm (14.173")	16.4 mm, +2.0 mm, -0.0 (0.646" + 0.078", -0.00)	22.4 mm (0.882")
24 mm	R2	360 mm (14.173")	24.4 mm, +2.0 mm, -0.0 (0.961" + 0.078", -0.00)	30.4 mm (1.197")

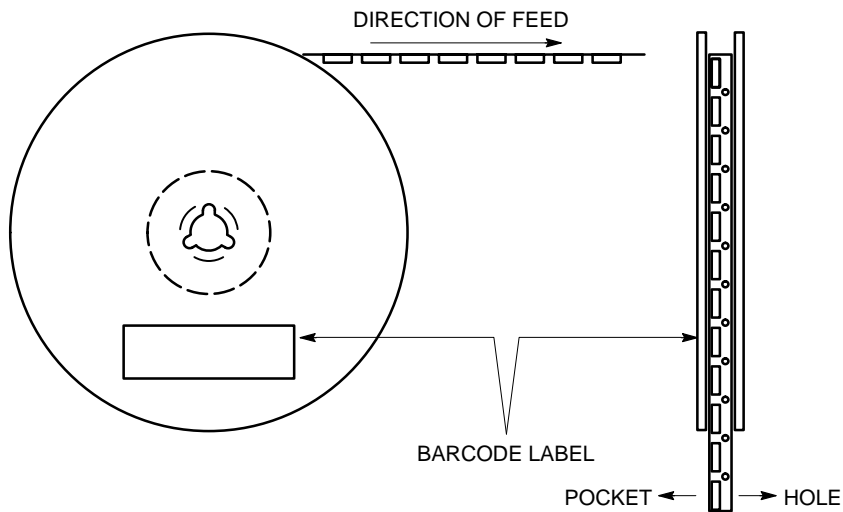
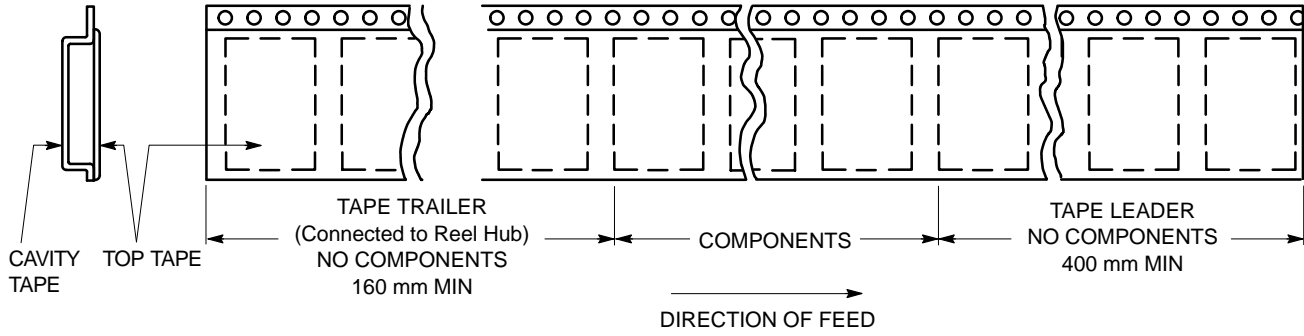


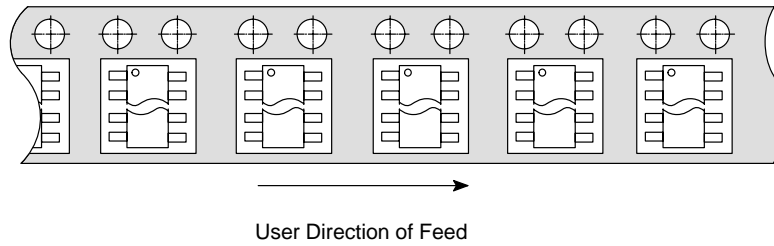
Figure 11. Reel Winding Direction



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**Figure 12. Tape Ends for Finished Goods**



**Figure 13. TSSOP and SOIC R2 Reel Configuration/Orientation**

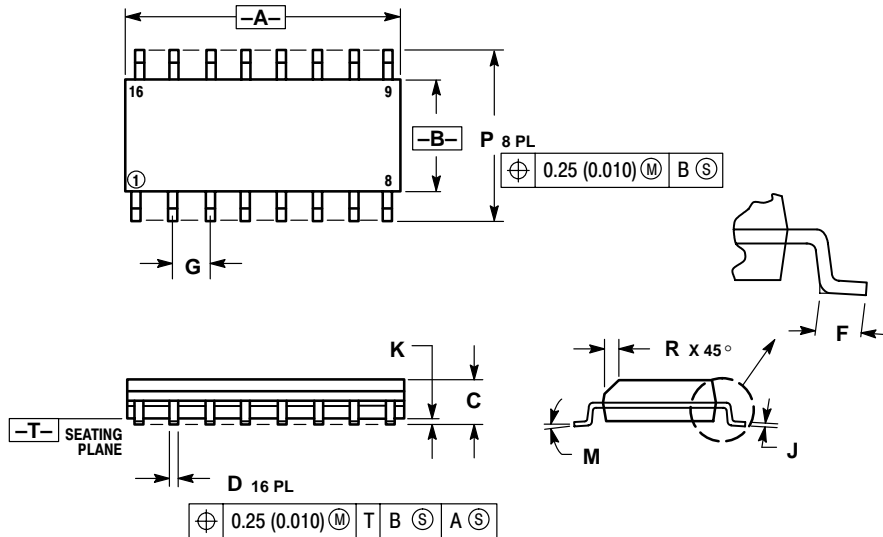
## TAPE UTILIZATION BY PACKAGE

Tape Size	SOIC	TSSOP	QFN	SC88A / SOT-353 SC88/SOT-363
8 mm				5-, 6-Lead
12 mm	8-Lead	8-, 14-, 16-Lead	8-, 14-, 16-Lead	
16 mm	14-, 16-Lead	20-, 24-Lead	20-, 24-Lead	
24 mm	18-, 20-, 24-, 28-Lead	48-, 56-Lead	48-, 56-Lead	

# MC74LVX257

## PACKAGE DIMENSIONS

SOIC-16  
D SUFFIX  
CASE 751B-05  
ISSUE J

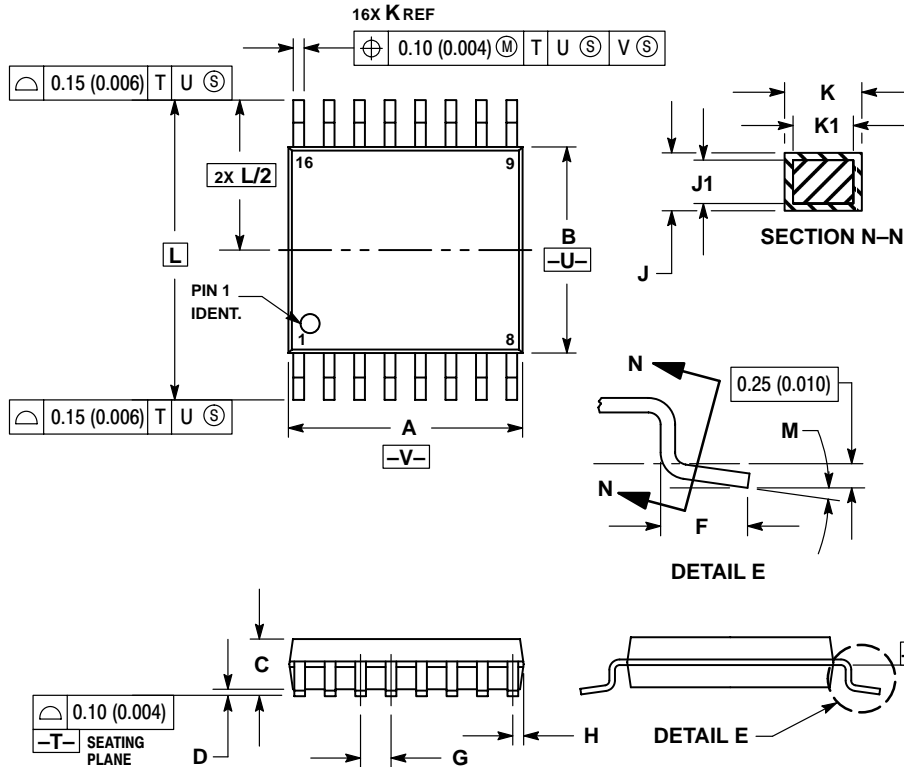


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

TSSOP-16  
DT SUFFIX  
CASE 948F-01  
ISSUE O



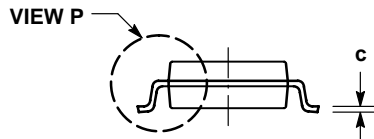
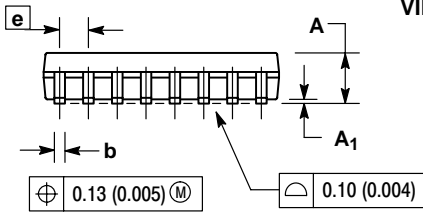
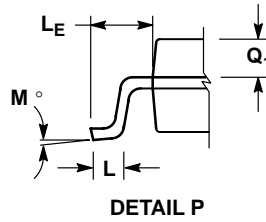
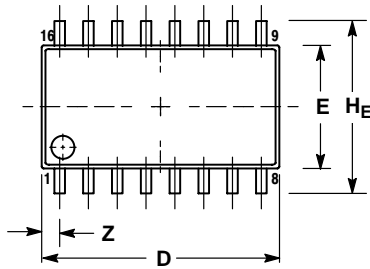
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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SOIC EIAJ-16  
M SUFFIX  
CASE 966-01  
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H <sub>E</sub>	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L <sub>E</sub>	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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