HARRIS

HY-9574

ADVANCED

Sampling 12 Bit A/D Converter with 8/16 Bit μP Interface

Features

- Complete 12 Bit Sampling A/D Converter with Reference and Clock
- Throughput Rate (Typical) 48kHz
- 32 Pin Plastic Dual-In-Line Package

A/D Converter Features

- Full 8-, 12- or 16 Bit Microprocessor Bus Interface
- 150ns Bus Access Time
- No Missing Codes Over Temperature
- Minimal Setup Time for Control Signals
- 25μs Maximum Conversion Time
- Low Noise, via Current-Mode Signal Transmission Between Chips
- Byte Enable/Short Cycle (Ao Input)

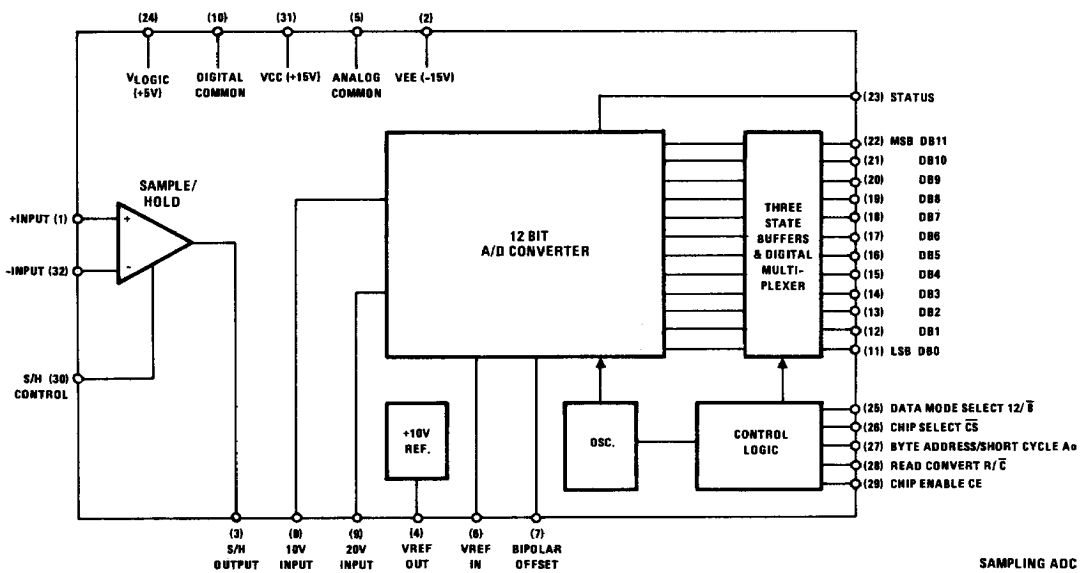
Applications

- Precision Industrial Data Acquisition Systems
- Electronic Test and Scientific Instrumentation
- Process Control Systems
- Peak Detectors

Sample/Hold Features

- Gain DC ..... $2x10^6$ V/V
- Acquisition Time ..... 1.0μs (±0.01%)
- Droop Rate ..... 0.08μV/μs (25°C)
  2.4μV/μs (Full Temp.)
- Aperture Time 25ns
- Pedestal Error 1.0mV
- Internal Hold Capacitor
- Fully Differential Input
- TTL Compatible

Functional Diagram



Description

The HY-9574 is designed for use in precision, high speed data acquisition systems. The Harris Sample/Hold amplifier (HA-5320) and 12 bit A/D converter (HI-574A) have been combined in a single package to reduce package count and to insure component compatibility.

The Sample/Hold (HA-5320) circuit consists of an input transconductance amplifier capable of providing large amounts of charging current, a low leakage analog switch, and an output integrating amplifier. The analog switch sees virtual ground as its load; therefore, charge injection on the hold capacitor is constant over the entire input/output voltage range. The device includes a hold capacitor, so no external hold capacitor is required.

The Sample and Hold chip (HA-5320) is manufactured using the Harris Dielectric Isolation process, which minimizes stray capacitance and eliminates SCR's. This allows higher speed and latch-free operation.

The 12 bit successive approximation Analog-to-Digital section is an HA-574A chip set. It includes a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up.

Custom design of each IC (Bipolar Analog and CMOS Digital) has yielded improved versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current-controlled for excellent stability over temperature. The oscillator is trimmed for a nominal conversion time of 20 $\pm$ 1μs.

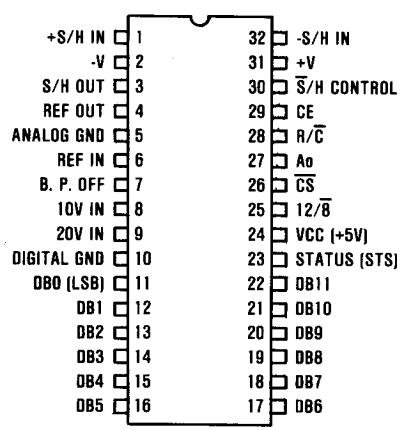
The Sample/Hold and ADC stages are not connected internally to provide maximum flexibility to the designer.

The HY-9574 offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The buried zener reference circuit is trimmed for minimum temperature coefficient.

Power requirements are $\pm$15V and +5V, with typical dissipation of 850mW. All models are packaged in a 32 pin plastic DIP with 600 mil row centers.

Pinout

TOP VIEW



Absolute Maximum Ratings

V_{CC} to Digital Common ..... 0 to +16.5V
V_{EE} to Digital Common ..... 0 to -16.5V
V_{Logic} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±1V
Digital Inputs (CE, CS, A_0, 12/8, R/C, S/H)
to Digital Common ..... -0.5V to V_{Logic} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$ +IN, -IN)
to Analog Common ..... ±16.5V
$20V_{IN}$ to Analog Common ..... ±24V

REF OUT ..... Indefinite Short to Common, Momentary Short to V_{CC}
S/H Differential Input Voltage ..... ±24V
S/H Output Current, Continuous ..... ±20mA
Storage Temperature ..... -65°C to +150°C
Power Dissipation * 2560mW
Lead Temperature, Soldering ..... 180°C
Thermal Resistance, θja ..... 39°C/W
θjc ..... 14°C/W

*Derate 25.6mW/°C above 75°C

	MIN	TYP	MAX	UNITS
Maximum Offset Error			±3	LSB
Maximum Sampling Rate (Note 1)			37	kHz
POWER SUPPLY REJECTION				
Maximum change in full scale calibration				
+15V ±0.5V J and A models			±2	LSB
All Other Models			±1	LSB
-15V ±0.5V J and A Models			±3	LSB
All Other Models			±2	LSB
+5V ±0.5V All Models			±½	LSB
POWER SUPPLIES				
Operating Voltages				
V_{Logic}	4.5	5.0	5.5	Volts
V_{CC}	14.5	15.0	16.0	Volts
V_{EE}	-14.5	-15.0	-16.0	Volts
Operating Currents				
I_{Logic}		7	15	mA
I_{CC} (Note 3)		22	28	mA
I_{EE} (Note 3)		32	41	mA

(In configuration as shown in Figure 1)

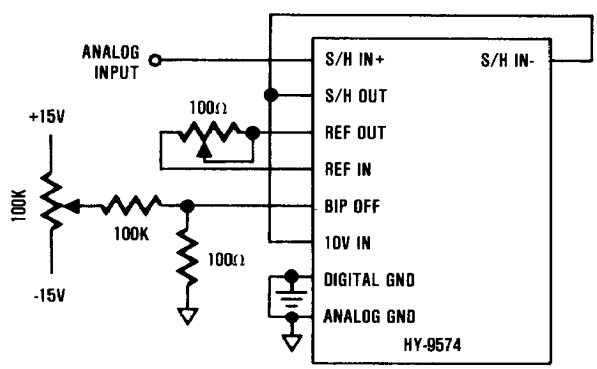


FIGURE 1. FOR CALIBRATION INSTRUCTION SEE "RANGE SELECTION AND CALIBRATION PROCEDURES" SECTION OF THIS DATA SHEET.

PARAMETER	TEMP	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
Input Voltage Range	-40°C to +85°C	±10			V
Input Resistance	25°C	1	5		MΩ
D.C. & TRANSFER ACCURACY SPECIFICATIONS					
Resolution (Maximum)				12	Bits
Linearity Error	-40°C to +85°C			±1	LSB
Differential Linearity Error					
J and A Models	Full			11	Bits
All Other Models	Full			12	Bits
DIGITAL INPUT & OUTPUT CHARACTERISTICS					
Input Voltage (High), V_{IH}	Full	+2.4		+5.5	V
Input Voltage (Low), V_{IL}	Full	-0.5		+0.8	V
Input Current (V_{IL} = 0V)	Full			-5 (Note 2)	μA
Input Current (V_{IH} = +5V)	Full			+5 (Note 2)	μA
Logic "0" Output (I_{SINK} = 1.6mA)	Full			+0.4	V
Logic "1" Output (I_{SOURCE} = 500μA)	Full	+2.4			V
Leakage Current (High Z State, DB0-11 Only)	Full	-5	0.1	+5	μA
POWER SUPPLY CHARACTERISTICS					
Positive Supply Voltage		+14.5		+16.0	V
Negative Supply Voltage		-14.5		-16.0	V
Logic Supply Voltage		+4.5		+5.5	V
Positive Supply Current (Note 3)			22	28	mA
Negative Supply Current (Note 3)			32	41	mA
Logic Supply Current			7	15	mA
Power Supply Rejection V+ (Note 10)					
J & A Models	25°C			±2	LSB
All Other Models	25°C			±1	LSB
Power Supply Rejection V- (Note 10)					
J & A Models	25°C			±2	LSB
All Other Models	25°C			±1	LSB
Power Dissipation			850		mW
TIMING SPECIFICATIONS					
Conversion Time 12 Bit Cycle	+25°C	15	20	25	μs
8 Bit Cycle	+25°C	10	13	17	μs
STS Delay After Data Valid	+25°C	300	500	1000	ns
S/H Acquisition Time (0.01%)	+25°C		1.0	1.5	μs
Aperture Time	+25°C		25		ns
Aperture Uncertainty	+25°C		0.3		ns
Droop Rate	+25°C		0.08	0.5	μV/μs
	-40°C to +85°C		17	100	μV/μs
Throughput Rate (Note 1)	+25°C			37	kHz

Electrical Characteristics Test Conditions (Unless otherwise specified)
V_{Supply} = ±15V; C_H - Internal; Digital Input (Pin 14), V_{AL} = +0.8V (Sample), V_{AH} = +2.0V (Hold).

OPERATING TEMP RANGE		-40°C ≤ TA ≤ 85°C			0°C ≤ TA ≤ 75°C			
PARAMETER	**TEMP**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT CHARACTERISTICS								
Input Voltage Range	Full	±10			±10			V
Input Resistance	25°C	1	5		1	5		MΩ
Input Capacitance	25°C			3			3	pF
Offset Voltage	25°C		0.2	0.5		0.5	1.0	mV
	Full			2.0			1.5	mV
Bias Current	25°C		70	200		100	300	nA
	Full			200			300	nA
Offset Current	25°C		30	100		30	300	nA
	Full			100			300	nA
Common Mode Range	Full	±10			±10			V
CMRR (Note 4)	25°C	80	90		72	90		dB
Offset Voltage T.C.	Full		5	15		5	20	µV/°C
TRANSFER CHARACTERISTICS								
Gain, dC	25°C	10^6	2×10^6		3×10^5	2×10^6		V/V
Gain Bandwidth Product (Note 5)								
C_H = 100pF	25°C		2.0			2.0		MHz
OUTPUT CHARACTERISTICS								
Output Voltage	Full	±10			±10			V
Output Current	25°C	±10			±10			mA
Full Power Bandwidth (Note 6)	25°C		600			600		kHz
Output Resistance (Hold Mode)	25°C		1.0			1.0		Ω
Total Output Noise, DC to 10MHz								
Sample	25°C		125	200		125	200	µV RMS
Hold	25°C		125	200		125	200	µV RMS
TRANSIENT RESPONSE								
Rise Time (Note 5)	25°C		100			100		ns
Overshoot (Note 5)	25°C		15			15		%
Slew Rate (Note 7)	25°C		45			45		V/µs
DIGITAL INPUT CHARACTERISTICS								
Input Voltage (High), V_{AH}	Full	2.0			2.0			V
Input Voltage (Low), V_{AL}	Full			0.8			0.8	V
Input Current (V_{AL} = 0V)	Full			4			4	µA
Input Current (V_{AH} = +5V)	Full			0.1			0.1	µA
SAMPLE/HOLD CHARACTERISTICS								
Acquisition Time (0.1%) (Note 7)	25°C		0.8	1.2		0.8	1.2	µs
Acquisition Time (0.01%) (Note 7)	25°C		1.0	1.5		1.0	1.5	µs
Aperture Time (Note 8)	25°C		25			25		ns
Effective Aperture Delay Time (See S/H Glossary)	25°C	-50	-25	0	-50	-25	0	ns
Aperture Uncertainty	25°C		0.3			0.3		ns
Hold Capacitor, C_H			100			100		pF
Droop Rate	25°C		0.08	0.5		0.08	0.5	µV/µs
Droop Rate	Full		2.4	100		1.2	100	µV/µs
Drift Current (Note 9)	25°C		8	50		8	50	pA
Drift Current (Note 9)	Full		0.24	10		0.12	10	nA
Charge Transfer (Note 9)	25°C		0.1	0.5		0.1	0.5	pC
Hold Mode Settling Time (0.01%)	Full		165	250		165	250	ns
Hold Mode Feedthrough 10Vp-p, 100kHz	Full		2			2		mV
POWER SUPPLY CHARACTERISTICS								
Power Supply Rejection V+	Full	80			80			dB
(Note 10) V-	Full	65			65			dB

DC and Transfer Accuracy Specifications

(Typical @ +25°C with V_{CC} = +15V, V_{LOGIC} = +5V, V_{EE} = -15V unless otherwise specified)

	TEMPERATURE RANGE 0°C to +75°C			
MODEL	**HY-9574J**	**HY-9574K**	**HY-9574L**	**UNITS**
Resolution (Maximum)	12	12	12	Bits
LINEARITY ERROR				
25°C (Maximum)	±1	±1/2	±1/2	LSB
0°C to +75°C (Maximum)	±1	±1/2	±1/2	LSB
DIFFERENTIAL LINEARITY ERROR				
(Max. resolution for which no missing codes is guaranteed)				
25°C	11	12	12	Bits
T_{MIN} to T_{MAX}	11	12	12	Bits
Unipolar Offset (Max.) (Adjustable to zero)	±2	±2	±2	LSB
Bipolar Offset (Max.) (Adjustable to zero)	±10	±4	±4	LSB
FULL SCALE CALIBRATION ERROR				
25°C (Max.), with fixed 50Ω resistor from REF OUT to REF IN (Adjustable to zero)	0.3	0.3	0.3	% of Full Scale
T_{MIN} to T_{MAX}				
(No adjustment at +25°C)	0.5	0.4	0.35	% of Full Scale
(With adjustment to zero at +25°C)	0.22	0.12	0.05	% of Full Scale
TEMPERATURE COEFFICIENTS				
Guaranteed max change to T_{MIN} or T_{MAX} (Using internal ref.)				
Unipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Bipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Full Scale Calibration	±9	±5	±2	LSB
	(45)	(25)	(10)	(ppm/°C)
POWER SUPPLY REJECTION				
Max. change in Full Scale Calibration				
+13.5V < V_{CC} < +16.5 or +11.4V < V_{CC} < +12.6V	±2	±1	±1	LSB
+4.5V < V_{LOGIC} < +5.5V	±1/2	±1/2	±1/2	LSB
-16.5V < V_{EE} < -13.5V or -12.6V < V_{EE} < -11.4V	±2	±1	±1	LSB
ANALOG INPUT RANGES				
Bipolar	-5 to +5			Volts
	-10 to +10			Volts
Unipolar	0 to +10			Volts
	0 to +20			Volts
INPUT IMPEDANCE				
10 Volt Span	5K, ± 25%			Ohms
20 Volt Span	10K, ± 25%			Ohms
INTERNAL REFERENCE				
Voltage	+10.0 ± 0.1 Max.			Volts
Output Current available for external loads (External load should not change during conversion.	2.0 Max.			mA

DC and Transfer Accuracy Specifications

(Typical @ +25°C with V_{CC} = +15V, V_{LOGIC} = +5V, V_{EE} = -15V unless otherwise specified)

	TEMPERATURE RANGE -40°C to +85°C		
MODEL	**HY-9574A**	**HY-9574B**	**UNITS**
Resolution (Maximum)	12	12	Bits
LINEARITY ERROR			
25°C (Maximum)	±1	±1/2	LSB
-40°C ≤ T_A ≤ 85°C (Maximum)	±1	±1	LSB
DIFFERENTIAL LINEARITY ERROR			
(Max. resolution for which no missing codes is guaranteed)			
25°C	11	12	Bits
T_{MIN} to T_{MAX}	11	12	Bits
Unipolar Offset (Max.) (Adjustable to zero)	±2	±2	LSB
Bipolar Offset (Max.) (Adjustable to zero)	±10	±4	LSB
FULL SCALE CALIBRATION ERROR			
25°C (Max.), with fixed 50Ω resistor from REF OUT to REF IN (Adjustable to zero)	0.3	0.3	% of Full Scale
T_{MIN} to T_{MAX}			
(No adjustment at +25°C)	0.8	0.6	% of Full Scale
(With adjustment to zero at +25°C)	0.5	0.25	% of Full Scale
TEMPERATURE COEFFICIENTS			
Guaranteed max change to T_{MIN} or T_{MAX} (Using internal ref.)			
Unipolar Offset	±2	±1	LSB
	(5)	(2.5)	(ppm/°C)
Bipolar Offset	±4	±2	LSB
	(10)	(5)	(ppm/°C)
Full Scale Calibration	±20	±10	LSB
	(50)	(25)	(ppm/°C)
POWER SUPPLY REJECTION			
Max. change in Full Scale Calibration			
+13.5V < V_{CC} < +16.5 or +11.4V < V_{CC} < +12.6V	±2	±1	LSB
+4.5V < V_{LOGIC} < +5.5V	±1/2	±1/2	LSB
-16.5V < V_{EE} < -13.5V or -12.6V < V_{EE} < -11.4V	±2	±1	LSB
ANALOG INPUTS, INPUT RANGES			
Bipolar	-5 to +5		Volts
	-10 to +10		Volts
Unipolar	0 to +10		Volts
	0 to +20		Volts
INPUT IMPEDANCE			
10 Volt Span	5KΩ, ± 25%		Ohms
20 Volt Span	10KΩ, ± 25%		Ohms
INTERNAL REFERENCE			
Voltage	+10.0 ± 0.1 Max.		Volts
Output Current	2.0 Max.		mA
available for external loads (External load should not change during conversion.			

Digital Characteristics (Note 11)

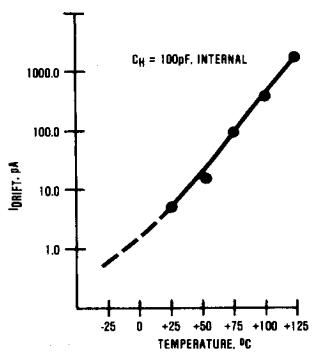
(ALL MODELS, OVER FULL TEMPERATURE RANGE)	MIN	TYP	MAX
Logic Inputs (CE, CS, R/C, A0, 12/8)			
Logic "1"	+2.4V (Note 12)		+5.5V
Logic "0"	-0.5V		+0.8V
Current	-5μA	0.1μA	+5μA
Capacitance		5pF	
Logic Outputs (DB11-DB0, STS)			
Logic "0" (I_{SINK} — 1.6mA)			+0.4V
Logic "1" (I_{SOURCE} — 500μA)	+2.4V		
Leakage (High - Z State, DB11-DB0 Only)	-5μA	0.1μA	+5μA
Capacitance		5pF	

NOTES:

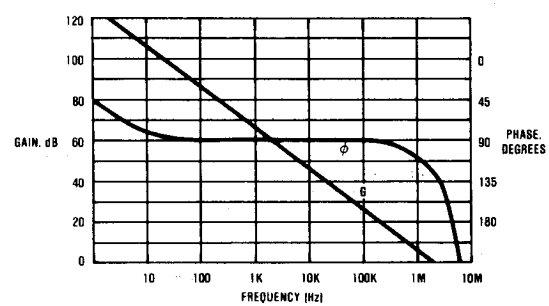
1. Maximum T.R. = $(t_{acq} + t_{conv})^{-1}$, see Harris Application Note 538.
2. Conventional current flowing into the package is designated "+", current flowing out is "—".
3. Supply current specified for a 0V differential between pins 1 and 32. Supply current will increase with differential input (as may occur in the Hold Mode) to approximately +39mA and -49mA at 20V.
4. V_{CM} = ±5VDC
5. Vo = 200mVp-p; R_L = 2kΩ; C_L = 50pF.
6. Vo = 20Vp-p; R_L = 2kΩ; C_L = 50pF; Unattenuated output.
7. Vo = 10V step; R_L = 2kΩ; C_L = 50pF.
8. Derived from computer simulation only, not tested.
9. V_{IN} = 0V, V_{AH} = +3.5V, tr < 20ns (V_{IL} to V_{IH}).
10. Based on a one volt delta in each supply, i.e. 15V ± 0.5VDC.
11. See "HY-9574 ADC Timing Specifications" for a detailed listing of digital timing parameters.
12. Although this guaranteed threshold is higher than standard TTL (+2.0V), bus loading is much less, i.e., typical input current is only 0.25% of a TTL load.

Sample/Hold Amplifier Performance Curves V_{SUPPLY} = ±15VDC

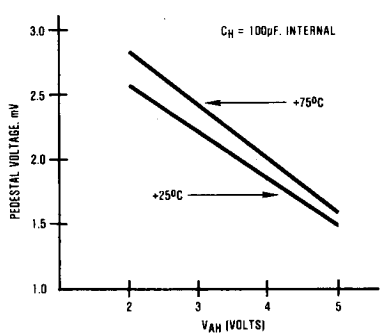
DRIFT CURRENT vs. TEMPERATURE



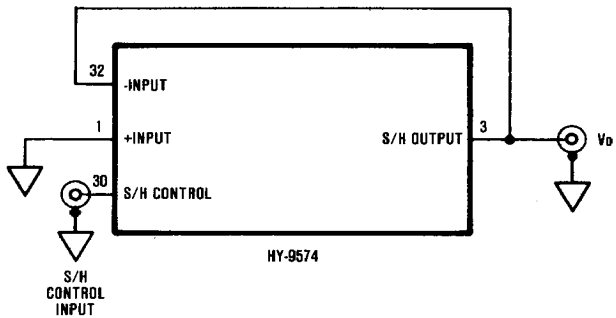
OPEN LOOP GAIN AND PHASE RESPONSE



PEDESTAL vs. LOGIC (V_{AH}) VOLTAGE

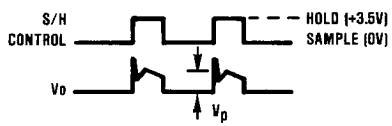


CHARGE TRANSFER AND DRIFT CURRENT



CHARGE TRANSFER TEST

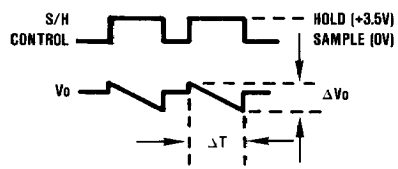
1. Observe the "pedestal" voltage V_p:



2. Compute charge transfer: Q = VpCH

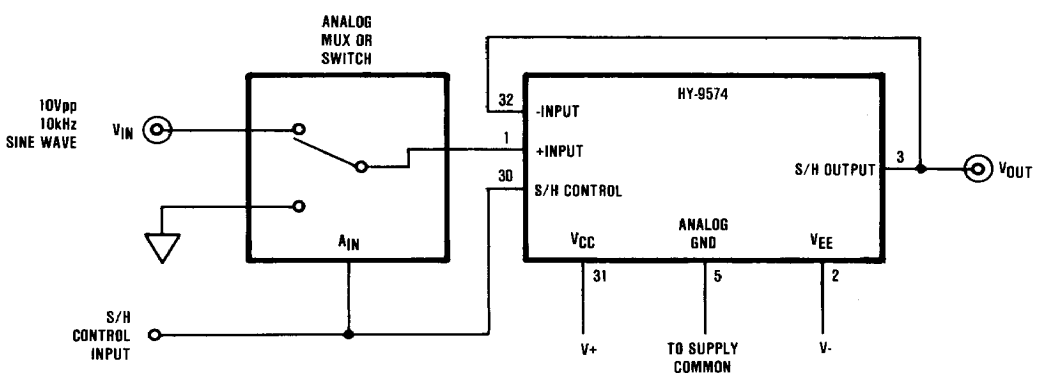
DRIFT CURRENT TEST

1. Observe the voltage "droop", $\Delta Vo/\Delta T$:



2. Measure the slope of the output during hold, $\Delta Vo/\Delta T$, and compute drift current: $I_D = C_H \Delta Vo/\Delta t$.

S/H HOLD MODE FEEDTHROUGH ATTENUATION



$$\text{FEEDTHROUGH (dB)} = 20 \text{ Log } \frac{V_{OUT}}{V_{IN}}$$

WHERE V_{OUT} = VOLTS pp, Hold Mode
V_{IN} = VOLTS pp

Glossary of Terms

Sample and Hold

Acquisition Time — The time required following a "sample" command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

Charge Transfer — The small charge transferred to the holding capacitor from the inter-electrode capacitance of the switch when the unit is switched to the Hold Mode. Charge transfer is directly proportional to sample-to-hold offset pedestal error, where:

$$\text{Charge Transfer (pC)} = C_H \text{ (pF)} \times \text{Offset Error (V)}$$

Aperture Time — The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

Hold Step Error — The output error due to Charge Transfer (see above). It may be calculated from the specified parameter, Charge Transfer, using the following relationship:

$$\text{Hold Step (V)} = \frac{\text{Charge Transfer (pC)}}{100\text{pF}}$$

See Sample/Hold Amplifier Performance Curves.

Effective Aperture Delay Time (EADT) — The difference between propagation time from the analog input to the S/H switch, and digital delay time between the Hold command and opening of the switch.

EADT may be positive, negative or zero. If zero, the S/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors will correspond to a value of V_{IN} that occurred before the Hold command.

Aperture Uncertainty — The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

Drift Current — The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

$$I_D \text{ (pA)} = C_H \text{ (pF)} \times \frac{\Delta V}{\Delta T} \text{ (Volts/sec)}$$

Analog/Digital Converter

Linearity Error — Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs ½LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level one and one-half (1½) LSB's beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HY-9574K, L, and B grades are guaranteed for maximum nonlinearity of ±½LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HY-9574J and A grades are guaranteed to ±1LSB maximum error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one. Note that the linearity error is not user-adjustable.

Differential Linearity Error (No Missing Codes) — A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HY-9574K, L, and B grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HY-9574J and A grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

Unipolar Offset — The first transition should occur at a level ½LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

Bipolar Offset — Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value ½LSB below analog common. The bipolar offset error and temperature specify the initial deviation and maximum change in the error over temperature.

Full Scale Calibration Error — The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value one and one-half (1½) LSB's below the nominal full scale (9.9963 volts for 10,000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 2 and 3. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

Temperature Coefficients — The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

Power Supply Rejection — The standard specifications for the HY-9574 assume use of +5.00 and ±15.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

Code Width — A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

Quantization Uncertainty — Analog-to-digital converters exhibit an inherent quantization uncertainty of ±½LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

Left-Justified Data — The data format used in the HY-9574 is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

Applying the HY-9574

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

Physical Mounting and Layout Considerations

Layout — Unwanted, parasitic circuit components, (L, R and C) can make 12 bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies — Supply voltages to the HY-9574 (+15V, -15V and +5V) must be "quiet" and well regulated. Voltage spikes on these lines can affect the converter's accuracy, causing several LSB's to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure "quiet" DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessasry to counter the effect of variations in supply current. Connect one pair from pin 24 to 10 (V_{LOGIC} Supply), one from pin 31 to 5 (V_{CC} to Analog Common) and one from pin 2 to 5 (V_{EE} to Analog Common). For each capacitor pair, a 10μF tantalum type in parallel with a 0.1μF ceramic type is recommended.

Ground Connections — Pin 5 (Analog Common) and pin 10 (Digital Common) should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 5 to (usually) 15V common, and from pin 10 to (usually) the +5V logic common. If the converter is located some distance from the system's "single point" ground, make only these connections to pins 5 and 10: Tie them together at the package, and back to the system ground with a single path. This path should have low resistance. (Code dependent currents flow in the V_{CC}, V_{EE} and V_{LOGIC} terminals, but not through the HY-9574's Analog Common or Digital Common.

Range Connections And Calibration Procedures

The HY-9574 is a "complete sampling" A/D converter, meaning it can be fully operational with addition of the power supply voltages, a Start Convert signal, and a few external components as shown in Figures 2 and 3. Nothing more is required for most applications.

Whether controlled by a processor or operating in the stand-alone mode, the HY-9574 offers three standard input ranges: 0V to +10V, ±5V and ±10V. The maximum errors for gain and offset are listed under Specifications. If required, however, these errors may be adjusted to zero as explained below. Power supply and ground connections have been discussed in an earlier section.

Unipolar Connections and Calibration — Refer to Figure 2. The resistors shown are for calibration of offset and gain. If this is not required, replace R2* with a 50Ω, 1% metal film resistor and remove the network on pin 7. Connect pin 7 to pin 5. Then connect the S/H output to pin 8 for the 0V to 10V range. Inputs to +20V (5V over the power supply) are no problem for the A/D - the converter operates normally. But the S/H cannot handle inputs over V_{CC}.

Calibration consists of adjusting the converter's most negative output to its ideal value (offset adjustment), then, adjusting the most positive output to its ideal value (gain adjustment). To understand the procedure, note that in principle, one is settling the output with respect to the midpoint of an increment of analog input, as denoted by two adjacent code changes. Nominal value of an increment is one LSB. However, this approach is impractical because nothing "happens" at a midpoint to indicate that an adjustment is complete. Therefore, calibration is performed in terms of the observable code changes instead of the midpoint between code changes.

For example, midpoint of the first LSB increment should be positioned at the origin, with an output code of all 0's. To do this, apply an input of +½LSB (+1.22mV for the 10V range). Adjust the Offset potentiometer R1 until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Next, perform a Gain Adjust at positive full scale. Again, the ideal input corresponding to the last code change is applied. This is one and one-half (1½) LSB's below the nominal full scale (+9.9963V for 10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Connections and Calibration — Refer to Figure 3. The gain and offset errors listed under Specifications may be adjusted to zero using potentiometers R1 and R2*. If this isn't required, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

Connect the S/H output to pin 8 for a ±5V range, or to pin 9 for a ±10V range. Calibration of offset and gain is similar to that for the unipolar ranges as discussed above. First apply a DC input voltage ½LSB above negative full scale (i.e., -4.9988V for the ±5V range, or -9.9976V for the ±10V range). Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage one and one-half (1½) LSB's below positive full scale (+4.9963V for ±5V range; +9.9927 for ±10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

* The 100Ω potentiometer R2 provides Gain Adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (LSB equals 2.5mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then, to provide Gain Adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 8.

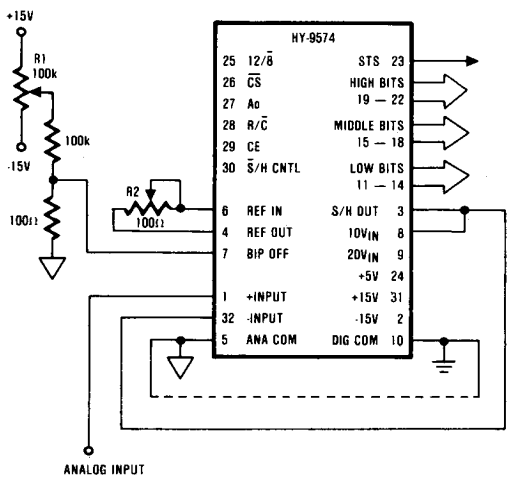


FIGURE 2. UNIPOLAR CONNECTIONS

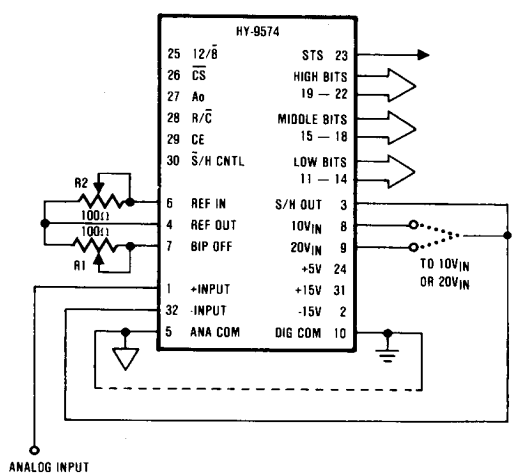


FIGURE 3. BIPOLAR INPUT CONNECTIONS

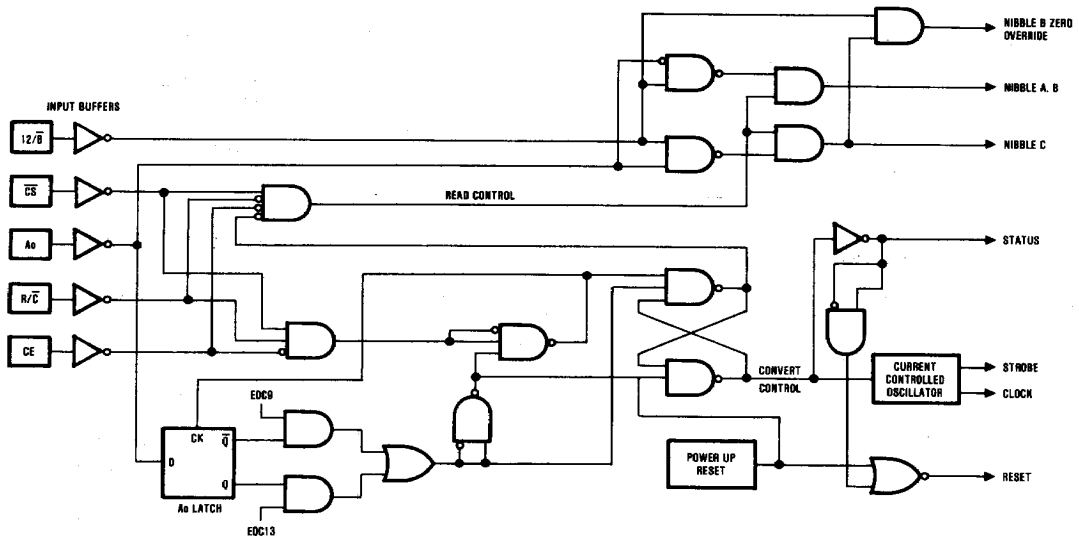


FIGURE 4. HY-9574 ADC CONTROL LOGIC

Controlling The HY-9574

The HY-9574 includes logic for direct interface to most microprocessor systems. The processor may take full control of each conversion, or the converter may operate in the "stand-alone" mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8 or 12 bit conversion cycle, capturing the signal with the S/H, initiating the conversion, and reading the output data when ready - choosing either 12 bits at once or 8 followed by 4, in a left-justified format. The six control inputs are all TTL/CMOS compatible: (12/$\overline{8}$, $\overline{CS}$, Ao, $\overline{S}$/H, R/$\overline{C}$ and CE). Table 1 illustrates the use of these inputs in controlling the converter's operations. Also, a simplified schematic of the internal control logic for the ADC is shown in Figure 4.

"Stand-Alone Operation"

The simplest control interface calls for a single control line connected to R/$\overline{C}$ as shown in Figure 5. The output data appears in words of 12 bits each.

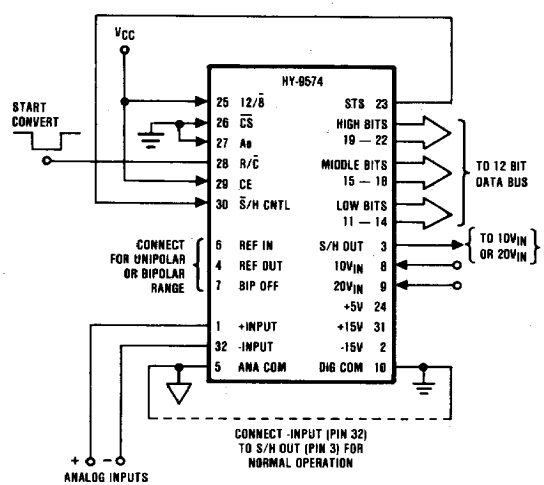


FIGURE 5. GENERAL PURPOSE 12 BIT "STAND ALONE" CONFIGURATION

The R/$\overline{C}$ signal may have any duty cycle within (and including) the extremes shown in Figures 6 and 7. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress. Timing parameters particular to this mode of operation are listed below under "Stand-Alone Mode Timing."

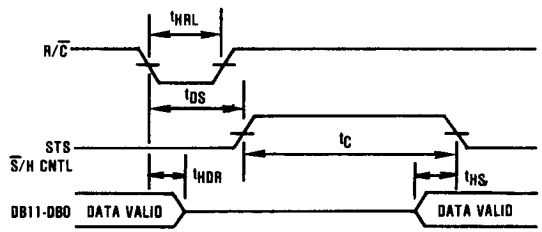


FIGURE 6. LOW PULSE FOR R/$\overline{C}$ — OUTPUTS ENABLED AFTER CONVERSION

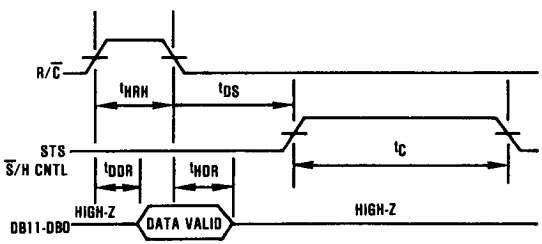


FIGURE 7. HIGH PULSE FOR R/$\overline{C}$ — OUTPUTS ENABLED WITH R/$\overline{C}$ HIGH, OTHERWISE HIGH-Z

Stand-Alone Mode Timing

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid	300	500	1000	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

Conversion Length

A Convert Start transition (See Table 1) latches the state of Ao, which determines whether the conversion continues for 12 bits (Ao low) or stops with 8 bits (Ao high). If all 12 bits are read following an 8 bit conversion, the three LSB's will read zero and DB3 will read ONE. Ao is latched because it is also involved in enabling the output buffers (see "Reading the Output Data"). No other control inputs are latched.

TABLE 1. TRUTH TABLE FOR HY-9574 CONTROL INPUTS

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	Ao	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

Conversion Start

Once a signal is captured by the S/H, conversion may be initiated as shown in Table 1 by a logic transition on any of three inputs: CE, $\overline{CS}$ or R/$\overline{C}$. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same, and if necessary, all three may change state simultaneously. To assure that a particular input controls the start of conversion, the other two should be set up at least 50ns earlier, however. See the HY-9574 Timing Specifications, Convert Mode.

This variety of HY-9574 control modes allows a simple interface in most system applications. The Convert Start timing relationships are illustrated in Figure 8.

The output signal STS indicates status of the converter by going high only while a conversion is in progress. While STS is high, the output buffers remain in a high impedance state and data cannot be read. Also, an

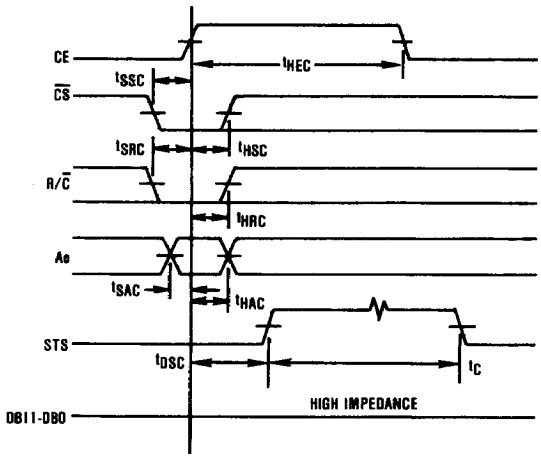


FIGURE 8. CONVERT START TIMING

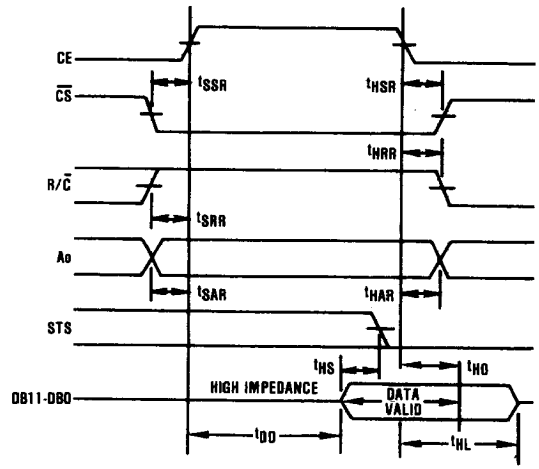


FIGURE 9. READ CYCLE TIMING

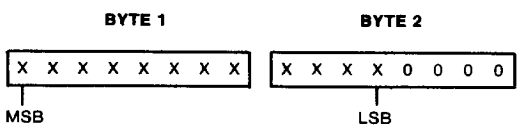
additional Start Convert will not reset the converter or reinitiate a conversion while STS is high. (However, if Ao changes state after a conversion begins, an additional Start Convert signal will latch the new state of Ao, possibly causing a wrong cycle length (8 vs 12 bits) for that conversion).

Reading The Output Data

The output data buffers remain in a high impedance state until four conditions are met: R/$\overline{C}$ high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs 12/$\overline{8}$ and Ao. Timing constraints are illustrated in Figure 9.

The 12/$\overline{8}$ input will be tied high or low in most applications, though it is fully TTL/CMOS compatible. With 12/$\overline{8}$ high, all 12 output lines become active simultaneously, for interface to a 12 or 16 bit data bus. The Ao input is ignored.

With 12/$\overline{8}$ low, the output is organized in two 8 bit bytes, selected one at a time by Ao. This allows an 8 bit data bus to be connected as shown in Figure 10. Ao is usually tied to the least significant bit of the address bus, for storing the HY-9574 output in two consecutive memory locations. (With Ao low, the 8 MSB's only are enabled. With Ao high, 4 MSB's are disabled, bits 4 through 7 are forced to zero, and the 4 LSB's are enabled). This two byte format is considered "left justified data", for which a decimal (or binary!) point is assumed to the left of byte 1:



Further, Ao may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in Figure 10 will never be enabled at the same time.

A read operation usually begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than (t_{DD} + t_{HS}) before STS goes low. See Figure 9.

HY-9574 ADC Timing Specifications at +25°C *

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
CONVERT MODE					
t_{DSC}	STS Delay from CE		100	200	ns
t_{HEC}	CE Pulse Width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE Setup	50	20		ns
t_{HSC}	$\overline{CS}$ Low during CE High	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE Setup	50	0		ns
t_{HRC}	R/$\overline{C}$ Low during CE High	50	20		ns
t_{SAC}	Ao to CE Setup	0	0		ns
t_{HAC}	Ao Valid during CE High	50	20		ns
t_C	Conversion Time, 12-Bit Cycle **	15	20	25	μs
	8-Bit Cycle **	10	13	17	μs
READ MODE					
t_{DD}	Access Time from CE		75	150	ns
t_{HD}	Data Valid after CE Low	25	35		ns
t_{HL}	Output Float Delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup	50	0		ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0	0		ns
t_{SAR}	Ao to CE Setup	50	25		ns
t_{HSR}	$\overline{CS}$ Valid after CE Low	0	0		ns
t_{HRR}	R/$\overline{C}$ High after CE Low	0	0		ns
t_{HAR}	Ao Valid after CE Low	50	25		ns
t_{HS}	STS Delay after Data Valid	300	500	1000	ns

* Time is measured from 50% level of digital transitions.
** Tmin to Tmax

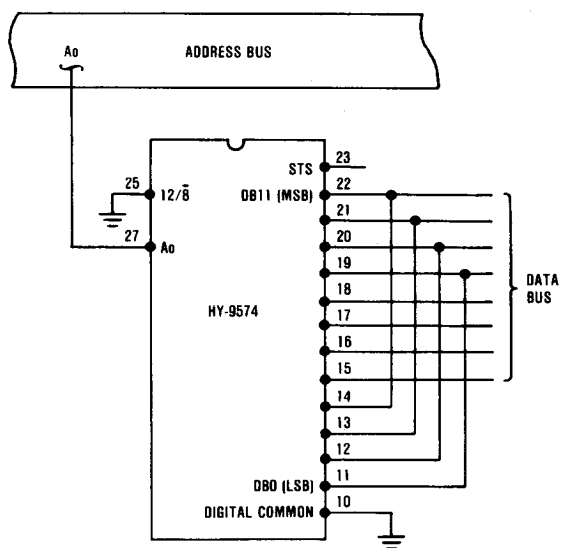
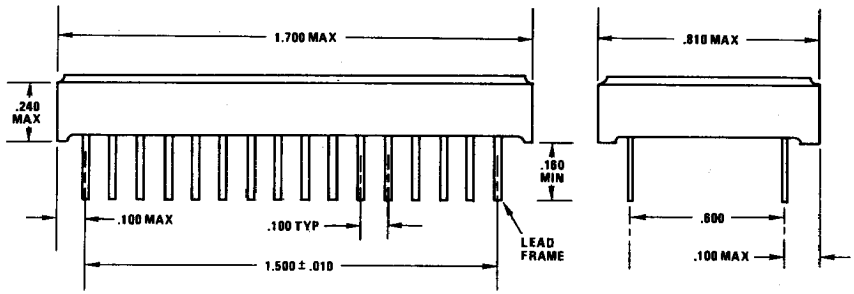


FIGURE 10. INTERFACE TO AN 8-BIT DATA BUS

Package

32 PIN PLASTIC DIP



Ordering Information

MODEL	TEMPERATURE	MAX LIN. ERROR	RESOLUTION NO MISS. CODE	FULL SCALE TC ppm/°C MAX
J = HY3-9574J-5	0°C to +75°C	±1 LSB	11 Bits	45.0
K = HY3-9574K-5	0°C to +75°C	±½ LSB	12 Bits	25.0
L = HY3-9574L-5	0°C to +75°C	±½ LSB	12 Bits	10.0
A = HY3-9574A-9	-40°C to +85°C	±1 LSB	11 Bits	50.0
B = HY3-9574B-9	-40°C to +85°C	±1 LSB	12 Bits	25.0