

CXK581000ATM/AYM/AM -10LLB

-10LLB

131072-word × 8-bit High Speed CMOS Static RAM

Description

The CXK581000ATM/AYM/AM is a high speed CMOS static RAM organized as 131072 words by 8 bits.

A polysilicon TFT cell technology realized extremely low stand-by current and higher data retention stability.

Special feature are low power consumption, high speed and broad package line-up.

The CXK581000ATM/AYM/AM is a suitable RAM for portable equipment with battery back up.

Features

- Wide supply voltage range operation: 2.7 to 5.5V
- Fast access time: (Access time)

3V Operation 150ns (Max.)

5V Operation 100ns (Max.)

- Low standby current

3V Operation 14μA (Max.)

5V Operation 20μA (Max.)

- Low voltage data retention: 2.0 V (Min.)

- Broad package line-up

CXK581000ATM/AYM

8mm x 20mm 32 pin TSOP package

CXK581000AM

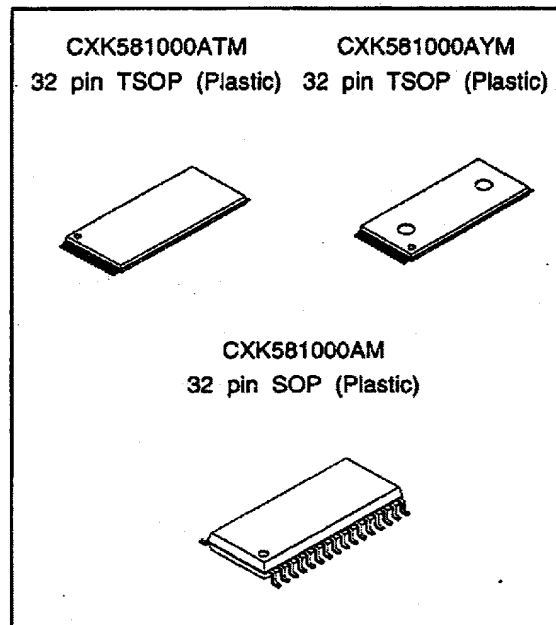
525mil 32 pin SOP package

Function

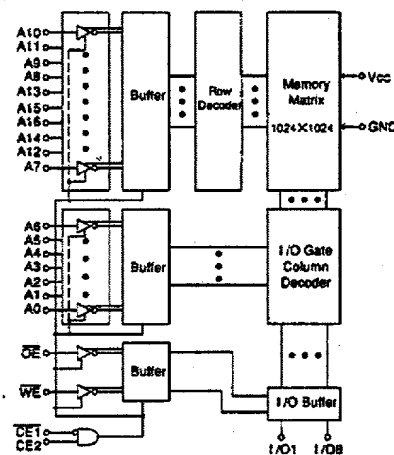
131072 word x 8 bit static RAM

Structure

Silicon gate CMOS IC

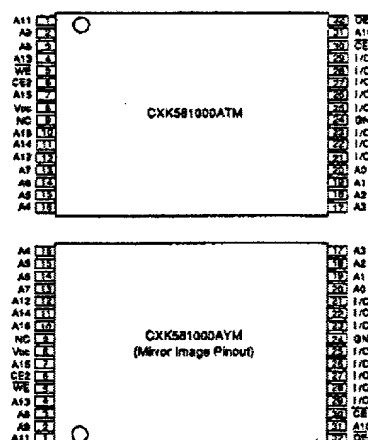


Block Diagram



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Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	Power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta=25°C, GND=0 V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5* to Vcc+0.5	
Input and output voltage	V _{I/O}	-0.5* to Vcc+0.5	
Allowable power dissipation	P _d	0.7	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	
Soldering temperature	T _{solder}	235 ± 10	°C · s

*V_{IN} V_{I/O} = -3.0 V Min. for pulse width less than 50ns.

Truth Table

CE1	CE2	OE	WE	Mode	I/O pin	Vcc current
H	x	x	x	Not selected	High Z	ISB1, ISB2
x	L	x	x	Not selected	High Z	ISB1, ISB2
L	H	H	H	Output disable	High Z	Icc1, Icc2, Icc3
L	H	L	H	Read	Data out	Icc1, Icc2, Icc3
L	H	x	L	Write	Data in	Icc1, Icc2, Icc3

x: "H" or "L"

DC Recommended Operating Conditions

(Ta=0 to +70°C, GND=0 V)

Item	Symbol	Vcc=5V±10%			Vcc=2.7 to 5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply voltage	Vcc	4.5	—	5.5	2.7	—	5.5	V
Input high voltage	V _{IH}	2.2	—	Vcc+0.3	2.2	—	Vcc+0.3	
Input low voltage	V _{IL}	-0.3*	—	0.8	-0.3*	—	0.4	

*V_{IL} = -3.0 V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC characteristics

(GND=0 V, $T_a=0$ to $+70^{\circ}\text{C}$)

Item	Symbol	Test conditions	VCC=3V $\pm$ 10%			VCC=5V $\pm$ 10%			Unit
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	ILI	VIN=GND to VCC	-1	—	1	-1	—	1	μA
Output leakage current	ILO	$\overline{\text{CE}}1=\text{V}_{\text{IH}}$ or $\text{CE}2=\text{V}_{\text{IL}}$ or $\overline{\text{OE}}=\text{V}_{\text{IH}}$ or $\overline{\text{WE}}=\text{V}_{\text{IL}}$ V/O=GND to VCC	-1	—	1	-1	—	1	
Operating power supply current	ICC1	$\overline{\text{CE}}1=\text{V}_{\text{IL}}$, $\text{CE}2=\text{V}_{\text{IH}}$ VIN=V _{IH} or V _{IL} IOUT=0mA	—	0.5	1.3	—	7	15	mA
Average operating current	ICC2	Min. cycle duty=100% IOUT=0mA	—	14	23	—	35	60	
	ICC3	Cycle time 1 μs duty=100% IOUT=0mA $\overline{\text{CE}}1 \leq 0.2\text{V}$ $\text{CE}2 \geq \text{V}_{\text{CC}} - 0.2\text{V}$ $\text{V}_{\text{IL}} \leq 0.2\text{V}$ $\text{V}_{\text{IH}} \geq \text{V}_{\text{CC}} - 0.2\text{V}$	—	3	7	—	10	20	
Standby current	ISB1	$\text{CE}2 \leq 0.2\text{V}$ or $\overline{\text{CE}}1 \geq \text{V}_{\text{CC}} - 0.2\text{V}$ $\text{CE}2 \geq \text{V}_{\text{CC}} - 0.2\text{V}$	0 to $+70^{\circ}\text{C}$		14	—	—	20	μA
			0 to $+40^{\circ}\text{C}$		2.8	—	—	4	
			$+25^{\circ}\text{C}$		1.4	—	0.7	2	
	ISB2	$\overline{\text{CE}}1=\text{V}_{\text{IH}}$ or $\text{CE}2=\text{V}_{\text{IL}}$	—	0.06	0.3	—	0.6	3	mA
Output high voltage	VOH	I _{OH} =-1.0mA	2.2	—	—	2.4	—	—	V
Output low voltage	VOL	I _{OL} =2.1mA	—	—	0.4	—	—	0.4	

* $T_a=25^{\circ}\text{C}$

I/O capacitance

(Ta=25°C, f=1MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	—	7	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	—	8	

Note) This parameter is sampled and is not 100% tested.

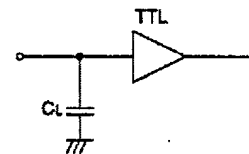
AC Characteristics

• AC test conditions

(V_{CC}=2.7 to 5.5V, Ta=0 to +70°C)

• Test circuit

Item	Conditions	
	V _{CC} =3V±10%	V _{CC} =5V±10%
Input pulse high level	V _{IH} =2.2 V	V _{IH} =2.2 V
Input pulse low level	V _{IL} =0.4 V	V _{IL} =0.8 V
Input rise time	t _r =5ns	t _r =5ns
Input fall time	t _f =5ns	t _f =5ns
Input and output reference level	1.5 V	1.5 V
Output load conditions	C _L *=100pF, 1TTL	C _L *=100pF, 1TTL



* C_L includes scope and jig capacitances.

• Read cycle ($\overline{WE}$ ="H")

Item	Symbol	VCC=3V±10%		VCC=5V±10%		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	tRC	150	—	100	—	ns
Address access time	tAA	—	150	—	100	
Chip enable access time ($\overline{CE1}$)	tCO1	—	150	—	100	
Chip enable access time (CE2)	tCO2	—	150	—	100	
Output enable to output valid	tOE	—	70	—	50	
Output hold from address change	tOH	15	—	15	—	
Chip enable to output in low Z ($\overline{CE1}$, CE2)	tLZ1, tLZ2	10	—	10	—	
Output enable to output in low Z ($\overline{OE}$)	tOLZ	5	—	5	—	
Chip disable to output in high Z ($\overline{CE1}$, CE2)	tHZ1*, tHZ2*	—	50	—	35	
Output disable to output in high Z ($\overline{OE}$)	tOHZ*	—	50	—	35	

* tHZ1, tHZ2 and tOHZ are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

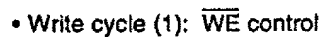
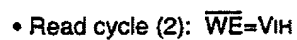
• Write cycle

Item	Symbol	VCC=3V±10%		VCC=5V±10%		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	tWC	150	—	100	—	ns
Address valid to end of write	tAW	100	—	70	—	
Chip enable to end of write	tCW	100	—	70	—	
Data to write time overlap	tDW	60	—	40	—	
Data hold from write time	tDH	0	—	0	—	
Write pulse width	tWP	90	—	70	—	
Address setup time	tAS	0	—	0	—	
Write recovery time ($\overline{WE}$)	tWR	0	—	0	—	
Write recovery time ($\overline{CE1}$, CE2)	tWR1	0	—	0	—	
Output active from end of write	tOW	10	—	10	—	
Write to output in high Z	tWHZ*	—	30	—	30	

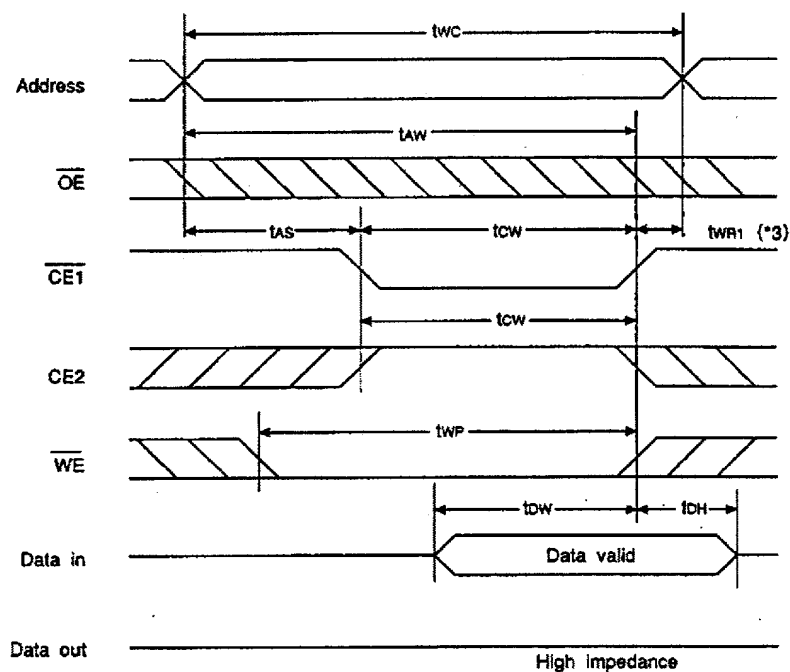
* tWHZ is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

- Read cycle (1): $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$

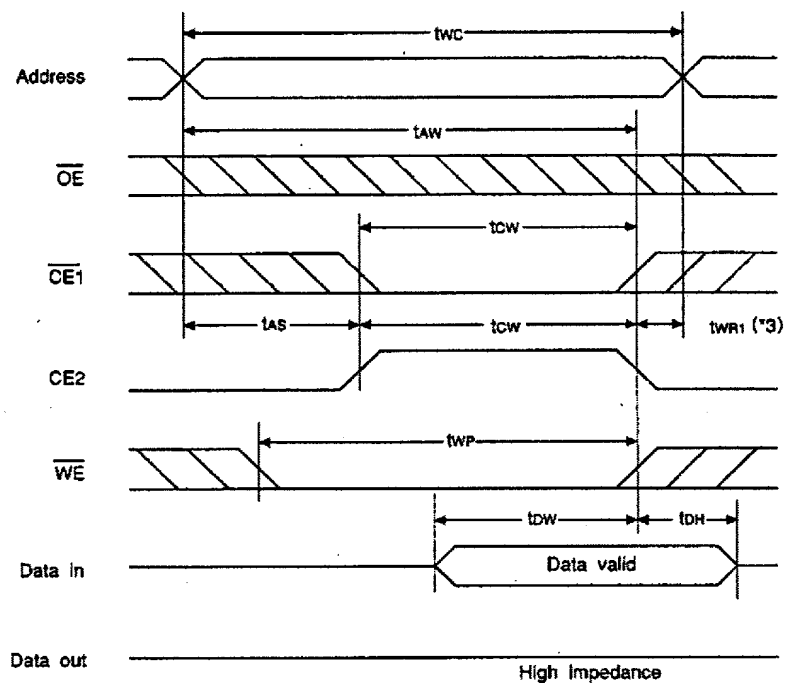
- Read cycle (1): $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



• Write cycle (2): $\overline{CE1}$ control



• Write cycle (3): $\overline{CE2}$ control

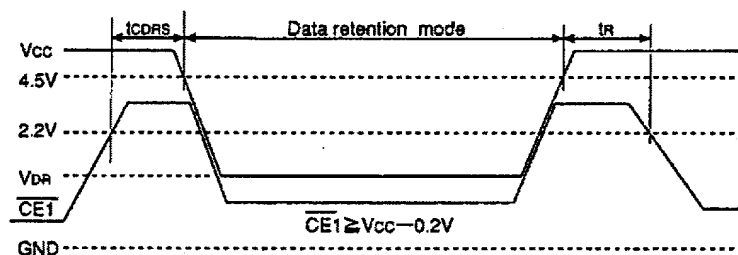


Note)

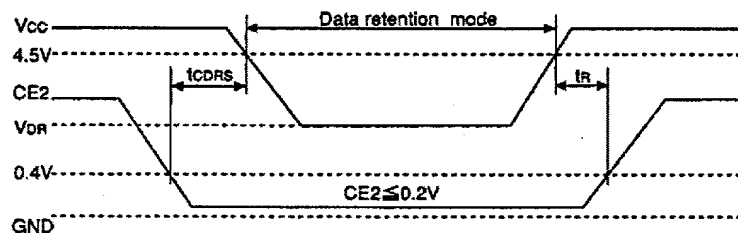
- *1 Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and $\overline{CE2}$ is at high simultaneously.
- *2 Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.
- *3 t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of $\overline{CE2}$, whichever comes earlier, until the end of the write cycle.

Data retention waveform

- Low supply voltage data retention waveform (1) ($\overline{\text{CE1}}$ control)



- Low supply voltage data retention waveform (2) (CE2 control)



Data Retention Characteristics

(Ta=0 to 70°C)

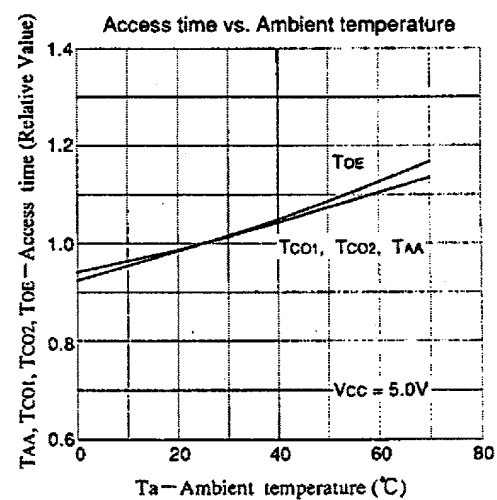
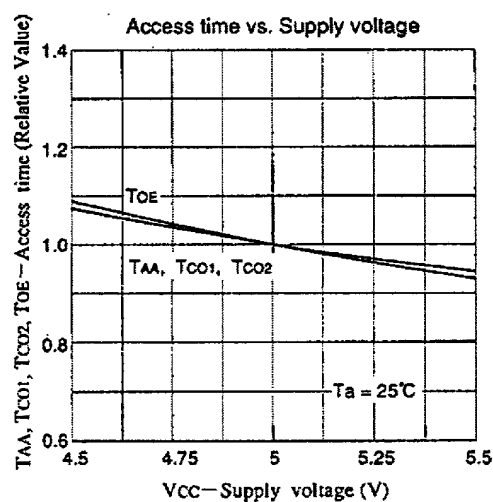
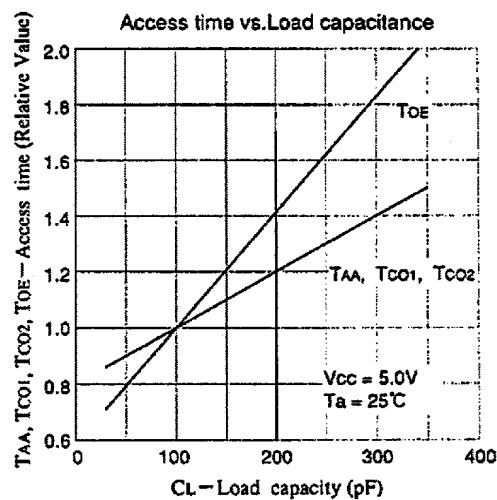
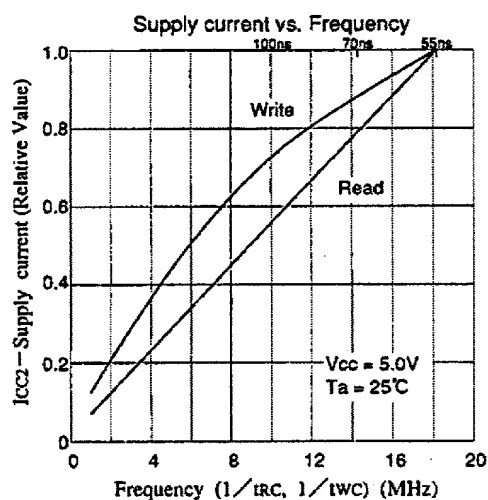
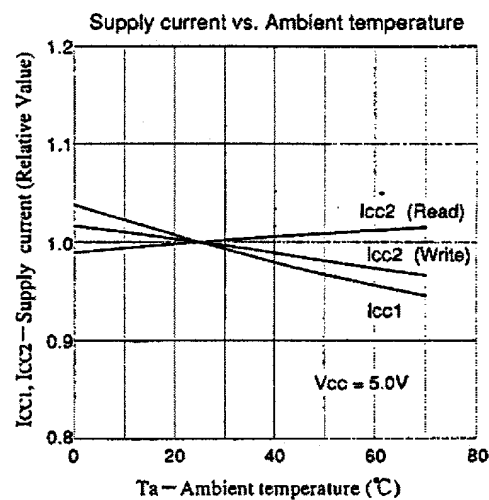
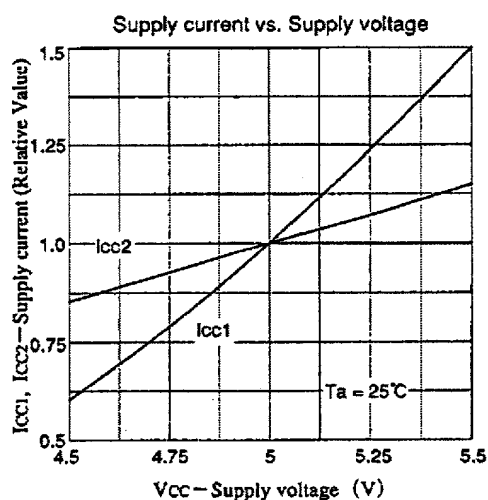
Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Data retention voltage	VDR	*1	2.0	—	5.5	V
Data retention current	ICCDR1	VCC=3.0 V*1	0 to +70°C	—	12	μA
			0 to +40°C	—	2.4	
			+25°C	0.4	1.2	
	ICCDR2	VCC=2.0 to 5.5 V*1	—	0.7*2	20	
Data retention setup time	tCDRS	Chip disable to data retention mode	0	—	—	ns
Recovery time	tr		5	—	—	ms

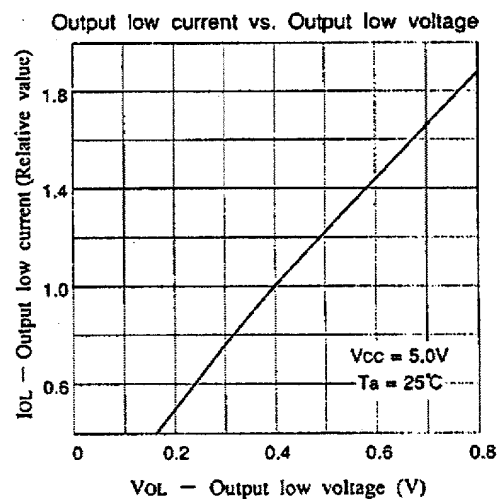
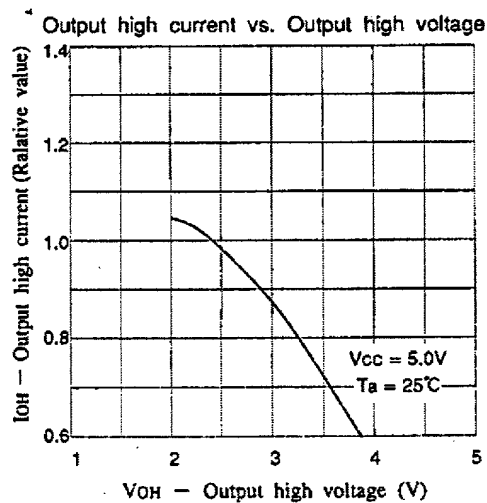
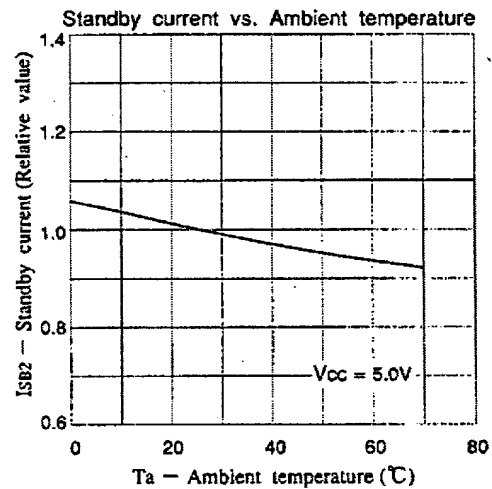
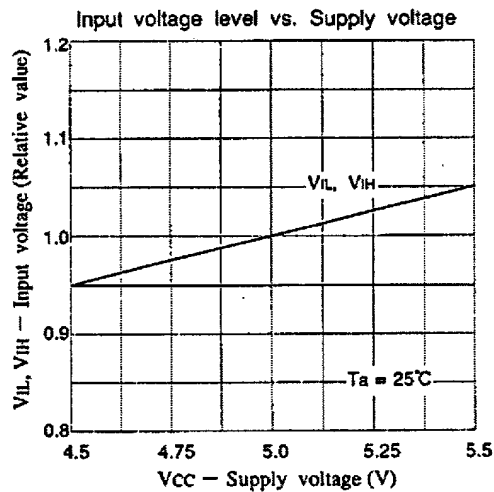
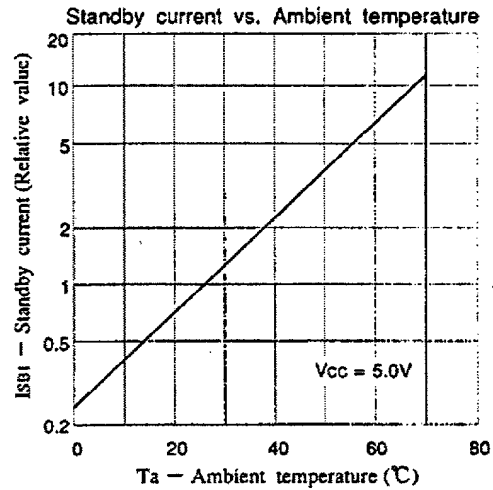
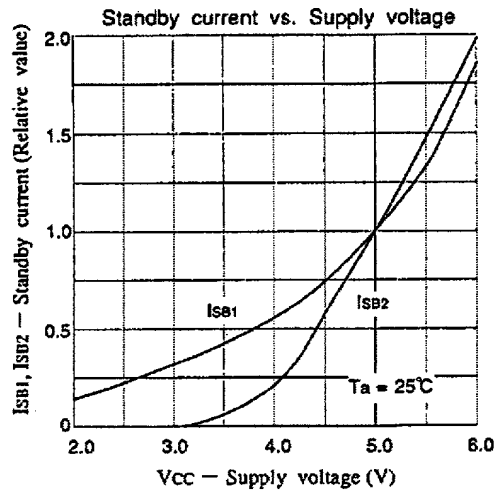
Note)

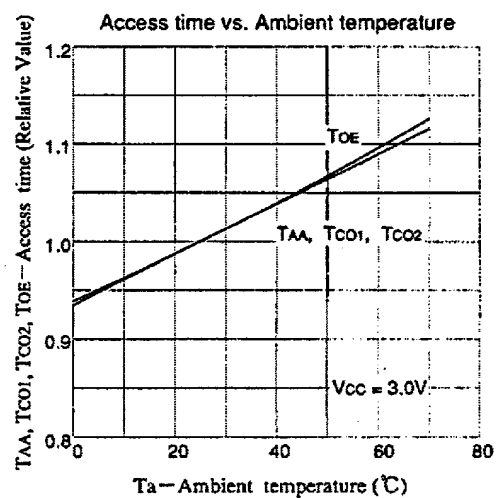
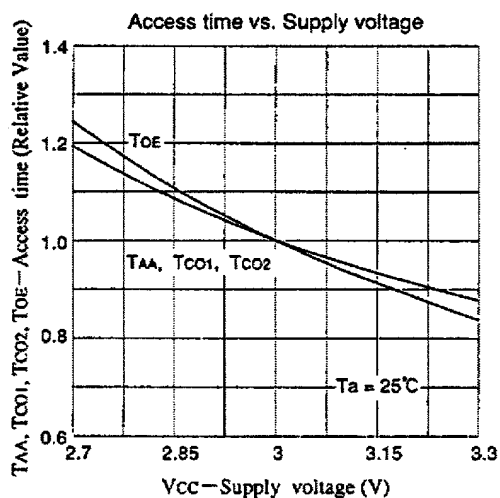
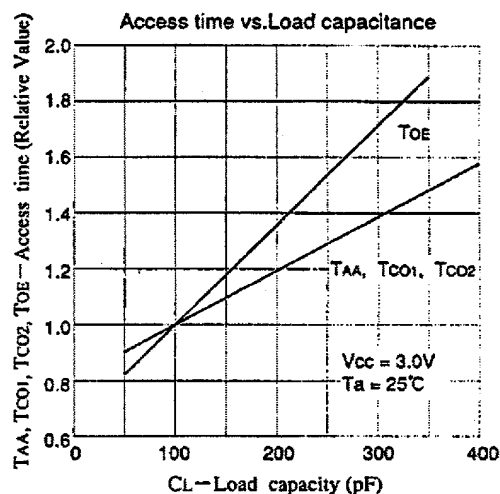
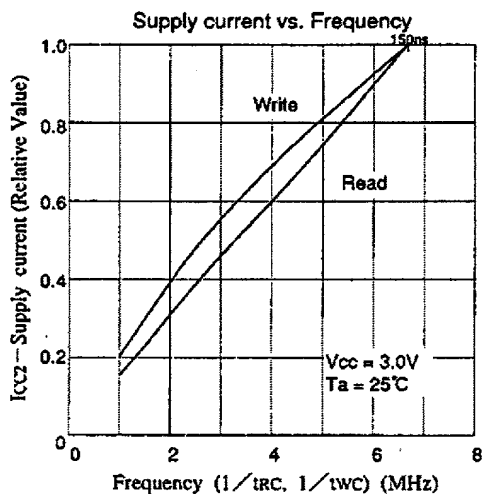
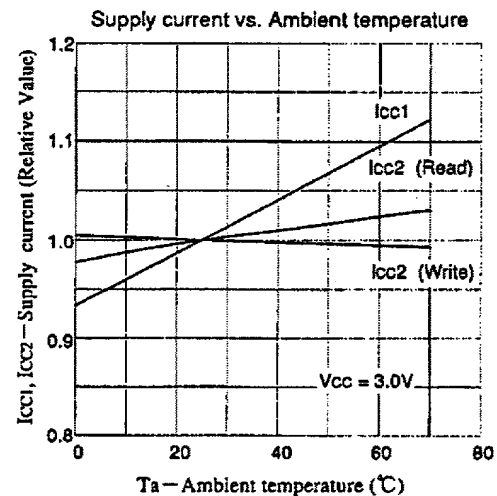
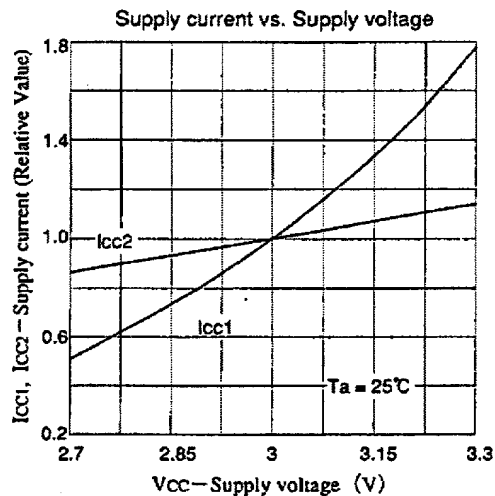
*1 $\overline{\text{CE1}} \geq V_{\text{CC}} - 0.2 \text{ V}$, $\text{CE2} \geq V_{\text{CC}} - 0.2 \text{ V}$ [$\overline{\text{CE1}}$ control] or $\text{CE2} \leq 0.2 \text{ V}$ [CE2 control]

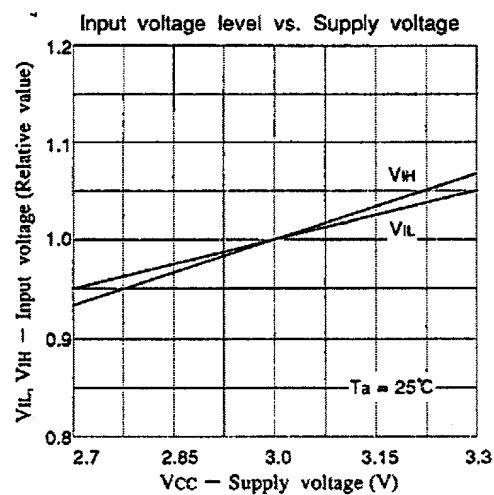
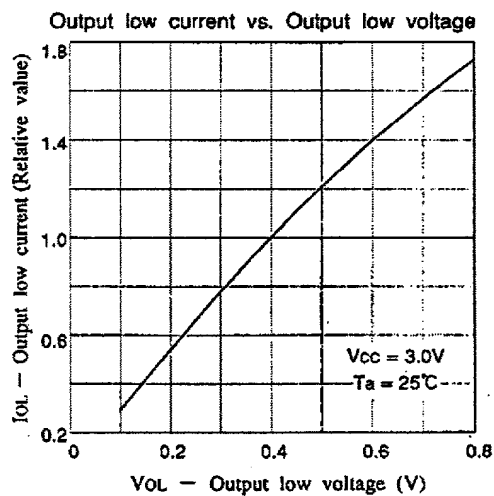
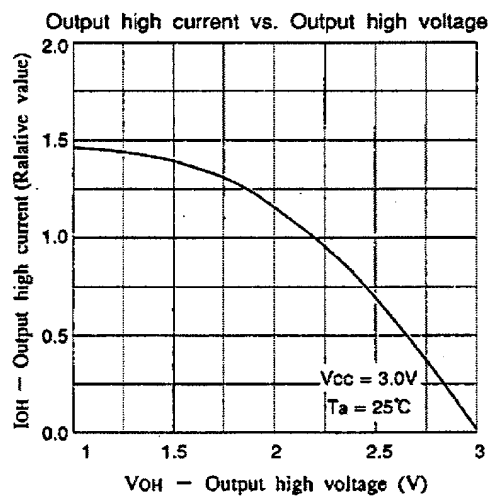
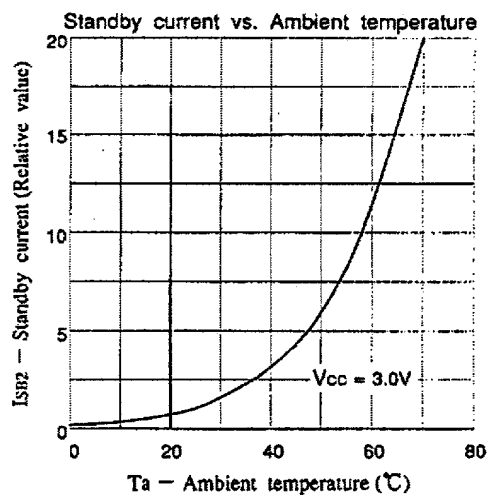
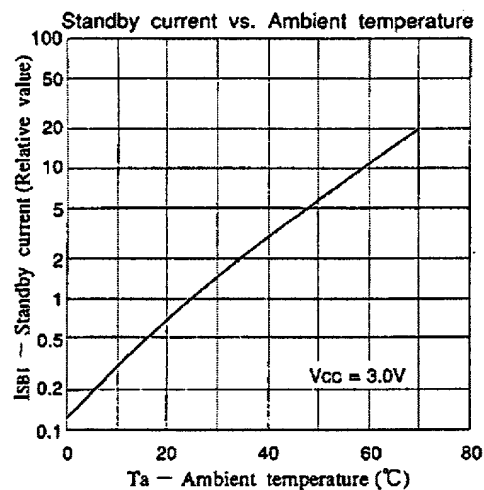
*2 VCC=5 V, Ta=25°C

Example of Representative Characteristics





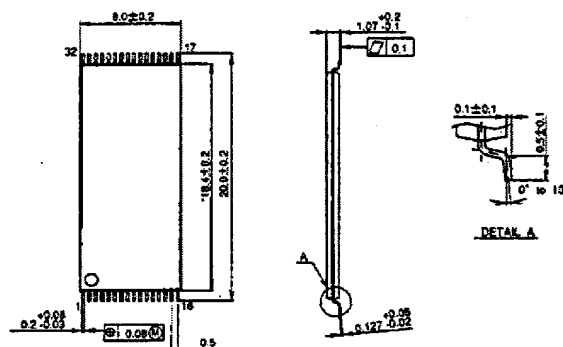




Package Outline Unit : mm

CXK581000ATM

32PIN TSOP(PLASTIC)



NOTE: *NOT INCLUDE MOLD FINIS.

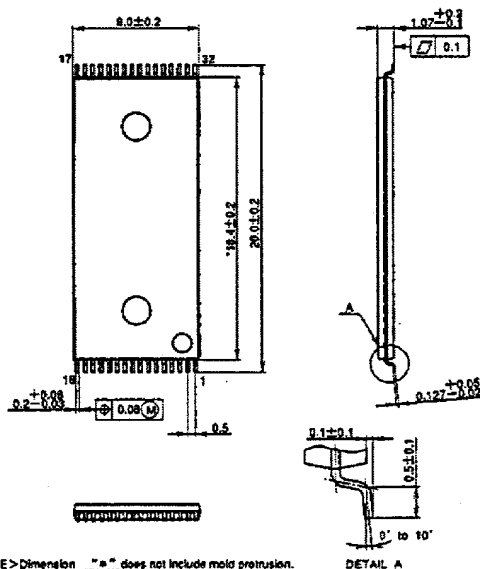
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EIAJ CODE	TSOP032-P-0820-A
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.3g

CXK581000AYM

32PIN TSOP(PLASTIC)



NOTE: *Dimension "a" does not include mold protrusion.

SONY CODE	TSOP-32P-L01A
EIAJ CODE	TSOP032-P-0820-B
JEDEC CODE	

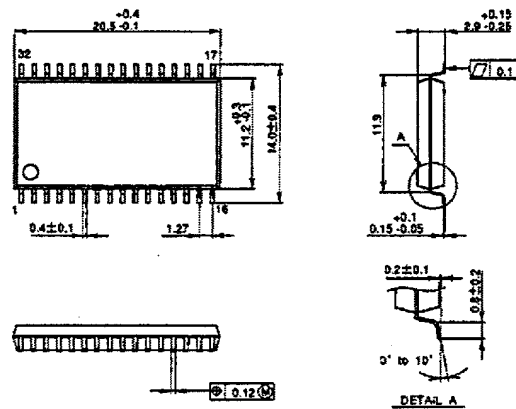
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.3g

Package Outline Unit : mm

CXXK581000AM

32PIN SOP(PLASTIC) 525MIL



PACKAGE STRUCTURE

SONY CODE	SOP-32P-L02
EIAJ CODE	*SOP032-P-0525-A
JEDEC CODE	—

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	1.2g