ANALOG DEVICES

Programmable Clock Generator

AD730

FEATURES

16 Selectable Frequencies
  216 MHz max ECL Output
  54 MHz max TTL Output
Low Output Jitter
Low Cost
Mask Programmable Frequencies
Single Reference Crystal or TTL Clock
Standard MPU Interface
Bt458 Compatible Reset
+5 Volt Supply
20-Pin SOIC Packaging

PRODUCT DESCRIPTION

The AD730 Programmable Clock Generator is a monolithic solution for providing up to 16 output frequencies. Output frequencies of greater than 216 MHz are realizable, combined with excellent jitter performance. The available output frequencies are determined through a "Personalization Mask Option." The AD730-1 has been personalized to provide the following frequencies with a 6.75 MHz reference crystal:

47.25 MHz	54.00 MHz
64.125 MHz	74.250 MHz
94.50 MHz	108.00 MHz
118.125 MHz	135.00 MHz
189.00 MHz	216.00 MHz

Other frequencies may be personalized on an AD730 using the following algorithm:

$$f_{OUT} = f_{REF}\frac{M}{N}$$

where: $N = 1$ or 2
$M = 1$ to 64

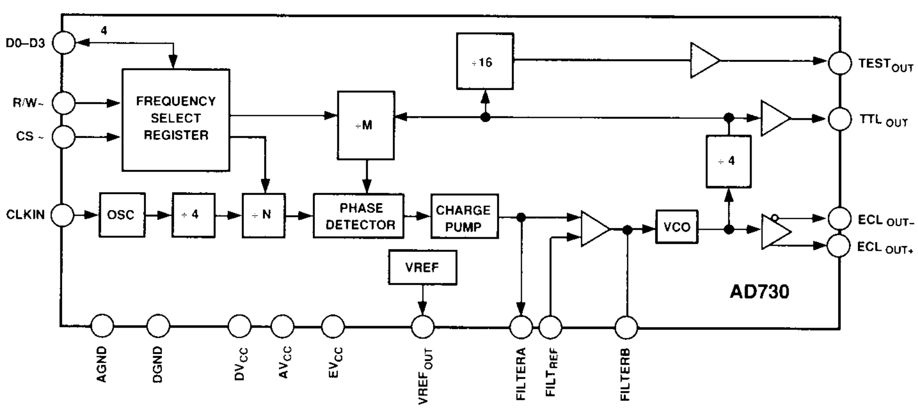
The output frequency is selected through a standard MPU interface. When selecting a new frequency, the ECL output is glitch free during the transition. To ensure compatibility with video DACs, the AD730 provides pipeline setup sequencing during frequency select switching. In addition to supplying the ECL output clock frequency, the AD730 provides a divide by 4 and divide by 64 TTL outputs.

Low jitter and excellent power supply rejection are achieved by careful attention to layout and the use of an active integrator in the loop filter. The only external components required are a reference crystal and three passive components for the PLL loop filter.

The AD730 will be available in a 20-pin SOIC package and is specified to operate over the 0°C to +70°C commercial temperature range. However, evaluation samples are available in a 20-pin side brazed package.

7

FUNCTIONAL BLOCK DIAGRAM



This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD730—SPECIFICATIONS

PROGRAMMABLE CLOCK GENERATOR (0°C ≤ T_A ≤ 70°C, 4.65 ≤ V_{CC} ≤ 5.25)

Parameter	Conditions	Min	Typ	Max	Units
CLOCK FREQUENCY (ECL)	See Note 1				
Jitter	f_{OUT} = 47.25 MHz (divide ratios = 28/4)		250	500	ps rms
Jitter	f_{OUT} = 54.00 MHz (divide ratios = 32/4)		250	500	ps rms
Jitter	f_{OUT} = 94.50 MHz (divide ratios = 56/4)		175	350	ps rms
Jitter	f_{OUT} = 108.00 MHz (divide ratios = 64/4)		175	350	ps rms
Jitter	f_{OUT} = 118.125 MHz (divide ratios = 140/8)		175	350	ps rms
Jitter	f_{OUT} = 135.00 MHz (divide ratios = 80/4)		175	350	ps rms
Jitter	f_{OUT} = 189.00 MHz (divide ratios = 112/4)		125	250	ps rms
Jitter	f_{OUT} = 216.00 MHz (divide ratios = 128/4)		125	250	ps rms
Jitter	f_{OUT} = 64.125 MHz (1024 × 768 @ 60 Hz)		250	500	ps rms
Jitter	f_{OUT} = 74.250 MHz (1024 × 768 @ 70 Hz)		250	500	ps rms
CLOCK FREQUENCY (TTL)[1]					
Jitter	1/4 Frequency of ECL Clock		250		ps rms
REFERENCE CLOCK INPUT					
Input Frequency			6.75		MHz
V_{IH}		2.0			V
V_{IL}				0.8	V
REFERENCE VOLTAGE[2]					
Output Voltage		1.215		1.255	V
Max Source Current		1.0			mA
Max Sink Current		300			µA
CLOCK OUTPUT (ECL)					
V_{OH}	See Note 3	4.04		4.19	V
V_{OL}	See Note 3	3.15		3.35	V
I_{OH}		10.5			mA
Rise Time	See Note 3	1.3		2.0	ns
Fall Time	See Note 3	1.3		2.0	ns
Duty Cycle Asymmetry	See Note 3	−10		+10	%
Output Frequency Range		47.25		216	MHz
CLOCK OUTPUT (TTL)					
V_{OH}		2.4			V
V_{OL}				0.4	V
I_{OL}				−2.0	mA
Rise Time	See Note 4			4	ns
Fall Time	See Note 4			4	ns
Duty Cycle Asymmetry	See Note 4	−20		+20	%
Output Frequency Range		11.8		54	MHz
CONTROL BUS LOGIC	CS~, D0, D1, D2, D3, R/W~				
V_{IH}		2.0			V
V_{IL}				0.8	V

NOTES

[1]a. Jitter is measured by triggering on the output clock, delayed 16 µs and then measuring the time period from the trigger edge to the next edge of the output clock after the delay. This measurement is repeated multiple times and then the RMS value is determined.

[1]b. The V_{CO} gain is 100 MHz/V (±40% tolerance). The charge pump current is 200 µA peak.

[2]The reference voltage will be trimmed within limits specified at Trim & Probe. However, we are not certain if these limits can be maintained when the part has been packaged. Initial silicon samples will determine what limits are achievable.

[3]ECL Output specifications are determined with the following load conditions: each output has a 330 Ω pull-down resistor to ground and a 220 Ω pull-up resistor to V_{CC}.

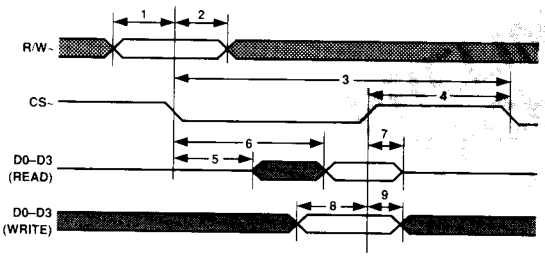
[4]TTL output rise time/fall time is determined with a 10 pF load. Rise time/fall time is defined as the 10% to 90% point.

Specifications subject to change without notice.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

TIMING (0°C ≤ T_A ≤ 70°C, 4.65 ≤ V_{CC} ≤ 5.25)

Parameter	Conditions	Min	Typ	Max	Units
TIMING					
R/W~ Setup Time	Timing Diagram – 1	0			ns
R/W~ Hold Time	Timing Diagram – 2	15			ns
CS~ Low + High Time	Timing Diagram – 3	70			ns
CS~ High Time	Timing Diagram – 4	25			ns
CS~ Asserted to Data Driven	Timing Diagram – 5	10			ns
CS~ Asserted to Data Valid	Timing Diagram – 6			75	ns
CS~ Negated to Data Tristated	Timing Diagram – 7			25	ns
Write Data Setup Time	Timing Diagram – 8	35			ns
Write Data Hold Time	Timing Diagram – 9	0			ns



Timing Diagram

ORDERING GUIDE

Model	Description	Package Option*
AD730JR-1	Wide Body 20-Pin SOIC	R-20

*For outline information see Package Information section.

POWER SUPPLIES (0°C ≤ T_A < 70°C, 4.5 V ≤ V_{CC} ≤ 5.5 V)

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage V_{CC}		4.5	5	5.5	V
Quiescent Current I_{CC}			62		mA
Power Dissipation			310		mW

ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage V_{CC}				7.5	V
Storage Temperature Range		–65		150	°C
Operating Temperature Range[2]		0		70	°C
Lead Temperature Range	Soldering 60 Sec			300	°C

NOTES

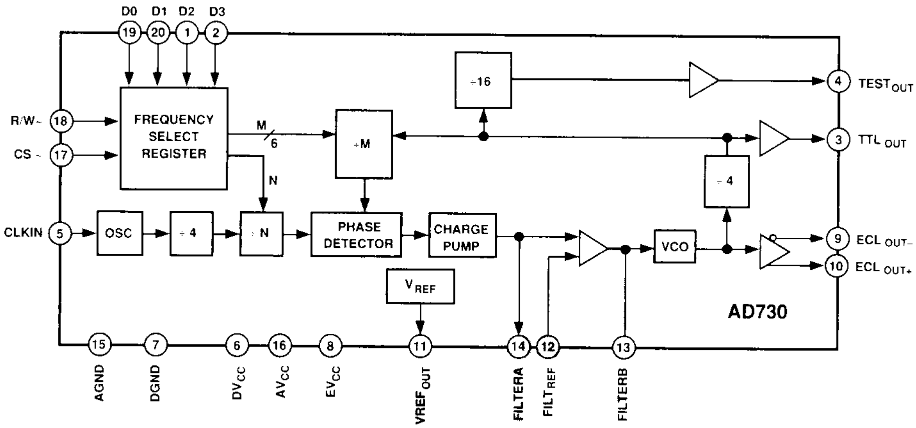
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other condition above those indicated in the operational section of this specification is not implied. Exposure to absolute rating conditions for extended period may affect device reliability.

[2]20-pin SOIC package θ_{JA} = 100°C/W.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

FREQUENCY SELECT REGISTER ASSIGNMENTS

D3	D2	D1	D0	f_{OUT} ECL	f_{OUT} TTL
0	0	0	0	47.25	11.8125 MHz
0	0	0	1	54.00	13.50 MHz
0	0	1	0	94.50	23.625 MHz
0	0	1	1	108.00	27.00 MHz
0	1	0	0	118.125	29.53 MHz
0	1	0	1	135.00	33.75 MHz
0	1	1	0	189.00	47.25 MHz
0	1	1	1	216.00	54.00 MHz
1	0	0	0	64.125	16.031 MHz
1	0	0	1	74.250	18.5625 MHz
1	0	1	0	undefined	undefined
1	0	1	1	undefined	undefined
1	1	0	0	undefined	undefined
1	1	0	1	undefined	undefined
1	1	1	0	undefined	undefined
1	1	1	1	OSCILLATOR STOPPED	



PIN ASSIGNMENTS

Pin	Description		I/O Type	Application Notes
01	D2	Frequency Select Bit 2	TTL I/O	2nd MSB of four frequency select pins.
02	D3	Frequency Select Bit 3	TTL I/O	MSB of four frequency select pins.
03	TTL_{OUT}	TTL Clock Output	TTL Output	TTL output frequency is one quarter of ECL output frequency. Output is actively driven high and low. It does not require a pull-up resistor.
04	$TEST_{OUT}$	Test Output	TTL Output	This is the ECL output divided by 64. Allows for in-circuit functional testing.
05	CLKIN	Crystal Oscillator Input	TTL Input	6.75 MHz Reference Crystal or Crystal Oscillator.
06	DV_{CC}	Digital V_{CC}	Power	V_{CC} for CMOS logic and TTL output.
07	DGND	Digital Ground	Power	Ground for CMOS logic and TTL output.
08	EV_{CC}	ECL V_{CC}	Power	V_{CC} for ECL Clock Output. Decoupling with 0.1 μF∥0.01 μF required.
09	ECL_{OUT-}	ECL clock output (negative)	ECL Output	ECL output referenced to V_{CC}.
10	ECL_{OUT+}	ECL clock output (positive)	ECL Output	ECL output referenced to V_{CC}.
11	V_{REFOUT}	1.235 V Bandgap Reference	Analog	Voltage reference for video DAC.
12	$FILT_{REF}$	Loop Filter Reference	Analog	An external capacitor allows adjustment for optimal loop noise performance.
13	FILTERB	PLL Filter	Analog	External loop filter. Apply PLL filter to FILTERB.
14	FILTERA	PLL Filter	Analog	External loop filter. Apply PLL filter to FILTERA.
15	AGND	Analog Ground	Power	Ground for PLL.
16	AV_{CC}	Analog V_{CC}	Power	V_{CC} for PLL. Decoupling with 0.1 μF∥0.01 μF required.
17	CS~	Chip Select	TTL Input	Negative edge latches state R/W~. Positive edge latches state of D0, D1, D2, D3.
18	R/W~	Read or Write to Data Bus	TTL Input	State is latched on negative CS~. Low for writing to and high for reading from the frequency select register.
19	D0	Frequency Select Bit 0	TTL I/O	LSB of four frequency select pins.
20	D1	Frequency Select Bit 1	TTL I/O	2nd LSB of four frequency select pins.

7

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

THEORY OF OPERATION

START-UP OPERATION

An internal power on reset function is provided in the AD730. Upon power-up, the device will reset to a fixed output frequency. This frequency is the lowest frequency output available −47.25 MHz. This frequency can also be obtained during normal operation by loading an all "0"s pattern (D0–D3) into the frequency select register.

CONTROL INTERFACE

The timing and operation of the digital interface is defined as the standard MPU interface. The state of the R/W~ signal is latched on the falling edge of CS~. This determines whether one is reading the current selected output frequency from the device or writing a new output frequency to the device. During a read operation, on the falling edge of CS~, the content of the frequency select register is driven onto the four data lines (D0–D3). On the rising edge of CS~, while writing, the four data inputs (D0–D3) are latched into the frequency select register. The content of the frequency select register determines which one of sixteen possible output frequencies will be generated. The AD730–1 has only ten frequencies that are defined in the device (see Frequency Select Register Assignments Table).

RESET FUNCTION

Two programmed reset modes are supported. The first reset is invoked by loading an all "1"s pattern (D0–D3) into the frequency select register. This reset function causes the main PLL oscillator to synchronously halt with the ECL output in the high state. When the frequency select register reprogrammed to a valid output frequency (see Frequency Select Register Assignments Table), the oscillator is released. Short duration clock half- cycles are avoided, both when entering and leaving this reset mode.

The second reset occurs each time the frequency select register is reprogrammed to a new frequency. This reset is intended to set the pipeline delay of the Bt458 video DAC. When a new frequency is programmed, the ECL_{OUT+} and ECL_{OUT-} are stopped with the ECL_{OUT+} high and $ECL_{OUT}(-)$ low for four rising edges of the TTL_{OUT} clock. On the fourth rising edge of the TTL_{OUT} clock, the ECL_{OUT} clock is synchronously released (see Figure 1).

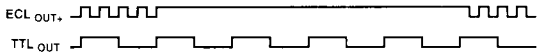


Figure 1.

REFERENCE CLOCK INPUT

The reference clock input, CLKIN, will accept either a standard TTL input or serve as a single pin oscillator by applying a <10 MHz crystal.

CLOCK OUTPUTS

The clock output is an ECL output, referenced to V_{CC}, that is capable of operating up to 216 MHz. This output contains circuitry that provides a smooth transition during changes in the output frequency. Specifically, in order to prevent a short cycle from occurring, the circuit checks the state of the output when a new frequency is written to the device in order to prevent a short cycle from occurring during frequency transitions. When the output reaches the correct state, a glitch free transition in frequency occurs.

TTL compatible, divide by 4 and 64, outputs are also provided, TTL_{OUT} and $TEST_{OUT}$ respectively.

GROUNDING

Proper grounding and decoupling should be a primary design objective when working with PLL circuits. Separate analog and digital supplies are present on chip, but it is recommended that there be one common analog and digital ground plane. This approach is less difficult to design, and it will produce good results. Decoupling of the analog power pins (Pins 8 and 16) should contain a 0.1 μF capacitor in parallel with a 0.01 μF capacitor.

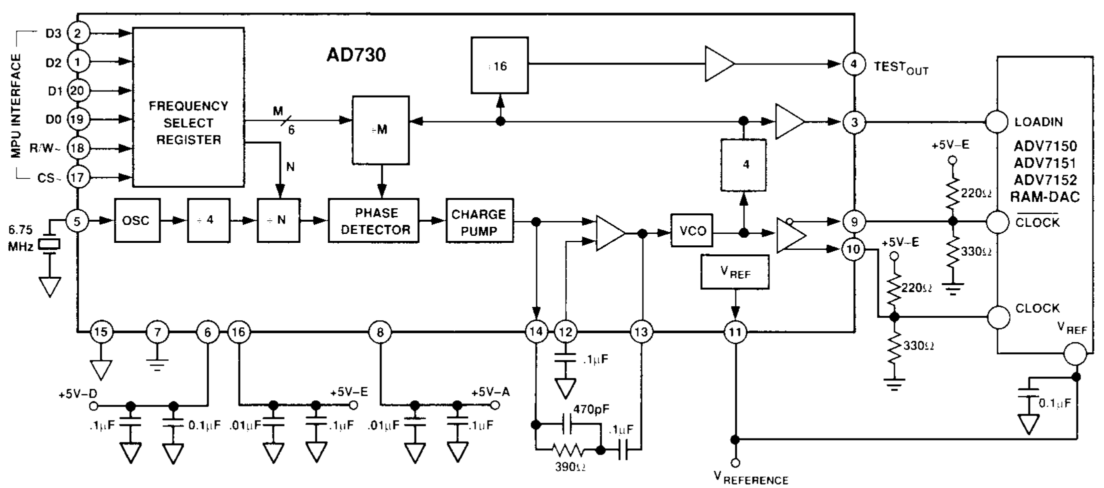


Figure 2. Typical Application

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.