ANALOG DEVICES

Complete High Speed 12-Bit Monolithic D/A Converter

ANALOG DEVICES INC

AD565A

1.1 Scope.

This specification covers the detail requirements for a precision, high speed, current output 12-bit resolution D/A converter with internal high stability buried Zener reference.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD565ASD/883B
−2	AD565ATD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: D-24.

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

V_{CC} to Power Ground . . . . . 0 to +18V
V_{EE} to Power Ground . . . . . 0 to −18V
Voltage on DAC Output (Pin 9) . . . . . −3V to +12V
Digital Inputs (Pins 13 to 24) to Power Ground . . . . . −1.0V to +7.0V
Ref In to Reference Ground . . . . . ±12V
Bipolar Offset to Reference Ground . . . . . ±12V
10V Span R to Reference Ground . . . . . ±12V
20V Span R to Reference Ground . . . . . ±24V
Ref Out . . . . . Indefinite Short to Power Ground
Momentary Short to V_{CC}
Power Dissipation 1000mW
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 25°C/W
θ_{JA} = 48°C/W

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Table 1.

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1]	Units
Relative Accuracy	RA	−1	1/2	1/2	3/4		All Bits with Positive Errors On. All Bit with Negative Errors On.	± LSB max
		−2	1/4	1/2	1/2	1/4		
Differential Nonlinearity	DNL	−1	3/4	3/4	1		Major Transitions	± LSB max
		−2	1/2	3/4	1	1/2		
Gain Error	A_E	−1, 2	0.25	0.25			R_{REF} = 50Ω Fixed	± % of FS max
Gain Error Temperature Coefficient	TCA_E	−1			30			± ppm of FS/ °C max
		−2			15			
Offset Error	V_{OS}	−1, 2	0.05	0.05				± % of FS max
Offset Error Temperature Coefficient	TCV_{OS}	−1, 2			2			± ppm of FS/ °C max
Bipolar Zero Error[2]	B_{PZE}	−1	0.15	0.15			R_{BO} = 50Ω Fixed	± % of FS max
		−2	0.10	0.15		0.10		
B/P Zero Error Temperature[2] Coefficient	TCB_{PZE}	−1, 2			10			± ppm of FS/ °C max
Input Resistance	R_{IN}	−1, 2	15					kΩ min
			25					kΩ max
Reference Output Voltage[3]	V_{REF}	−1, 2	9.90	9.90	9.90			+ V min
			10.10	10.10	10.10			+ V max
Reference Output Current[4]	I_{REF}	−1, 2	1.5	1.5				+ mA min
Full Scale Transition	t_{FS}	−1, 2	30				10% to 90% Delay Plus Rise Time	ns max
		−1, 2	50				90% to 10% Delay Plus Fall Time	ns max
Output Current Settling Time	t_{SL}	−1, 2	250					ns max
Compliance Voltage	CV	−1, 2	1.5				−55°C to +125°C	− V min
			10					+ V max
Output Resistance	R_{OUT}	−1, 2	6				Exclusive of Span Resistors	kΩ min
			10					kΩ max
Output Current	I_{OUT}	−1, 2	1.6	1.6			Unipolar (All Bits On)	− mA min
			2.4	2.4				− mA max
			0.8	0.8			Bipolar (All Bits On)	− mA min
			1.2	1.2				− mA max
Power Supply Rejection Ratio	PSRR	−1, 2	10	10			V_{CC} = +11.4V to +16.5V dc	± ppm of FSR/ % max
			25	25			V_{EE} = −11.4V to −16.5V dc	
Power Supply Current[4,5]	I_{CC}	−1, 2	5	5				+ mA max
	I_{EE}	−1, 2	18	18				− mA max
Power Dissipation	P_D	−1, 2	345	345				mW max
Digital Input High Voltage	V_{IH}	−1, 2	2.0	2.0				+ V min
			5.5	5.5				+ V max
Digital Input Low Voltage	V_{IL}	−1, 2	0.8	0.8				+ V max
Digital Input High Current	I_{IH}	−1, 2	300	300			V_{IH} = 5.5V	+ μA max
Digital Input Low Current	I_{IL}	−1, 2	100	100			V_{IL} = 0V	+ μA max

NOTES

[1] V_{CC} = +15V, V_{EE} = −15V, V_{IH} = 2.0V, V_{IL} = 0.8V, T_A = 25°C unless otherwise indicated. V_{IH} = 2.0V, and V_{IL} = 0.8V guaranteed design limits at −55°C and +125°C.

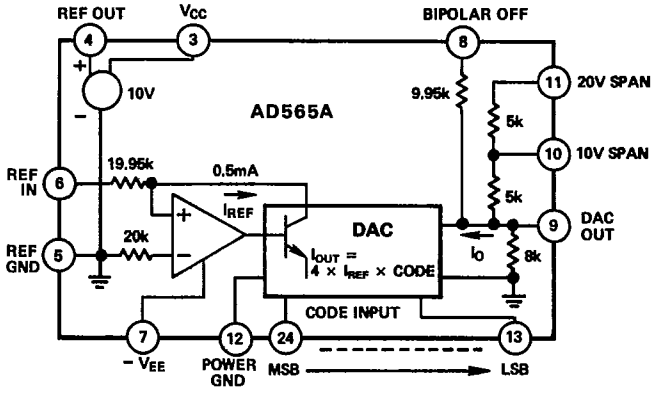
[2] MSB on; all other bits off.

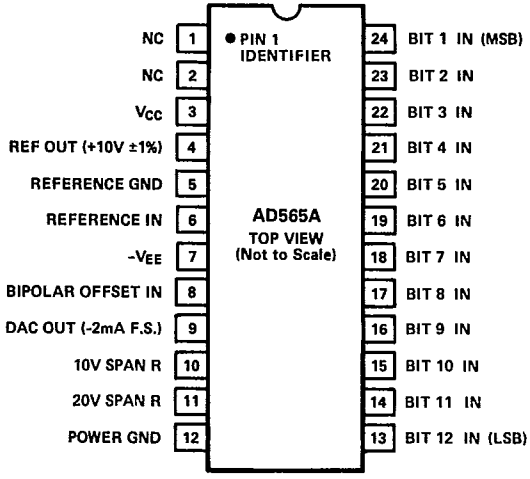
[3] In subgroup 1, the reference output is loaded with 0.5mA reference input current, 1.0mA bipolar offset current, and 1.5mA additional current. In subgroups 2 and 3, only the 0.5mA reference input current is applied. The reference must be buffered to supply external loads at elevated temperatures.

[4] Guaranteed for $+11.4 \leq V_{CC} \leq +16.5V$.

[5] Guaranteed for $-11.4 \geq V_{EE} \geq -16.5V$.

3.2.1 Functional Block Diagram and Terminal Assignments.





3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (56).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).