REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET	35	36	37	38	39	40	41	42	43	44									
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
98-12-11

REVISION LEVEL

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, HCMOS, VLSI, INTEGRATED MULTIPROTOCOL PROCESSOR, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-93159

SHEET 1 OF 44

DSCC FORM 2233
APR 97

5962-E073-99

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

5962	-	93159	01	Q	X	X
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)
\		/				
Drawing number						

1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	68302	Integrated multiprotocol processor

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA5-P132	132	Pin grid array
Y	See figure 1	132	Ceramic leaded chip carrier, gullwing-lead

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{DD})	-0.3 V to +7.0 V
Input voltage range (V_{IN})	-0.3 V to V_{CC}
Storage temperature range (T_{STG})	-55°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-ambient (Θ_{JA}):	
Case X	33°C/W
Case Y	46°C/W
Power dissipation at 16.67 MHz (P_D)	53 mA minimum to 64 mA maximum 2/
Power dissipation at 8.0 MHz (P_D)	26 mA minimum to 31 mA maximum 2/
Low power dissipation at 16.67 MHz (LP_D)	36 mA maximum 3/
Lowest power dissipation at 16.67 MHz (LP_D)	32 mA maximum 4/
Lowest power dissipation at 50.0 kHz (LP_D)	1 mA maximum 5/

1.4 Recommended operating conditions. 2/

Supply voltage range (V_{DD})	+4.5 V dc to +5.5 V dc
High level input voltage (V_{IH}):	
Except EXTAL	2.0 V minimum
EXTAL	4.0 V minimum
(NMSI1 in IDL mode) L1CLK, L1SY1, L1RXD, L1GR	V_{DD} - 20%
Low level input voltage (V_{IL}):	
Except EXTAL	0.8 V maximum
EXTAL	0.6 V maximum
(NMSI1 in IDL mode) L1CLK, L1SY1, L1RXD, L1GR	$0.2V_{DD}$
Frequency of operation	8 - 16.67 MHz
Ambient operating temperature range (T_A)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 6/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ The values shown are typical. The typical value varies as shown, based on how many IMP on-chip peripherals are enabled and the rate at which they are clocked.
3/ LPREC = 0, Divider = 2.
4/ LPREC = 1, Divider = 1024.
5/ The stated frequency must be externally applied to EXTAL only after the IMP has been placed in the lowest power mode with LPREC = 1. The device core is not specified to operate at frequency but the rest of the IMP is. In this configuration, the user does not divide the clock internally using the LPCD4-LPCD0 bits in the system control register.
6/ Values will be added when they become available.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagrams. The functional block diagrams shall be as specified on figure 3.

3.2.4 Timing waveforms. The timimg waveforms shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125EC, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions $-55°C \le T_A \le +125°C$ 1/ $+4.5\ V \le V_{DD} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{DD} = 5.0 V I_{OH} = 400 µA	All	1, 2, 3	V_{DD} - 1.0		V
Low level output voltage, A1-A23, PB0-PB11, FC0-FC2, $\overline{CS1}$ - $\overline{CS0}$, IAC, $\overline{AVEC}$, $\overline{BG}$, RCLK1-RCLK3, TCLK1-TCLK3, $\overline{RTS1}$ - $\overline{RTS3}$, SDS2, PA12, RXD2, RXD3, $\overline{CTS2}$, $\overline{CD2}$, $\overline{CD3}$, $\overline{DREQ}$	V_{OL1}	V_{DD} = 5.0 V I_{OL} = 3.2 mA	All	1, 2, 3		0.5	
Low level output voltage, $\overline{AS}$, $\overline{UDS}$, $\overline{LDS}$, R/$\overline{W}$, $\overline{BERR}$, $\overline{BGACK}$, $\overline{BCLR}$, $\overline{DTACK}$, $\overline{DACK}$, $\overline{RMC}$, D0-D15, $\overline{RESET}$	V_{OL2}	V_{DD} = 5.0 V I_{OL} = 5.3 mA	All	1, 2, 3		0.5	
Low level output voltage, TXD1, TXD2, TXD3	V_{OL3}	V_{DD} = 5.0 V I_{OL} = 7.0 mA	All	1, 2, 3		0.5	
Low level output voltage, $\overline{BR}$, $\overline{DONE}$, $\overline{HALT}$ ($\overline{BR}$ as output)	V_{OL4}	V_{DD} = 5.0 V I_{OL} = 8.9 mA	All	1, 2, 3		0.5	
Low level output voltage, CLKO	V_{OL5}	V_{DD} = 5.0 V I_{OL} = 3.2 mA	All	1, 2, 3		0.4	
Input leakage current	I_{IN}	V_{DD} = 5.5 V	All	1, 2, 3		20	µA
Three-state leakage current	I_{TSI}	V_{DD} = 5.5 V, V_{IN} = V_{DD}	All	1, 2, 3		20	
Open drain leakage current	I_{OD}	V_{DD} = 5.5 V, V_{IN} = V_{DD}	All	1, 2, 3		20	
Output drive: CLKO	O_{CLK}		All	1, 2, 3		50	pF
Output drive: ISDN I/F (GCI mode)	O_{GCI}					150	
Output drive: All other pins	O_{ALL}					130	
Input capacitance	C_{IN}	See 4.4.1c	All	4		15	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol or Test no.	Test conditions $-55°C \le T_A \le +125°C$ 1/ $+4.5\ V \le V_{DD} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
NMSI1 in IDL mode							
High level output voltage, L1TXD, SDS1, SDS2, L1RQ	V_{OH2}	V_{DD} = 5.0 V I_{OH} = 2.0 mA	All	1, 2, 3	V_{DD} - 0.5		V
Low level output voltage, L1TXD, SDS1, SDS2, L1RQ	V_{OL6}	V_{DD} = 5.0 V I_{OH} = 2.0 mA	All	1, 2, 3		0.5	V
Low level input current	I_{IL}	$V_{IN} = V_{SS}$	All	1, 2, 3		±10	: A
High level input current	I_{IH}	$V_{IN} = V_{DD}$	All	1, 2, 3		±10	: A
Functional tests		See 4.4.1b	All	7, 8			
Clock timing							
Clock period (EXTAL)	1	See figure 4	All	9, 10, 11	60	125	ns
Clock pulse width (EXTAL)	2,3				27	62.5	
Clock rise and fall time (EXTAL)	4,5					5	
EXTAL to CLKO delay 2/ 3/	5A				2	18	
IMP bus master cycles							
Clock high to FC, address valid	6	See figure 4	All	9, 10, 11		45	ns
Clock high to address, data bus high impedance (maximum)	7					50	
Clock high to address, FC invalid (minimum)	8				0		
Clock high to $\overline{AS}$, $\overline{DS}$ asserted 4/	9				3	30	
Address, FC valid to $\overline{AS}$, $\overline{DS}$ asserted (read)/ $\overline{AS}$ asserted (write) 5/	11				15		
Clock low to $\overline{AS}$, $\overline{DS}$ negated 4/	12					30	
$\overline{AS}$, $\overline{DS}$ negated to address, FC invalid 5/	13				15		
$\overline{AS}$ (and $\overline{DS}$ read) width asserted 5/	14				120		
$\overline{DS}$ width asserted, write 5/	14A				60		
$\overline{AS}$, $\overline{DS}$ width negated 5/	15				60		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Test conditions $-55°C \le T_A \le +125°C$ 1/ $+4.5\ V \le V_{DD} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
IMP bus master cycles – Continued							
Clock high to control bus high impedance	16	See figure 4	All	9, 10, 11		50	ns
$\overline{AS}$, $\overline{DS}$ negated to R/$\overline{W}$ invalid 5/	17				15		
Clock high to R/$\overline{W}$ high 4/	18					30	
Clock high to R/$\overline{W}$ low 4/	20					30	
$\overline{AS}$ asserted to R/$\overline{W}$ low (write) 5/ 9/	20A					10	
Address FC valid to R/$\overline{W}$ low (write) 5/	21				15		
R/$\overline{W}$ low to $\overline{DS}$ asserted (write) 5/	22				30		
Clock low to data-out valid	23					30	
$\overline{AS}$, $\overline{DS}$ negated to data-out invalid (write) 5/	25				15		
Data-out valid to $\overline{DS}$ asserted (write) 5/	26				15		
Data-in valid to clock low (setup time on read) 8/	27				7		
$\overline{AS}$, $\overline{DS}$ negated to $\overline{DTACK}$ negated (asynchronous hold) 5/	28				0	110	
$\overline{AS}$, $\overline{DS}$ negated to data-in invalid (hold time on read)	29				0		
$\overline{AS}$, $\overline{DS}$ negated to $\overline{BERR}$ negated	30				0		
$\overline{DTACK}$ asserted to data-in valid (setup time) 5/ 8/	31					50	
$\overline{HALT}$ and $\overline{RESET}$ input transition time	32					150	
Clock high to $\overline{BG}$ asserted	33					30	
Clock high to $\overline{BG}$ negated	34					30	
$\overline{BR}$ asserted to $\overline{BG}$ asserted	35				2.5	4.5	clks
$\overline{BR}$ negated to $\overline{BG}$ negated 10/	36				1.5	2.5	
$\overline{BGACK}$ asserted to $\overline{BG}$ negated	37				2.5	4.5	
$\overline{BGACK}$ asserted to $\overline{BR}$ negated 11/	37A				10	1.5	ns/clks

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Test conditions $-55°C \le T_A \le +125°C$ 1/ $+4.5\ V \le V_{DD} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
IMP bus master cycles – Continued							
$\overline{BG}$ asserted to control, address, data bus impedance ($\overline{AS}$ negates)	38	See figure 4	All	9, 10, 11		50	ns
$\overline{BG}$ width negated	39				1.5		clks
$\overline{AS}$, $\overline{DS}$ negated to $\overline{AVEC}$ negated	44				0	50	ns
$\overline{BGACK}$ width low	46				1.5		clks
Asynchronous input setup time 8/	47				10		ns
$\overline{BERR}$ asserted to $\overline{DTACK}$ asserted 5/ 6/	48				10		
Data-out hold from clock high	53				0		
R/ $\overline{W}$ asserted to data bus impedance change	55				0		
$\overline{HALT}$ / $\overline{RESET}$ pulse width 7/	56				10		clks
$\overline{BGACK}$ negated to $\overline{AS}$, $\overline{DS}$, R/ $\overline{W}$ driven	57				1.5		
$\overline{BGACK}$ negated to FC	57A				1		
$\overline{BR}$ negated to $\overline{AS}$, $\overline{DS}$, R/ $\overline{W}$ driven 10/	58				1.5		
$\overline{BR}$ negated to FC 10/	58A				1		
Clock high to $\overline{BCLR}$ asserted	60					30	ns
Clock high to $\overline{BCLR}$ negated 13/	61					30	
Clock low (S0 falling edge during read) to $\overline{RMC}$ asserted	62					30	
Clock high (S7 rising edge during write) to $\overline{RMC}$ negated	63					30	
$\overline{RMC}$ negated to $\overline{BG}$ asserted 12/	64					30	
DMA 17/							
$\overline{DREQ}$ asynchronous setup time 14/	80	See figure 4	All	9, 10, 11	15		ns
$\overline{DREQ}$ width low 15/	81				2		clks
$\overline{DREQ}$ low to $\overline{BR}$ low 16/	82					2	
Clock high to $\overline{BR}$ low 16/	83					30	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Test conditions $-55°C \le T_A \le +125°C$ 1/ $+4.5\ V \le V_{DD} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
DMA - Continued 17/							
Clock high to $\overline{BR}$ high impedance 16/	84	See figure 4	All	9, 10, 11		30	ns
$\overline{BGACK}$ low to $\overline{BR}$ high impedance 16/	85				30		
Clock high to $\overline{BGACK}$ low	86					30	
$\overline{AS}$ and $\overline{BGACK}$ high (the latest one) to $\overline{BGACK}$ low (when $\overline{BG}$ is asserted)	87				1.5	2.5 + 30	clks ns
$\overline{BG}$ low to $\overline{BGACK}$ low (no other bus master) 16/	88				1.5	2.5 + 30	clks ns
$\overline{BR}$ high impedance to $\overline{BG}$ high 16/	89				0		ns
Clock on which $\overline{BGACK}$ low to clock on which $\overline{AS}$ low	90				2	2	clks
Clock high to $\overline{BGACK}$ high	91					30	ns
Clock low to $\overline{BGACK}$ high impedance	92					15	
Clock high to $\overline{DACK}$ low	93					30	
Clock low to $\overline{DACK}$ high	94					30	
Clock high to $\overline{DONE}$ low output)	95					30	
Clock low to $\overline{DONE}$ high (impedance)	96					30	
$\overline{DONE}$ input low to clock high (asynchronous setup)	97				15		
External master internal asynchronous read/write cycles							
R/$\overline{W}$ valid to $\overline{DS}$ low	100	See figure 4	All	9, 10, 11	0		ns
$\overline{DS}$ low to data in valid	101					30	
$\overline{DTACK}$ low to data in hold time	102				0		
$\overline{AS}$ valid to $\overline{DS}$ low	103				0		
$\overline{DTACK}$ low to $\overline{DS}$ high	104				0		
$\overline{DS}$ high to $\overline{DTACK}$ high	105					45	
$\overline{DS}$ inactive to $\overline{AS}$ inactive	106				0		
$\overline{DS}$ high to R/$\overline{W}$ high	107				0		
$\overline{DS}$ high to data high impedance	108					45	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Test conditions $-55°C \le T_A \le +125°C$ 1/ $+4.5\ V \le V_{DD} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
External master internal asynchronous read/write cycles - Continued							
$\overline{DS}$ high to data out hold time 18/	108A	See figure 4	All	9, 10, 11	0		ns
$\overline{DS}$ high to data in hold time	109				0		
Data out valid to $\overline{DTACK}$ low	109A				15		
External master internal synchronous read/write cycles 19/							
Address valid to $\overline{AS}$ low	110	See figure 4	All	9, 10, 11	15		ns
$\overline{AS}$ low to clock high	111				30		
Clock low to $\overline{AS}$ high	112					45	
$\overline{AS}$ high to address hold time on write	113				0		
$\overline{AS}$ inactive time	114				1		clk
$\overline{UDS}$ / $\overline{LDS}$ low to clock high	115				40		ns
Clock low to $\overline{UDS}$ / $\overline{LDS}$ high	116					45	
R/ $\overline{W}$ valid to clock high	117				30		
Clock high to R/ $\overline{W}$ high	118					45	
$\overline{AS}$ low to IAC high	119					40	
$\overline{AS}$ high to IAC low	120					40	
$\overline{AS}$ low to $\overline{DTACK}$ low (0 wait state)	121					45	
Clock low to $\overline{DTACK}$ low (1 wait state)	122					30	
$\overline{AS}$ high to $\overline{DTACK}$ high	123					45	
$\overline{DTACK}$ high to $\overline{DTACK}$ high impedance	124					15	
Clock high to data out valid	125					30	
$\overline{AS}$ high to data high impedance	126					45	
$\overline{AS}$ high to data out hold time	127				0		
$\overline{AS}$ high to address hold time on read	128				0		
$\overline{UDS}$ / $\overline{LDS}$ inactive time	129				1		clk
Data in valid to clock low	130				30		ns
Clock low to data in hold time	131				15		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Test conditions $-55°C \le T_A \le +125°C$ 1/ $+4.5\ V \le V_{DD} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Internal master internal read/write cycles							
Clock high to IAC high	140	See figure 4	All	9, 10, 11		40	ns
Clock low to IAC low	141					40	
Clock high to $\overline{DTACK}$ low (0 wait state)	142					45	
Clock low to $\overline{DTACK}$ high	143					40	
Clock high to data out valid	144					30	
$\overline{AS}$ high to data out hold time	145				0		
Chip-select timing internal master 22/							
Clock high to $\overline{CS}$, $\overline{IACK}$ low 20/	150	See figure 4	All	9, 10, 11		40	ns
Clock low to $\overline{CS}$, $\overline{IACK}$ high 20/	151					40	
$\overline{CS}$ width negated	152				60		
Clock high to $\overline{DTACK}$ low (0 wait state)	153					45	
Clock low to $\overline{DTACK}$ low (1-6 wait states)	154					30	
Clock low to $\overline{DTACK}$ high	155					40	
Clock high to $\overline{BERR}$ low 21/	156					40	
Clock low to $\overline{BERR}$ high impedance 21/	157					40	
$\overline{DTACK}$ high to $\overline{DTACK}$ high impedance	158					15	
Input data hold time from S6 low	171				5		
$\overline{CS}$ negated to data out invalid	172				10		
Address, FC valid to $\overline{CS}$ asserted	173				15		
$\overline{CS}$ negated to address, FC invalid	174				15		
$\overline{CS}$ low time (0 wait state)	175				120		
$\overline{CS}$ negated to R/$\overline{W}$ invalid	176				10		
$\overline{CS}$ asserted to R/$\overline{W}$ low (write)	177					10	
$\overline{CS}$ negated to data in invalid (hold time on read)	178				0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Test conditions $-55°C \le T_A \le +125°C$ 1/ $+4.5\ V \le V_{DD} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Chip-select timing external master							
Clock low to $\overline{DTACK}$ low (1-6 wait states)	154	See figure 4	All	9, 10, 11		30	ns
$\overline{AS}$ low to $\overline{CS}$ low	160					30	
$\overline{AS}$ high to $\overline{CS}$ high	161					30	
Address valid to $\overline{AS}$ low	162				15		
R/$\overline{W}$ valid to $\overline{AS}$ low 23/	163				15		
$\overline{AS}$ negated to address hold time	164				0		
$\overline{AS}$ low to $\overline{DTACK}$ low (0 wait state)	165					45	
$\overline{AS}$ high to $\overline{DTACK}$ high	167					30	
$\overline{AS}$ low to $\overline{BERR}$ low 24/	168					30	
$\overline{AS}$ high to $\overline{BERR}$ high 24/ 25/	169					30	
Parallel I/O							
Input data setup time (to clock low)	180	See figure 4	All	9, 10, 11	20		ns
Input data hold time (from clock low)	181				10		
Clock high to data out valid (CPU writes data, control, or direction)	182					35	
Interrupts 26/							
Interrupt pulse width low $\overline{IRQ}$ (edge triggered mode)	190	See figure 4	All	9, 10, 11	50		ns
Minimum time between edges	191				3		clks
Timers							
Timer input capture pulse width	200	See figure 4	All	9, 10, 11	50		ns
TIN clock low pulse width	201				50		
TIN clock high pulse width	202				2		clks
TIN clock cycles time	203				3		
Clock high to $\overline{TOUT}$ valid	204					35	ns
$\overline{FRZ}$ input setup time (to clock high) 27/	205				20		
$\overline{FRZ}$ input hold time (from clock high)	206				10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Test conditions $-55°C \le T_A \le +125°C$ 1/ $+4.5\ V \le V_{DD} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Serial communication port 29/							
SPCLK clock output period	250	See figure 4	All	9, 10, 11	4	64	clks
SPCLK clock output rise/fall time	251					15	ns
Delay from SPCLK to transmit 28/	252				0	40	
SCP receive setup time 28/	253				40		
SCP receive hold time 28/	254				10		
IDL timing							
L1CLK (IDL clock) frequency 30/	260	See figure 4	All	9, 10, 11		6.66	MHz
L1CLK width low	261				55		ns
L1CLK width high	262				60		
L1TXD, L1RQ, SDS1-SDS2 rising falling time	263					20	
L1SY1 (sync) setup time (to L1CLK falling edge)	264				30		
L1SY1 (sync) hold time (from L1CLK falling edge)	265				50		
L1SY1 (sync) inactive before 4th L1CLK	266				0		
L1TxD active delay (from L1CLK rising edge)	267				0	75	
L1TxD to high impedance (from L1CLK rising edge) 31/	268				0	50	
L1RxD setup time (to L1CLK falling edge)	269				50		
L1RxD hold time (from L1CLK falling edge)	270				50		
Time between successive IDL syncs	271				20		L1CLK
L1RQ valid before falling edge of L1SY1	272				1		
L1GR setup time (to L1SY1 falling edge)	273				50		ns
L1GR hold time (from L1SY1 falling edge)	274				50		
SDS1-SDS2 active delay from L1CLK rising edge	275				10	75	
SDS1-SDS2 inactive delay from L1CLK falling edge	276				10	75	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Test conditions $-55°C \le T_A \le +125°C$ 1/ $+4.5\ V \le V_{DD} \le +5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
GCI timing							
L1CLK GCI clock frequency (normal mode) 32/		See figure 4	All	9,10,11		512	kHz
L1CLK clock period normal mode 32/	280				1800	2100	ns
L1CLK width low/high normal mode	281				840	1450	
L1CLK rise/fall time normal mode 33/	282						
L1CLK (GCI clock) period (MUX mode) 32/						6.668	kHz
L1CLK clock period MUX mode 32/	280				150		ns
L1CLK width low/high MUX mode	281				55		
L1CLK rise/fall time MUX mode 33/	282						
L1SY1 sync setup time to L1CLK falling edge	283				30		
L1SY1 sync hold time from L1CLK falling edge	284				50		
L1TxD active delay (from L1CLK rising edge) 34/	285				0	100	
L1TxD active delay (from L1SY1 rising edge) 34/	286				0	100	
L1RxD setup time to L1CLK rising edge	287				20		
L1RxD hold time from L1CLK rising edge	288				50		
Time between successive L1SY1 in: Normal mode	289				64		L1CLK
Time between successive L1SY1 in: SCIT mode					192		
SDS1-SDS2 active delay from L1CLK rising edge 35/	290				10	90	ns
SDS1-SDS2 active delay from L1SY1 rising edge 35/	291				10	90	
SDS1-SDS2 inactive delay from L1CLK falling edge	292				10	90	
GCIDCL (GCI data clock) active delay	293				0	50	
PCM timing							
L1CLK (PCM clock) frequency 32/	300	See figure 4	All	9, 10, 11		6.66	MHz
L1CLK width low/high	301				55		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Test no.	Test conditions $-55°C \le T_A \le +125°C$ 1/ $+4.5\ V \le V_{DD} \le +5.5\ V$ unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
PCM timing – Continued								
L1SY0-L1SY1 setup time to L1CLK falling edge	302	See figure 4		All	9, 10, 11	20		ns
L1SY0-L1SY1 hold time from L1CLK falling edge	303					40		
L1SY0-L1SY1 width low	304					1		L1CLK
Time between successive sync signals (short frame)	305					8		
L1TxD data valid after L1CLK rising edge 36/	306					0	70	ns
L1TxD to high impedance (from L1CLK rising edge)	307					0	50	
L1RxD setup time (to L1CLK falling edge) 37/	308					20		
L1RxD hold time (from L1CLK falling edge) 37/	309					50		
L1TxD data valid after syncs rising edge (long) 36/	310					0	100	
L1TxD to high impedance (from L1SY0-L1SY1 falling edge) (long)	311					0	70	
NMSI timing								
RCLK1 and TCLK1 frequency 38/	315	See figure 4	Internal clock	All	9, 10, 11		5.12	MHz
			External clock				6.668	
RCLK1 and TCLK1 low/high	316		Internal clock			70		ns
			External clock			55		
RCLK1 and TCLK1 rise/fall time 39/	317		Internal clock				20	
			External clock					
TxD1 active delay from TCLK1 falling edge	318		Internal clock			0	40	
			External clock			0	70	
$\overline{RTS1}$ active/inactive delay from TCLK1 falling edge	319		Internal clock			0	40	
			External clock			0	100	
$\overline{CTS1}$ setup time to TCLK1 rising edge	320		Internal clock			50		
			External clock			10		
RXD1 setup time to RCLK1 rising edge	321		Internal clock			50		
			External clock			10		
RXD1 hold time from RCLK1 rising edge 40/	322		Internal clock			10		
			External clock			50		
$\overline{CD1}$ setup time to RCLK1 rising edge	323		Internal clock			50		
			External clock			10		

See footnotes on next sheet.

TABLE I. Electrical performance characteristics - Continued.

1/ Unless otherwise specified, all test conditions are worst case condition. Unless otherwise specified f = 16.67 MHz.
2/ CLKO loading is 50 pF maximum.
3/ CLKO skew from the rising and falling edges of EXTAL will not differ from each other by more than 1 ns, if the EXTAL rise time equals the EXTAL fall time.
4/ For loading capacitance of less than or equal to 50 pF, subtract 4 ns from the value given in the maximum column.
5/ Actual value depends on clock period.
6/ If test #47 is satisfied for both $\overline{DTACK}$ and $\overline{BERR}$, test #48 may be ignored. In the absence of $\overline{DTACK}$, $\overline{BERR}$ is a synchronous input using the asynchronous input setup time (test #47).
7/ For power-up, the device must be held in the reset state for 100 ms to allow stabilization of on-chip circuit. After the system is powered up test #56 refers to the minimum pulse width required to reset the processor.
8/ If the asynchronous input setup (test #47) requirement is satisfied fo $\overline{DTACK}$, the $\overline{DTACK}$ asserted to data setup time (test #31) requirement can be ignored. The data must only satisfy the data-in to clock low setup time (test #27) for the following clock cycle.
9/ When $\overline{AS}$ and R/$\overline{W}$ are equally loaded (" 20%), subtract 5 ns from the values given in these columns.
10/ The device will negate $\overline{BG}$ and begin driving the bus if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.
11/ The minimum value must be met to guarantee proper operation. If the maximum value is exceeded, $\overline{BG}$ may be reasserted.
12/ This specification is valid only when the RMCST bit is set in the SCR register.
13/ Occurs on S0 of SDMA read/write access when the SDMA becomes bus master.
14/ $\overline{DREQ}$ is sampled on the falling edge of CLK in cycle steal and burst modes.
15/ If test #80 is satisfied for $\overline{DREQ}$, test #81 may be ignored.
16/ $\overline{BR}$ will not be asserted while $\overline{AS}$, $\overline{HALT}$, or $\overline{BERR}$ is asserted. Specifications are for DISABLE CPU mode only.
17/ $\overline{DREQ}$, $\overline{DACK}$, and $\overline{DONE}$ do not apply to the SDMA channels. IDMA and SDMA read and write cycle timing is the same as that for the device core.
18/ If $\overline{AS}$ is negated before $\overline{DS}$, the data bus could be three-stated(test #126) before $\overline{DS}$ is negated.
19/ Specifications are valid only when SAM = 1 in the SCR.
20/ For loading capacitance less than or equal to 50 pF, subtract 4 ns from the maximum value given.
21/ This specification is valid only when the ADCE or WPVE bits in the SCR are set.
22/ Tests #172-178 do not have diagrams. However, similar diagrams for $\overline{AS}$ are shown as #25, 11, 13, 14, 17, 20A, and 29, respectively.
23/ The minimum value must be met to guarantee write protection operation.
24/ This specification is valid when the DCE or WPVE bits in the SCR are set.
25/ Also applies after a timeout of the hardware watchdog.
26/ Setup time for the asynchronous inputs $\overline{IPL2}$ - $\overline{IPL0}$ and $\overline{AVEC}$ guarantees their recognition at the next falling edge of the clock.
27/ $\overline{FRZ}$ should be negated during total system reset.
28/ This also applies when SPCLK is inverted by CI in the SPMODE register.
29/ The enable signals for the slaves may be implemented by the parallel I/O pins.
30/ The ratio CLK/L1CLK must be greater than 2.5/1.
31/ High impedance is measured at the 30% and 70% of V_{DD} points, with the line at $V_{DD}/2$ through 10K in parallel with 130 pF.
32/ The ratio CLK/L1CLK must be greater than 2.5/1.
33/ Schmitt trigger used on input buffer.
34/ Condition C_L = 150 pF. L1TxD becomes valid after the L1CLK rising edge or L1SY1, whichever is later.
35/ SDS1-SDS2 become valid after the L1CLK rising edge or L1SY1, whichever is later.
36/ L1TxD becomes valid after the L1CLK rising edge or the sync enable, whichever is later, if long frames are used.
37/ Specification valid for both sync methods.
38/ The ratio CLK/TCLK1 and CLK/RCLK1 must be greater than 2.5/1 for external clock. For internal clock the ratio must be greater than 3/1 (the input clock to the baud rate generator may be either CLK or TIN1), in both cases the maximum frequency is limited to 16.67 MHz. In asynchronous mode (UART), the bit rate is 1/16 of the clock rate.
39/ Schmitt triggers used on input buffers.
40/ Also applies to $\overline{CD}$ hold time when $\overline{CD}$ is used as an external sync in BISYNC or totally transparent mode.

Case Y

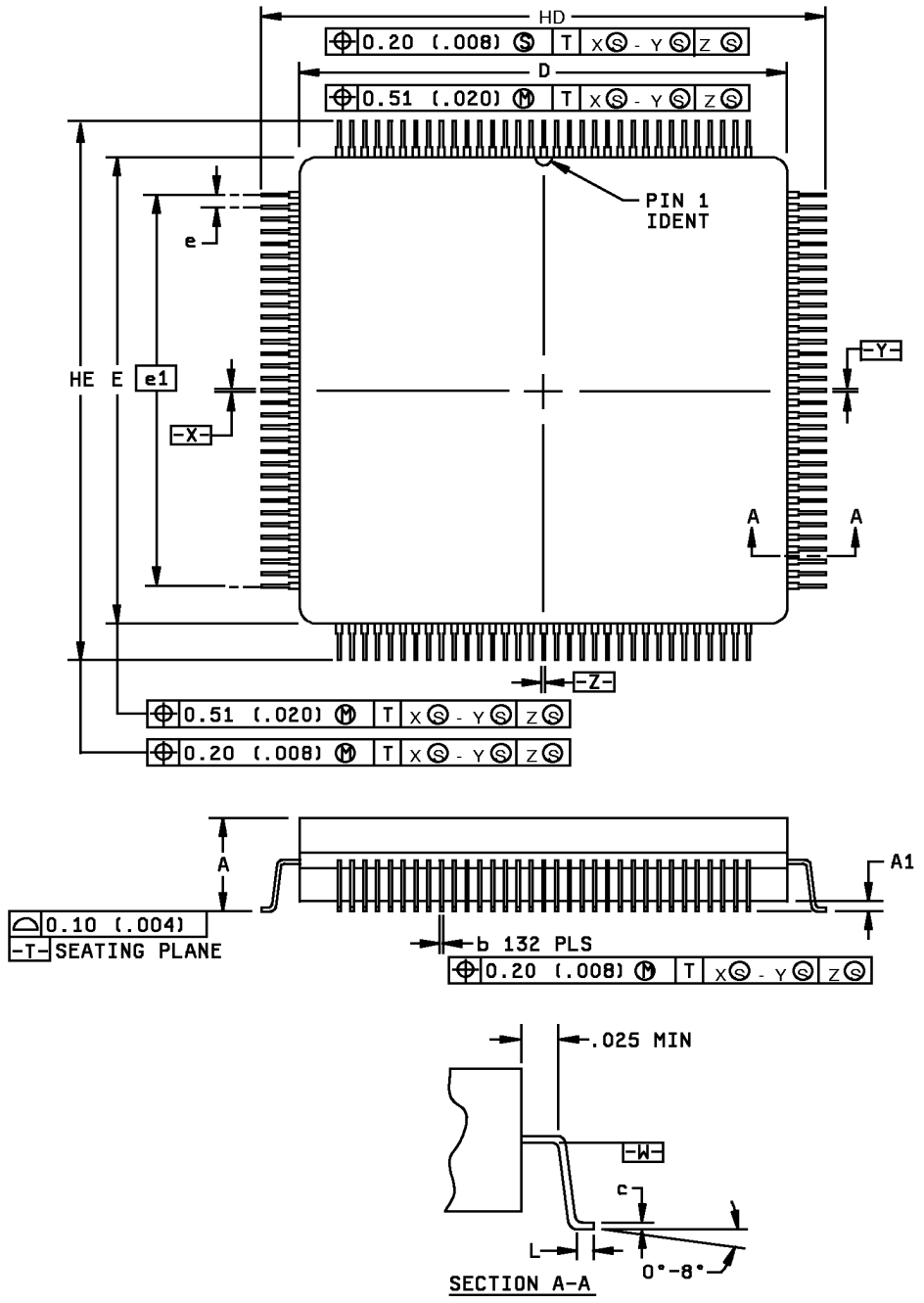


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-93159
		REVISION LEVEL	SHEET 18

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.94	4.52	.155	.178
A1	0.50	1.00	.019	.039
b	0.204	0.292	.0080	.0115
c	0.13	0.20	.005	.008
D	21.85	22.86	.860	.900
E	21.85	22.86	.860	.900
e	0.64 BSC		.025 BSC	
e1	20.32 REF		.800 REF	
HD	27.23	27.63	1.072	1.088
HE	27.23	27.63	1.072	1.088
L	0.51	0.76	.020	.030

NOTES:

1. The preferred unit of measurement is millimeters. However, this item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Dimensions D and E define maximum ceremic body dimensions including glass protrusion and mismatch of ceremic body top and bottom.
3. Datum plane -W- is located at the underside of leads where leads exit package body.
4. Datum X-Y and Z to be determined where center leads exit package body at datum -W-.
5. Dimensions HD and HE to be determined at seating plane, datum -T-.
6. Dimensions D and E to be determined at datum plane -W-.

FIGURE 1. Case outline - Continued.

Device type	All								
Case outline	X								
Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
A1	A14	C2	A13	E11	$\overline{CD2}$	J12	NC	M3	TIN2
A2	A21	C3	A17	E12	SDS2	J13	DISCPU	M4	V_{DD}
A3	A22	C4	GND	E13	RXD3	K1	$\overline{CS0}$	M5	$\overline{IACK7}$
A4	GND	C5	A23	F1	GND	K2	$\overline{RMC}$	M6	$\overline{AS}$
A5	D15	C6	D14	F2	A4	K3	IAC	M7	GND
A6	D12	C7	D11	F3	A5	K4	PB9	M8	CLKO
A7	GND	C8	V_{DD}	F11	TXD3	K5	$\overline{WDOG}$	M9	$\overline{BERR}$
A8	D9	C9	D4	F12	RCLK3	K9	$\overline{DTACK}$	M10	$\overline{BR}$
A9	D7	C10	D1	F13	TCLK3	K10	V_{DD}	M11	$\overline{BGACK}$
A10	D6	C11	$\overline{CD1}$	G1	A1	K11	TXD1	M12	$\overline{BG}$
A11	GND	C12	RCLK2	G2	A3	K12	$\overline{RTS1}$	M13	$\overline{RTS3}$
A12	D3	C13	$\overline{RTS2}$	G3	A2	K13	BUSW	N1	PB10
A13	RXD1	D1	A7	G11	PA12	L1	$\overline{CS2}$	N2	TIN1
B1	A11	D2	GND	G12	$\overline{DREQ}$	L2	PB11	N3	$\overline{IACK1}$
B2	A18	D3	A12	G13	GND	L3	GND	N4	GND
B3	A19	D4	A15	H1	FC0	L4	$\overline{TOUT1}$	N5	$\overline{UDS}$
B4	A20	D5	A16	H2	V_{DD}	L5	$\overline{IACK6}$	N6	R/$\overline{W}$
B5	V_{DD}	D9	RXD2	H3	FC1	L6	$\overline{LDS}$	N7	EXTAL
B6	D13	D10	$\overline{CTS1}$	H11	$\overline{FRZ}$	L7	XTAL	N8	V_{DD}
B7	D10	D11	TCLK2	H12	$\overline{DONE}$	L8	$\overline{IPL0}$	N9	$\overline{IPL1}$
B8	D8	D12	GND	H13	$\overline{DACK}$	L9	$\overline{AVEC}$	N10	$\overline{IPL2}$
B9	D5	D13	V_{DD}	J1	FC2	L10	NC	N11	$\overline{RESET}$
B10	D2	E1	A6	J2	$\overline{CS1}$	L11	$\overline{BCLR}$	N12	$\overline{HALT}$
B11	D0	E2	A8	J3	GND	L12	TCLK1	N13	RCLK1
B12	$\overline{CTS3}$	E3	A9	J4	PB8	L13	$\overline{CD3}$		
B13	$\overline{CTS2}$	E4	V_{DD}	J10	GND	M1	$\overline{CS3}$		
C1	A10	E10	TXD2	J11	BRG1	M2	$\overline{TOUT2}$		

FIGURE 2. Terminal connections.

Device type	All								
Case outline	Y								
Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
1	A1	28	V_{DD}	55	RCLK2	82	RCLK1	109	$\overline{IACK6}$
2	A2	29	GND	56	TCLK2	83	V_{DD}	110	$\overline{IACK1}$
3	A3	30	D15	57	GND	84	GND	111	TIN1
4	GND	31	D14	58	$\overline{CTS2}$	85	$\overline{DTACK}$	112	V_{DD}
5	A4	32	D13	59	$\overline{RTS2}$	86	$\overline{BCLR}$	113	$\overline{TOUT1}$
6	A5	33	D12	60	$\overline{CD2}$	87	$\overline{BG}$	114	TIN2
7	A6	34	GND	61	SDS2	88	$\overline{BGACK}$	115	$\overline{TOUT2}$
8	A7	35	D11	62	V_{DD}	89	NC	116	GND
9	A8	36	D10	63	RXD3	90	$\overline{BR}$	117	$\overline{WDOG}$
10	A9	37	D9	64	TXD3	91	$\overline{HALT}$	118	PB8
11	A10	38	D8	65	RCLK3	92	$\overline{RESET}$	119	PB9
12	A11	39	V_{DD}	66	TCLK3	93	$\overline{AVEC}$	120	PB10
13	GND	40	D7	67	GND	94	$\overline{BERR}$	121	PB11
14	A12	41	D6	68	PA12	95	$\overline{IPL2}$	122	IAC
15	A13	42	D5	69	$\overline{DREQ}$	96	$\overline{IPL1}$	123	$\overline{RMC}$
16	A14	43	D4	70	$\overline{DACK}$	97	$\overline{IPL0}$	124	$\overline{CS3}$
17	A15	44	GND	71	$\overline{DONE}$	98	CLKO	125	$\overline{CS2}$
18	V_{DD}	45	D3	72	$\overline{FRZ}$	99	V_{DD}	126	GND
19	A16	46	D2	73	DISCPU	100	EXTAL	127	$\overline{CS1}$
20	A17	47	D1	74	BUSW	101	XTAL	128	$\overline{CS0}$
21	A18	48	D0	75	NC	102	GND	129	FC2
22	A19	49	$\overline{CTS3}$	76	BRG1	103	R/$\overline{W}$	130	FC1
23	GND	50	$\overline{CD1}$	77	$\overline{CD3}$	104	$\overline{AS}$	131	V_{DD}
24	A20	51	$\overline{CTS1}$	78	$\overline{RTS3}$	105	$\overline{LDS}$	132	FC0
25	A21	52	RXD1	79	$\overline{RTS1}$	106	$\overline{UDS}$		
26	A22	53	RXD2	80	TXD1	107	GND		
27	A23	54	TXD2	81	TCLK1	108	$\overline{IACK7}$		

FIGURE 2. Terminal connections - Continued.

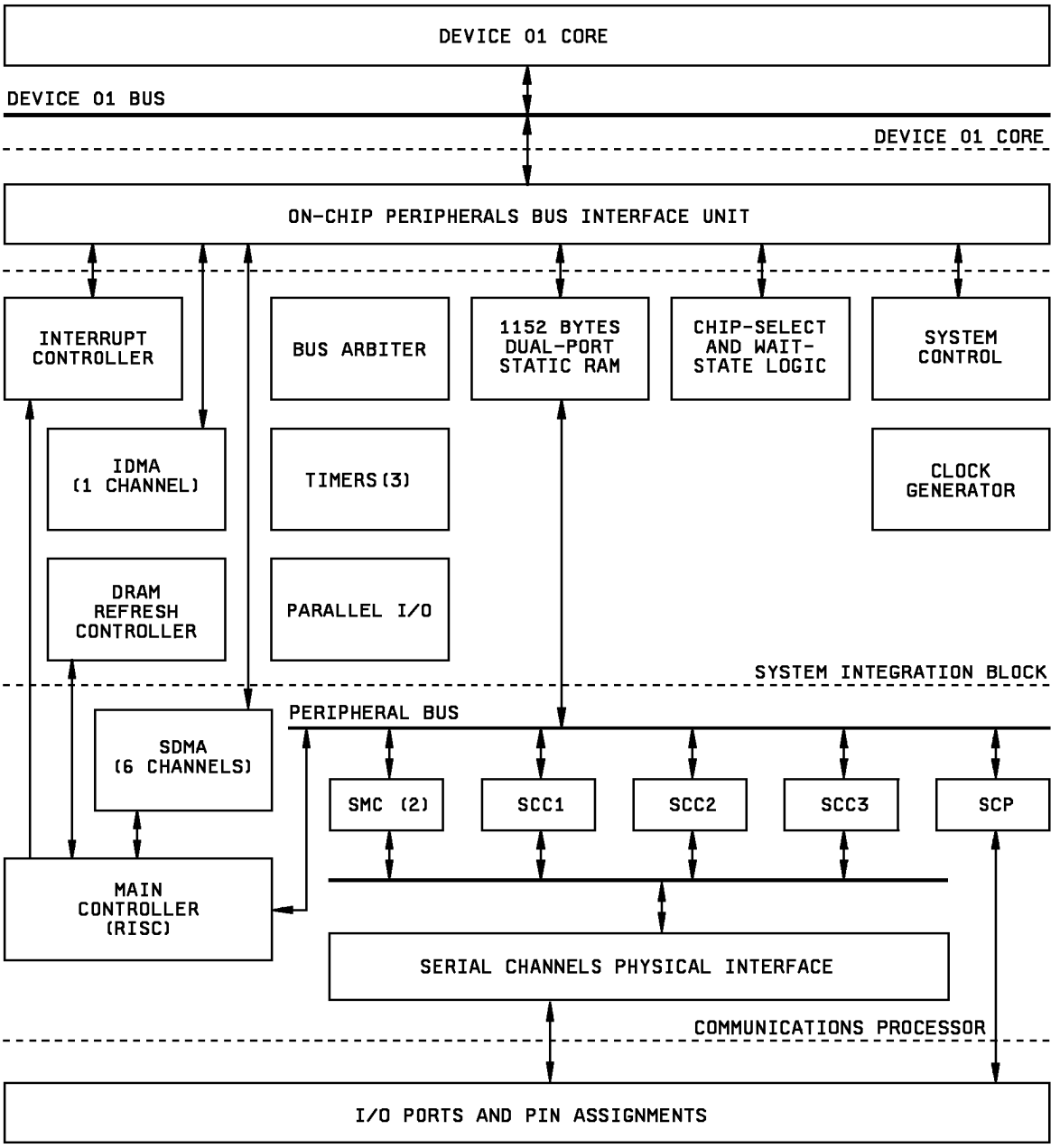


FIGURE 3. Functional block diagrams.

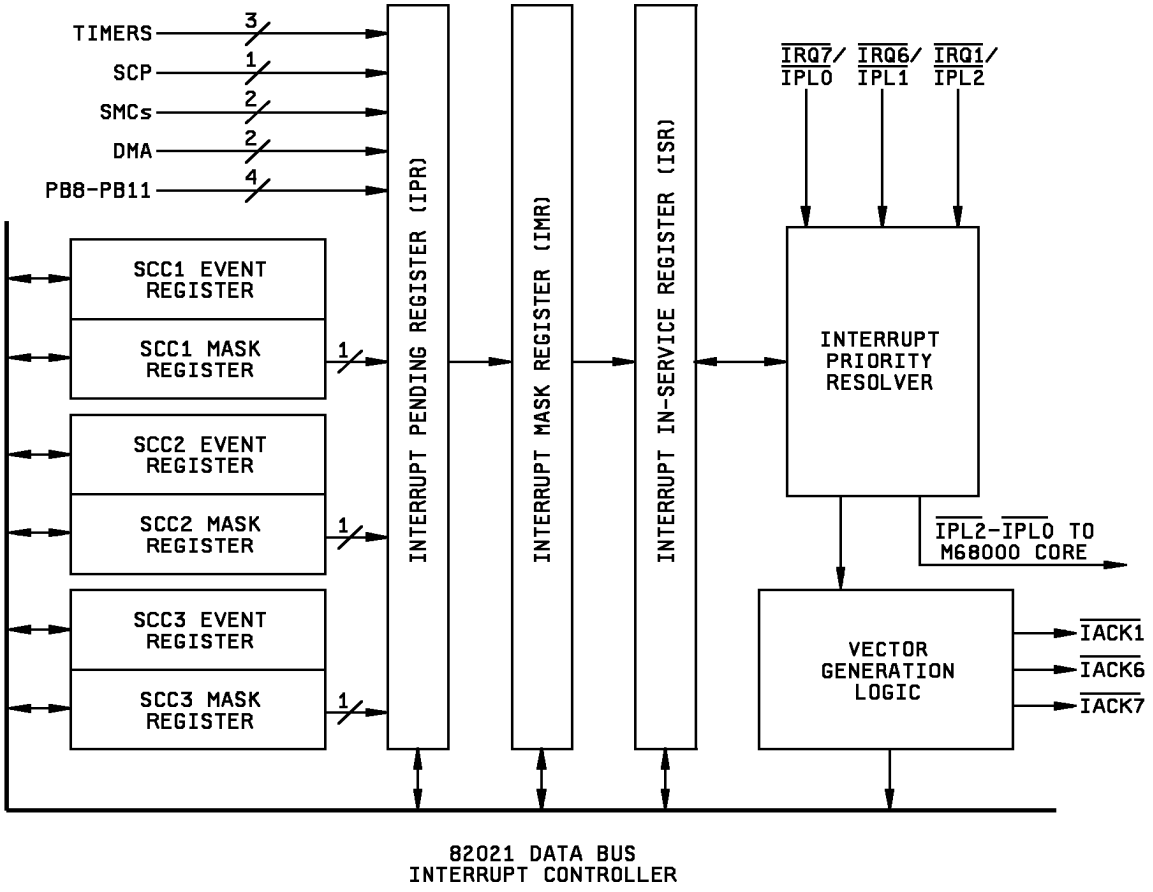
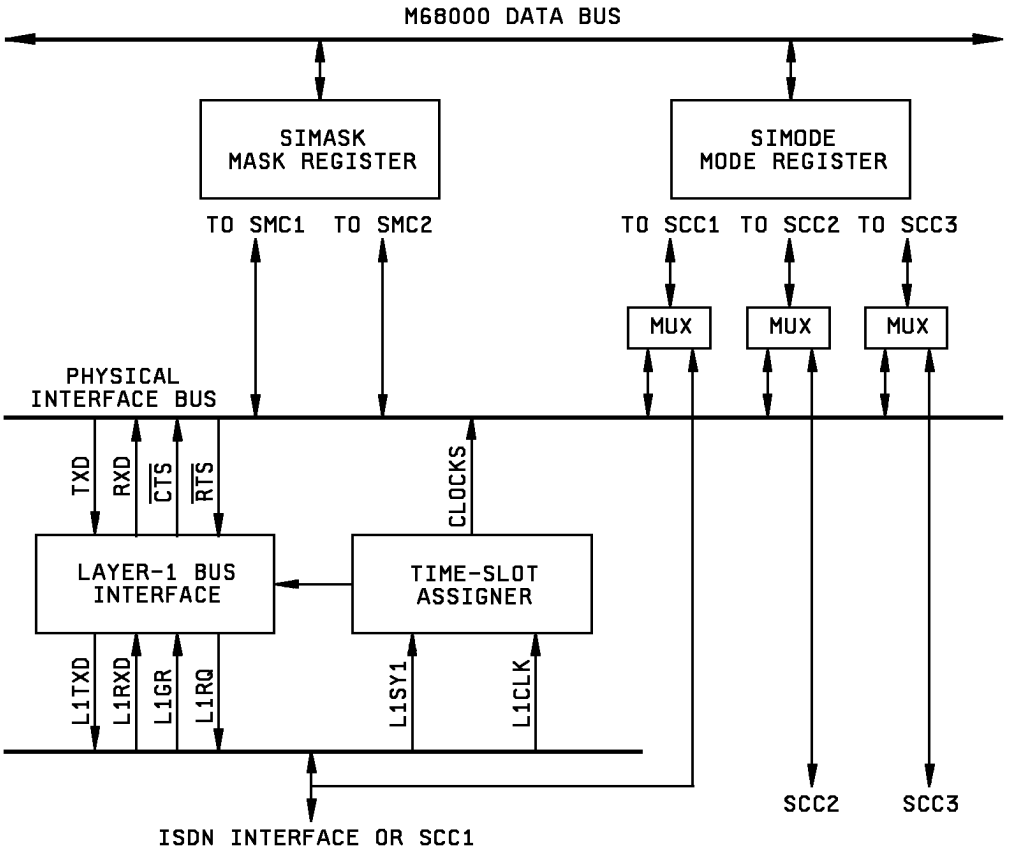
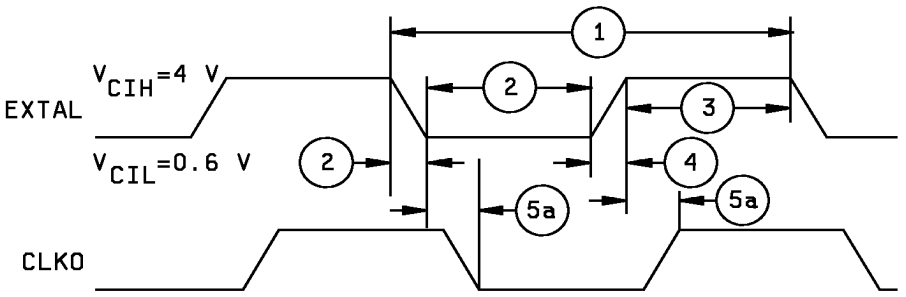


FIGURE 3. Functional block diagrams - Continued.



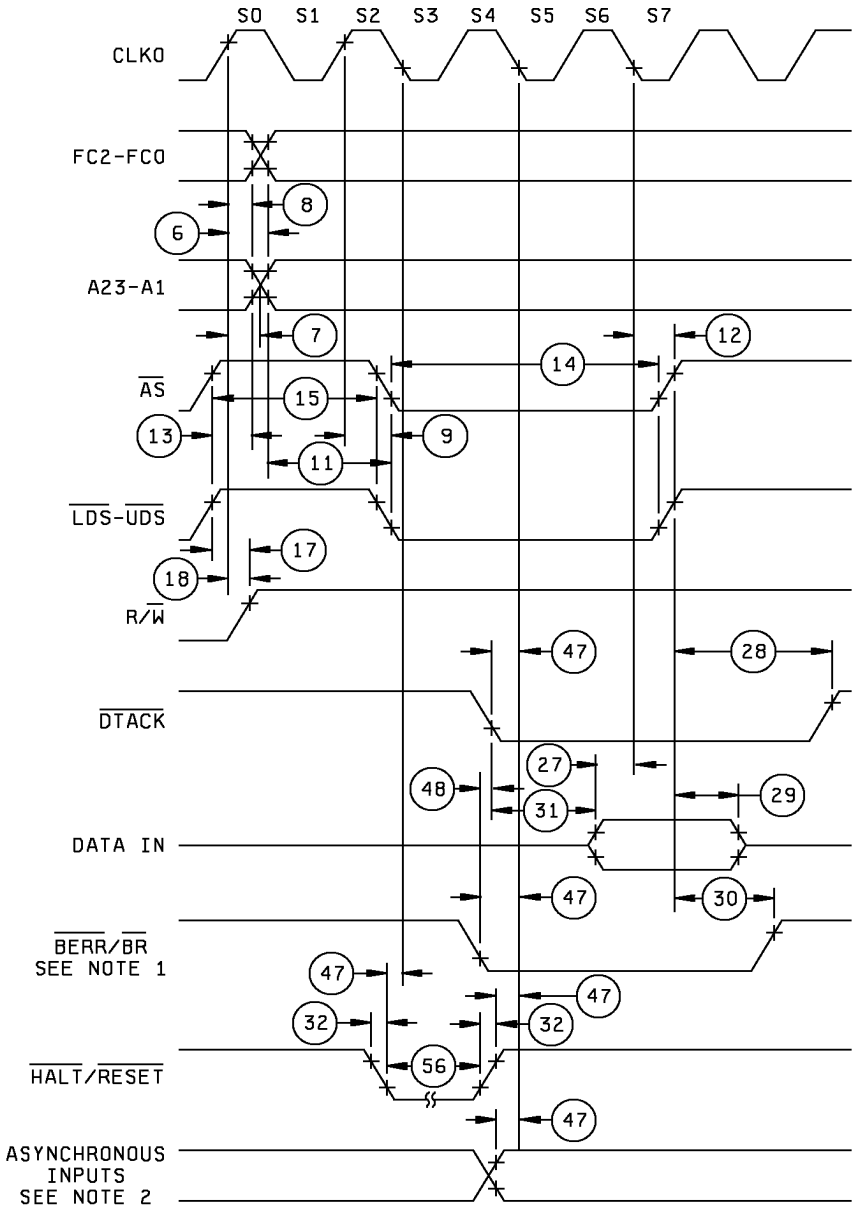
SERIAL CHANNELS PHYSICAL INTERFACE

FIGURE 3. Functional block diagrams - Continued.



CLOCK TIMING

FIGURE 4. Timing waveforms.

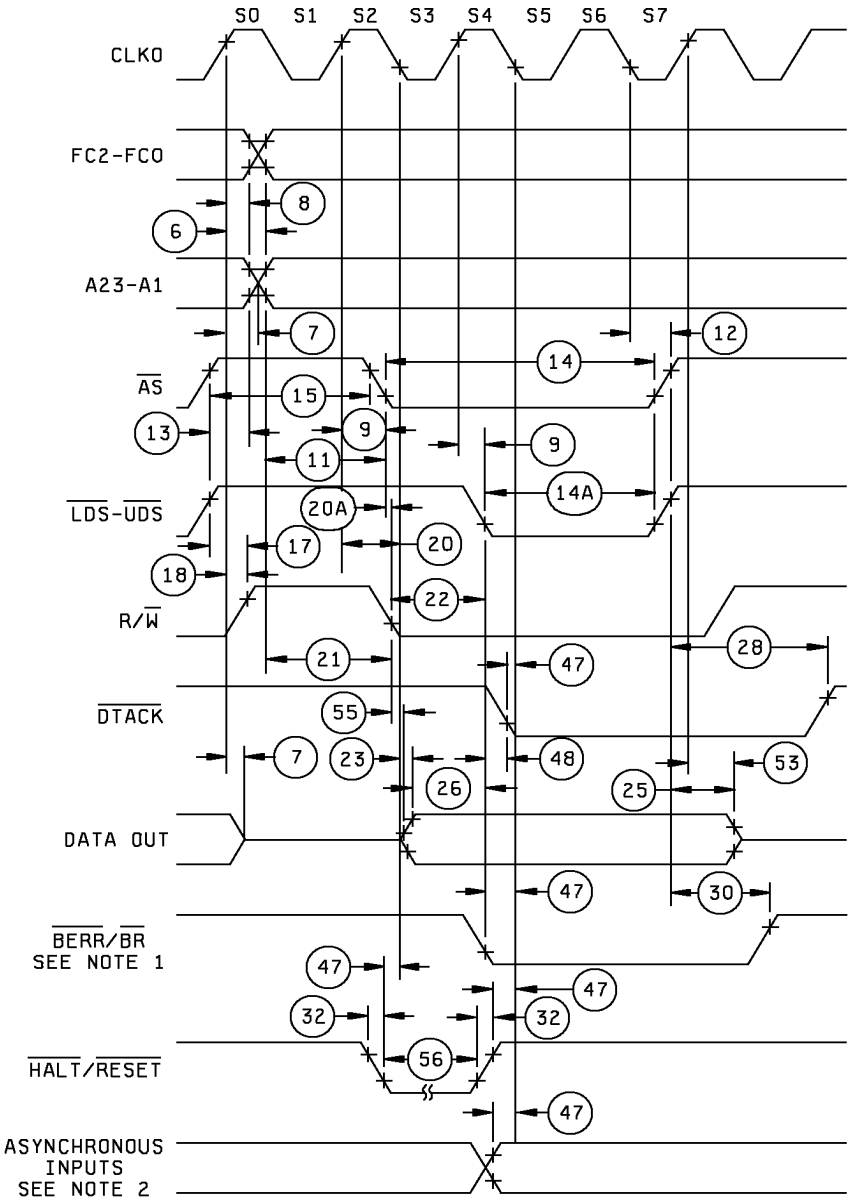


READ CYCLE TIMING

NOTES:

1. $\overline{BR}$ needs fall at the same time only to ensure being recognized at the end of the bus cycle.
2. Set up time for the asynchronous inputs $\overline{IPL2}$ - $\overline{IPL0}$ guarantees their recognition at the next falling edge of clock.
3. Timing measurement are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8 V and 2.0 V.

FIGURE 4. Timing waveforms - Continued.

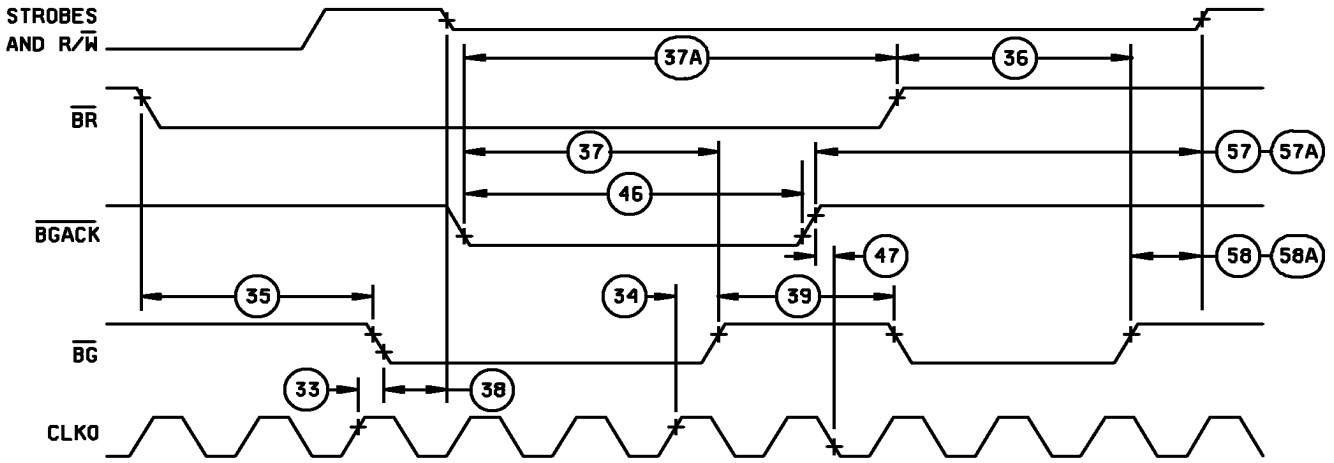


WRITE CYCLE TIMING

NOTES:

1. Because of the loading variations, R/$\overline{W}$ may be valid after $\overline{AS}$ even though both are initiated by the rising edge of S2 (#20A).
2. Timing measurement are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8 V and 2.0 V.

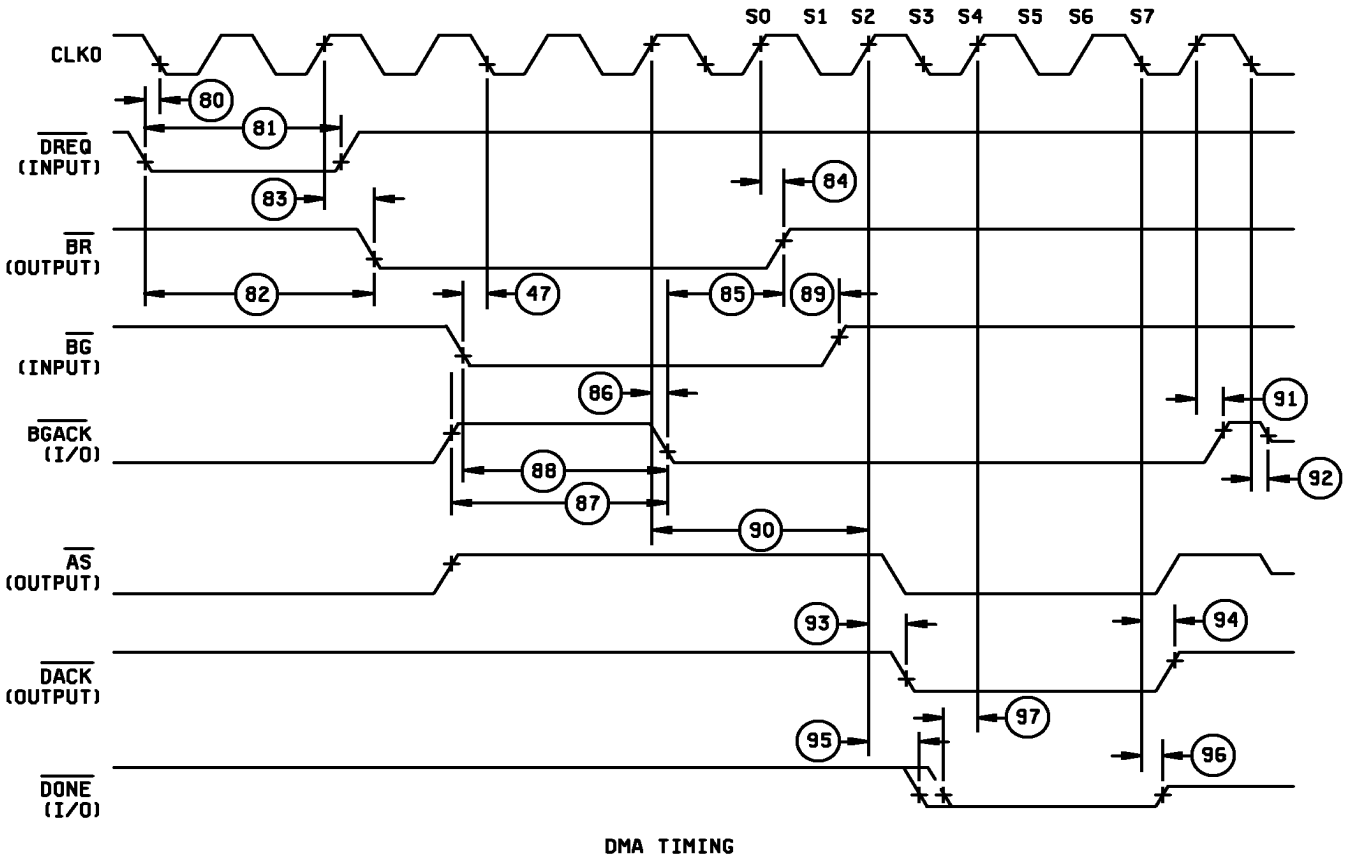
FIGURE 4. Timing waveforms - Continued.



BUS ARBITRATION TIMING

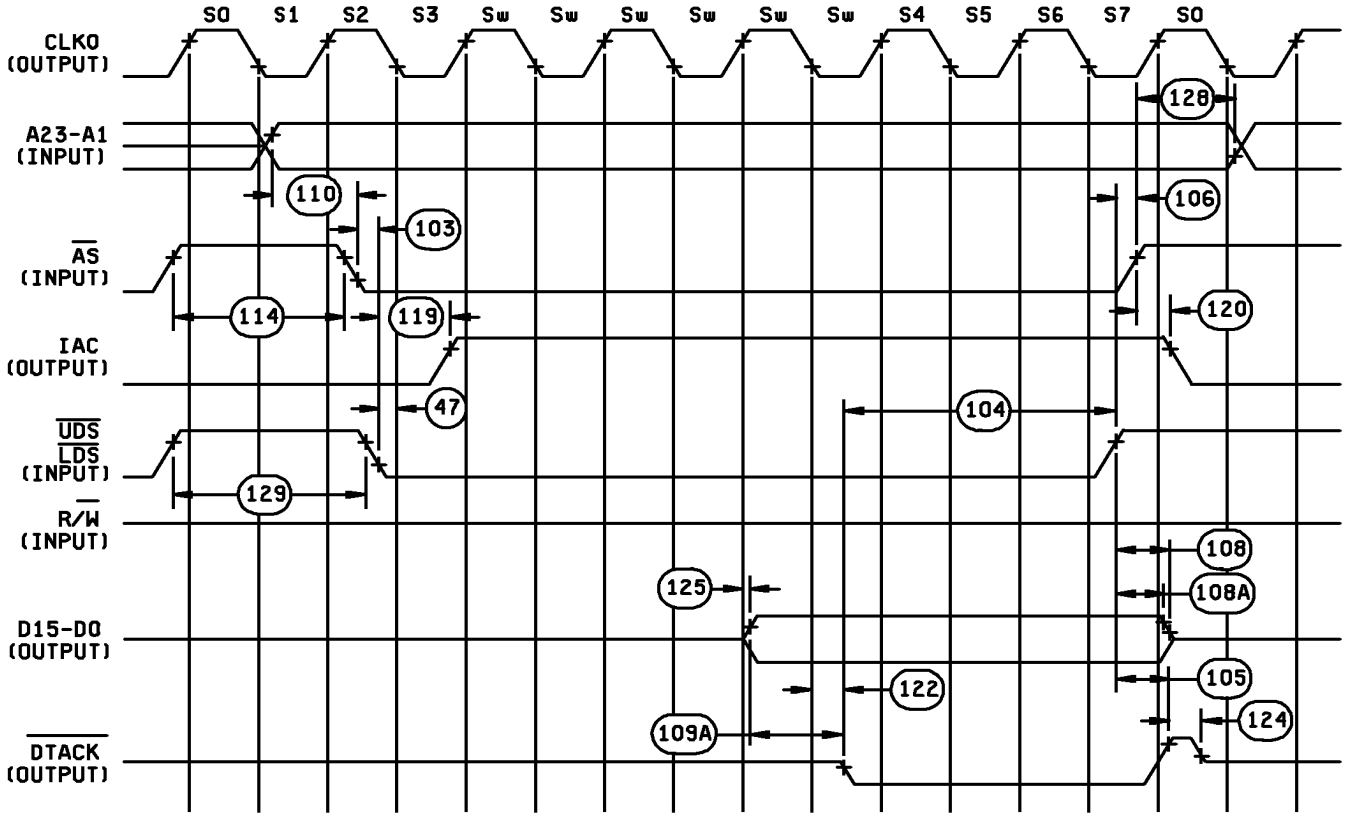
NOTE: Setup time to the clock (#47) for the asynchronous inputs $\overline{\text{BERR}}$, $\overline{\text{BGACK}}$, $\overline{\text{BR}}$, $\overline{\text{DTACK}}$, and $\overline{\text{IPL2}}$ - $\overline{\text{IPL0}}$ guarantees their recognition at the next falling edge of the clock.

FIGURE 4. Timing waveforms - Continued.



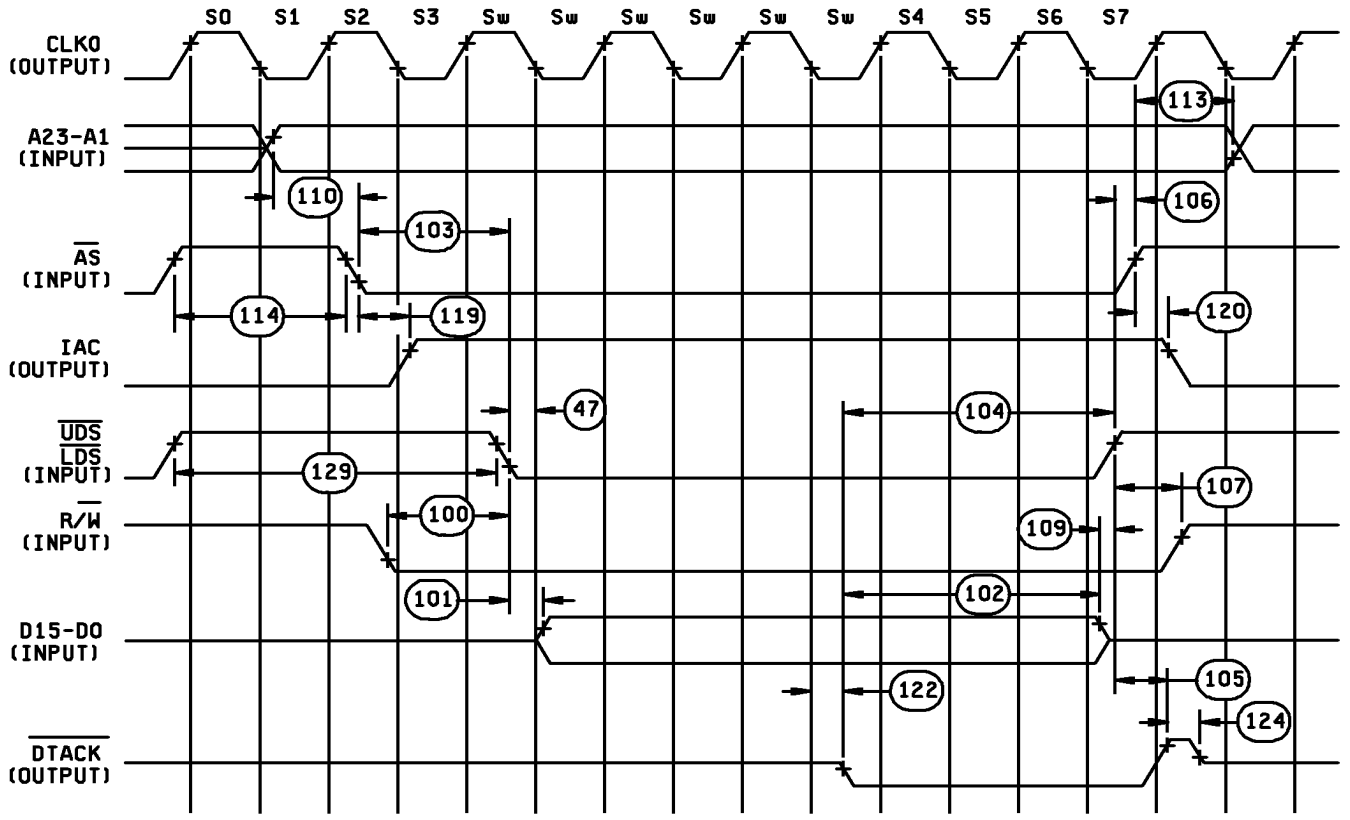
DMA TIMING

FIGURE 4. Timing waveforms - Continued.



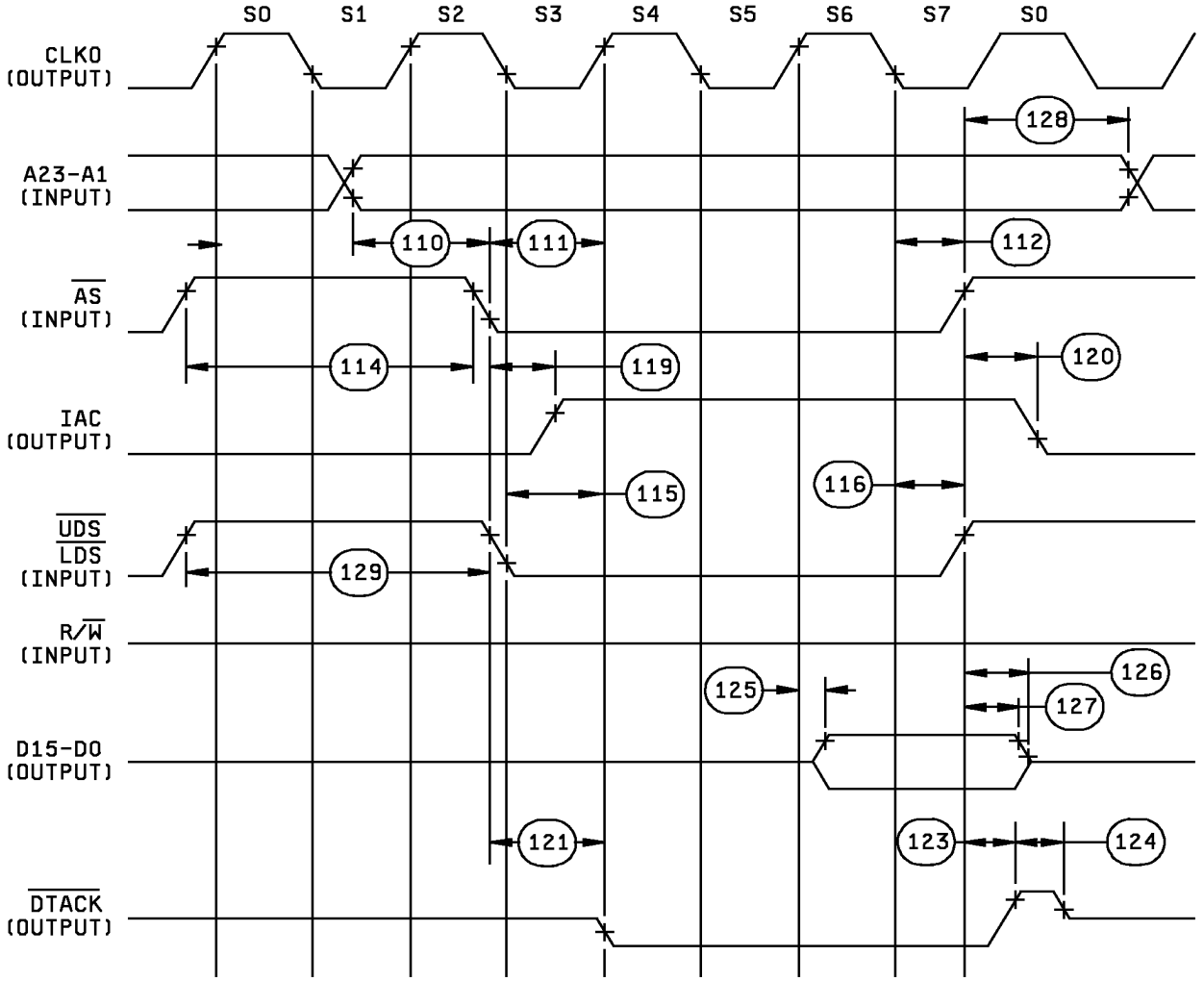
EXTERNAL MASTER INTERNAL ASYNCHRONOUS READ CYCLE TIMING

FIGURE 4. Timing waveforms - Continued.



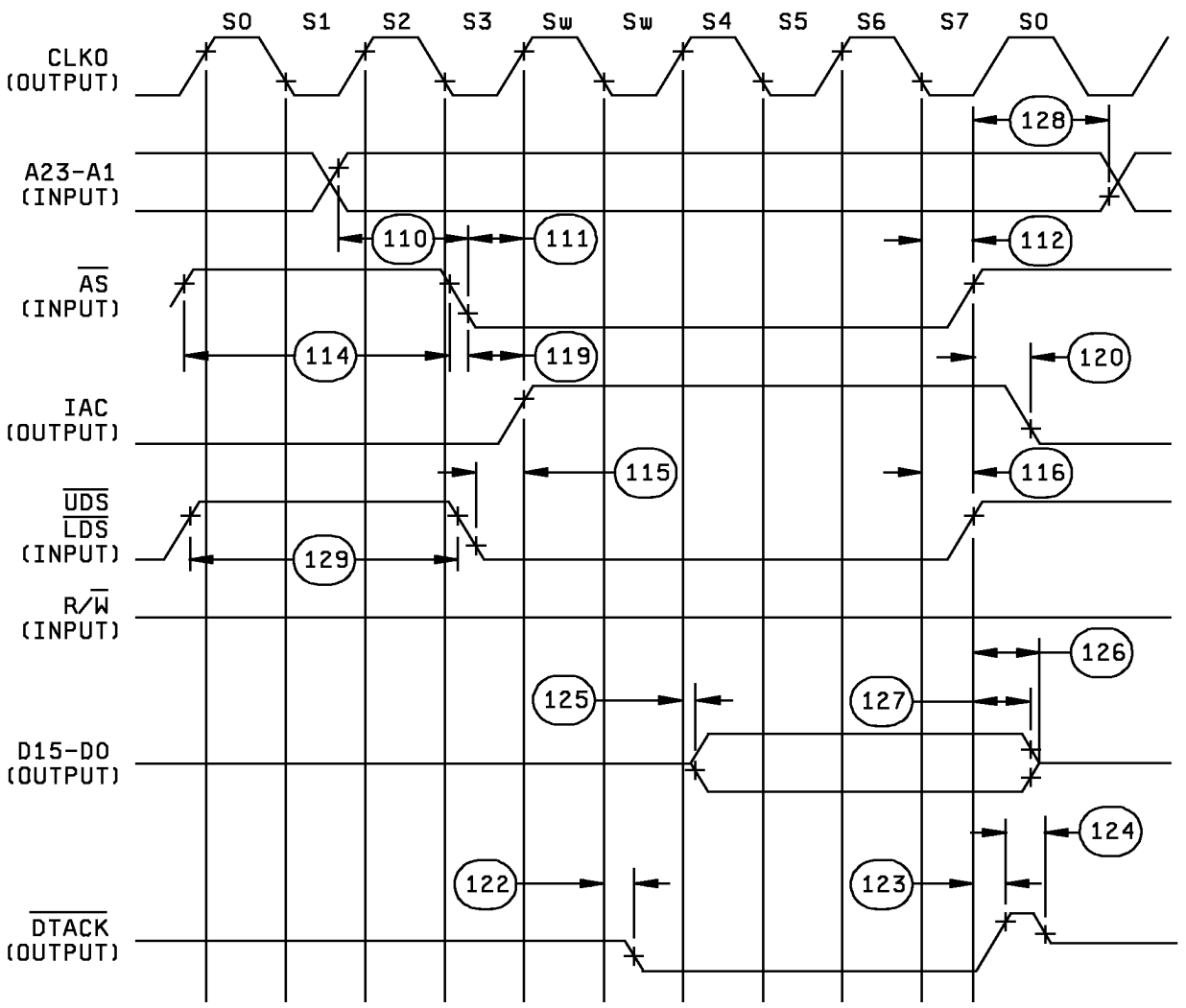
EXTERNAL MASTER INTERNAL ASYNCHRONOUS WRITE CYCLE TIMING

FIGURE 4. Timing waveforms - Continued.



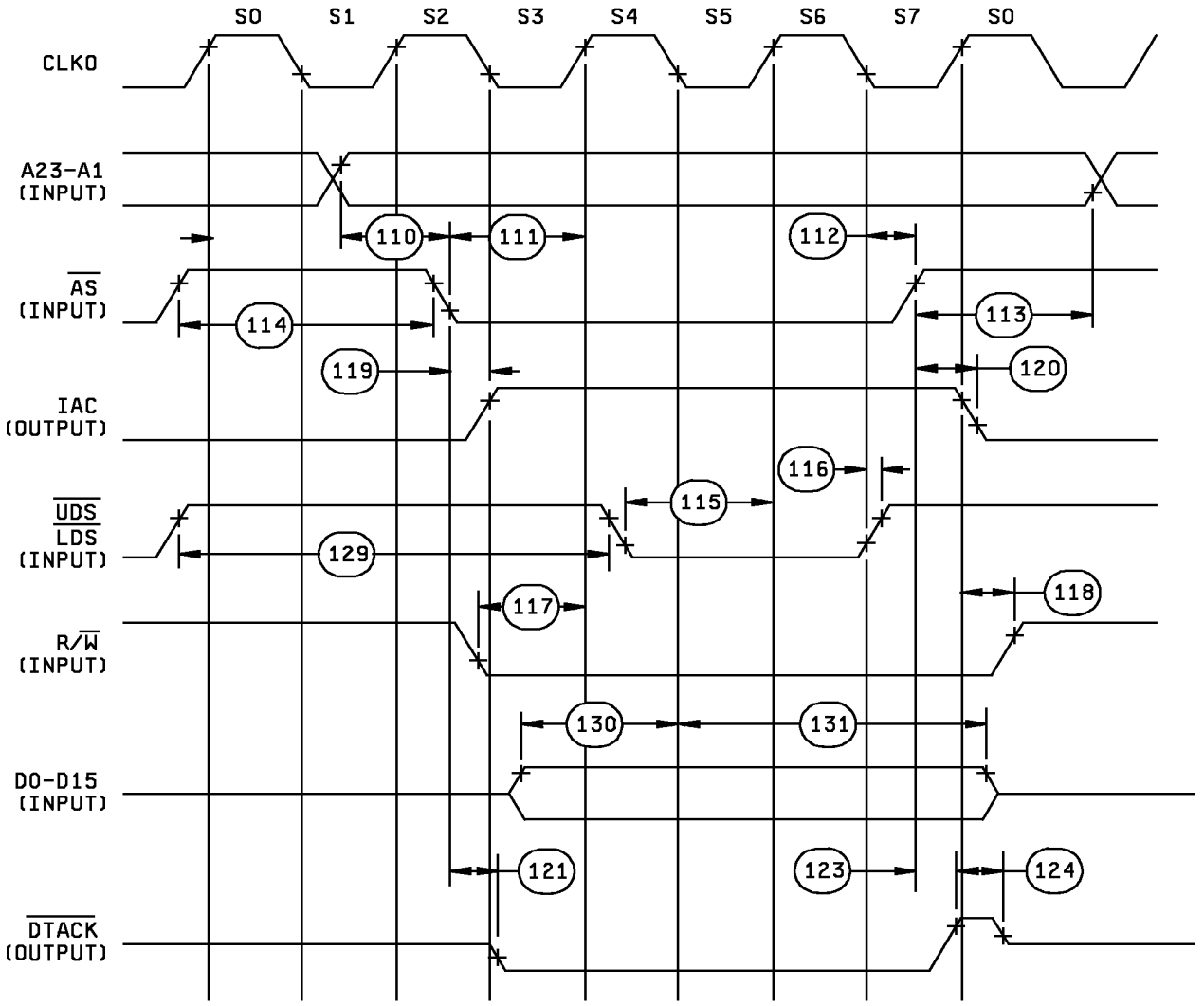
EXTERNAL MASTER INTERNAL SYNCHRONOUS READ CYCLE TIMING

FIGURE 4. Timing waveforms - Continued.



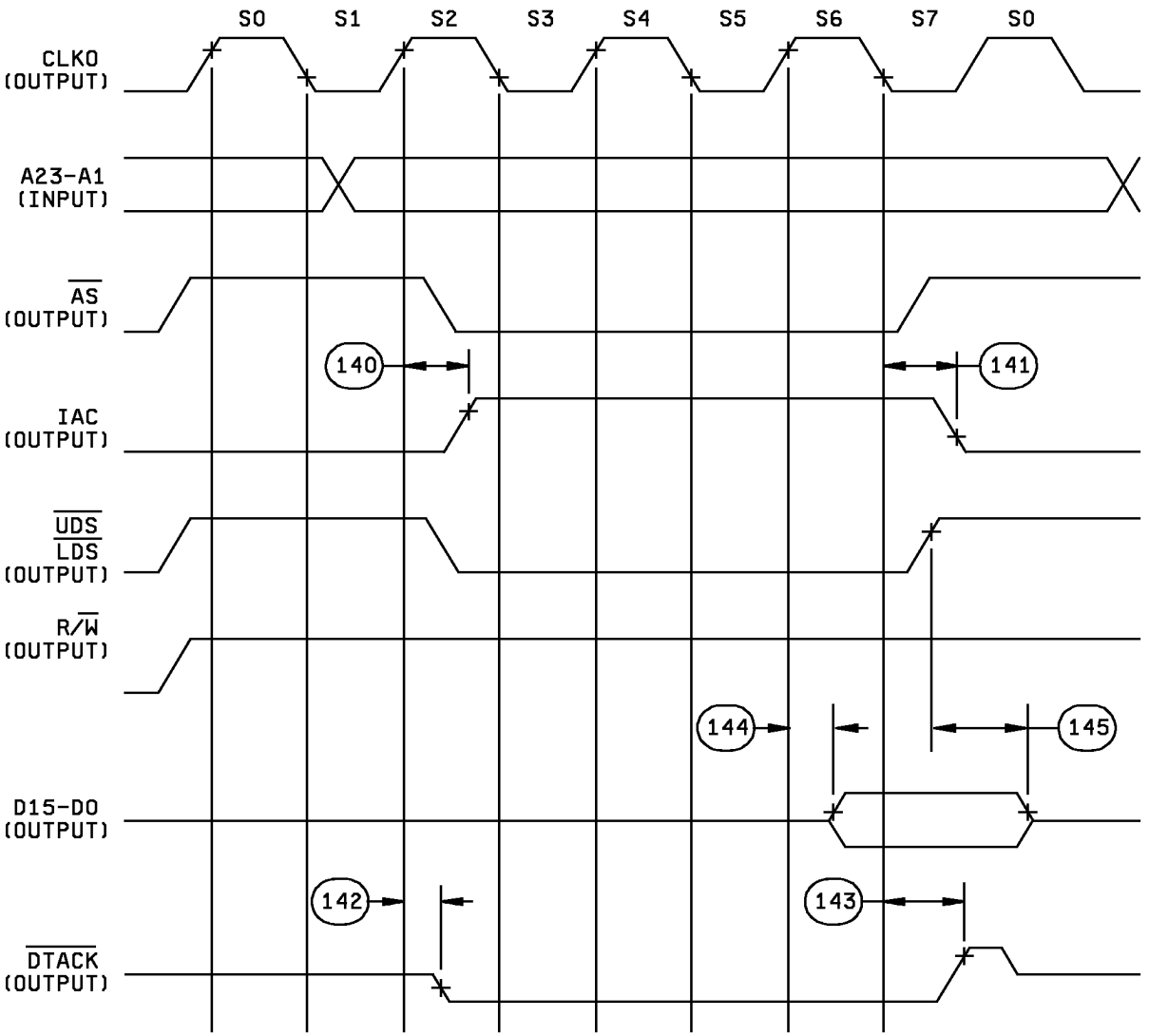
EXTERNAL MASTER INTERNAL SYNCHRONOUS
READ CYCLE (ONE WAIT STATE) TIMING

FIGURE 4. Timing waveforms - Continued.



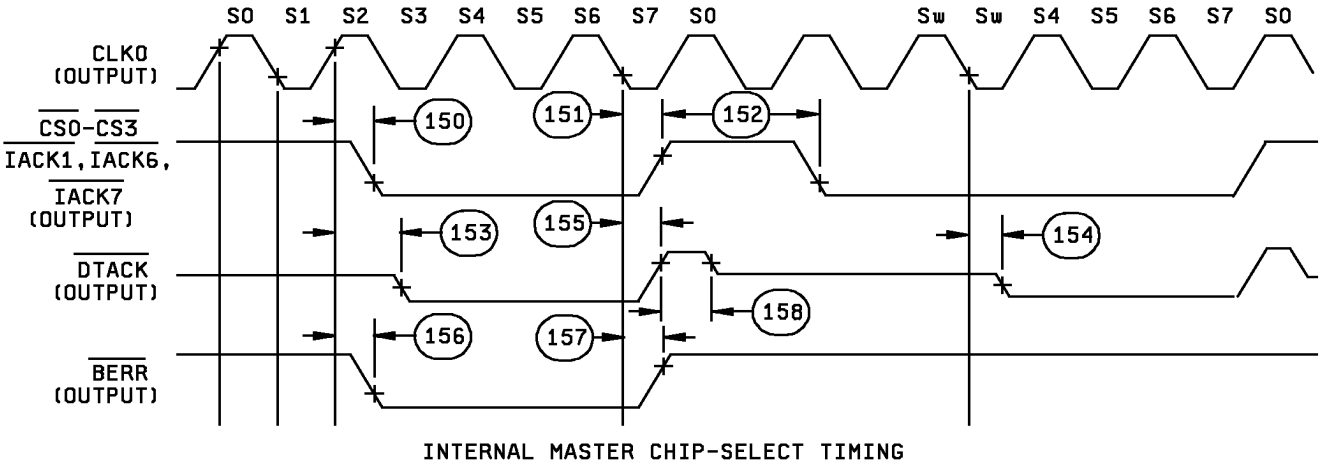
EXTERNAL MASTER INTERNAL SYNCHRONOUS WRITE CYCLE TIMING

FIGURE 4. Timing waveforms - Continued.

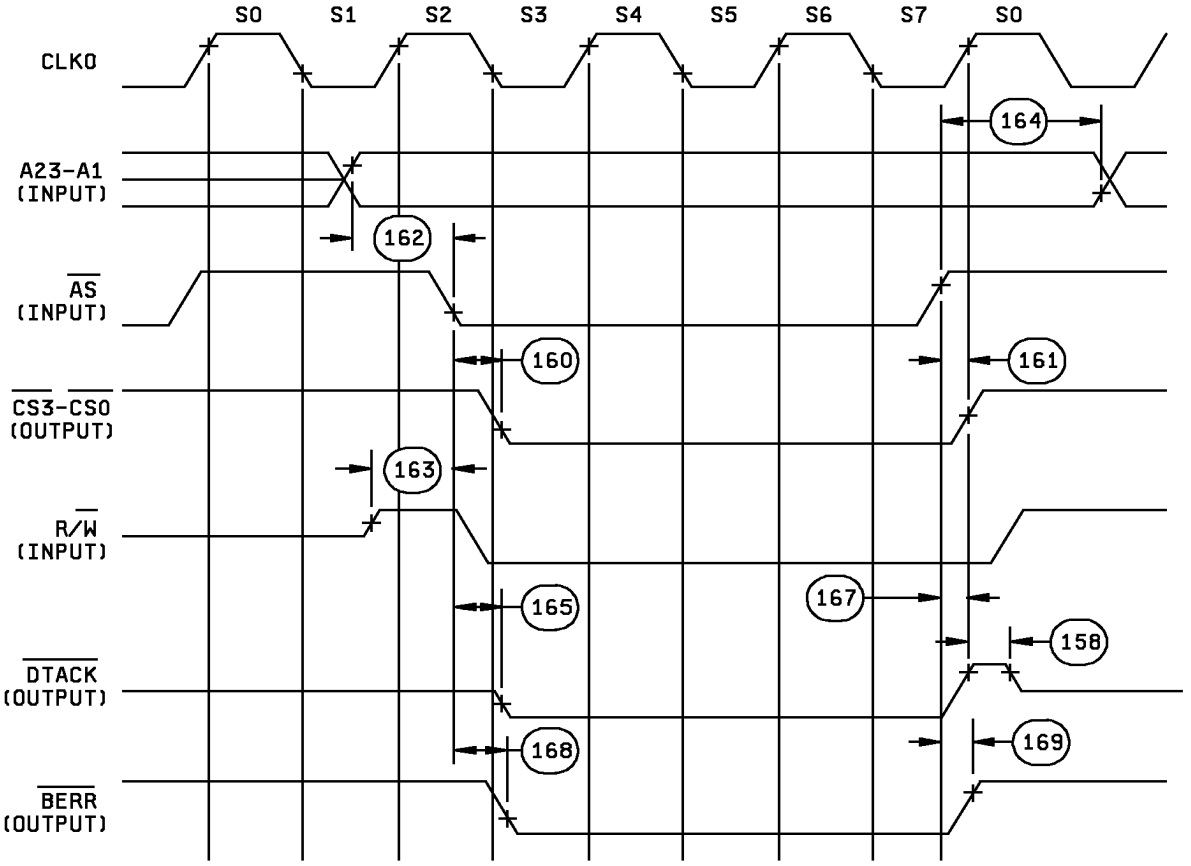


INTERNAL MASTER INTERNAL READ CYCLE TIMING

FIGURE 4. Timing waveforms - Continued.

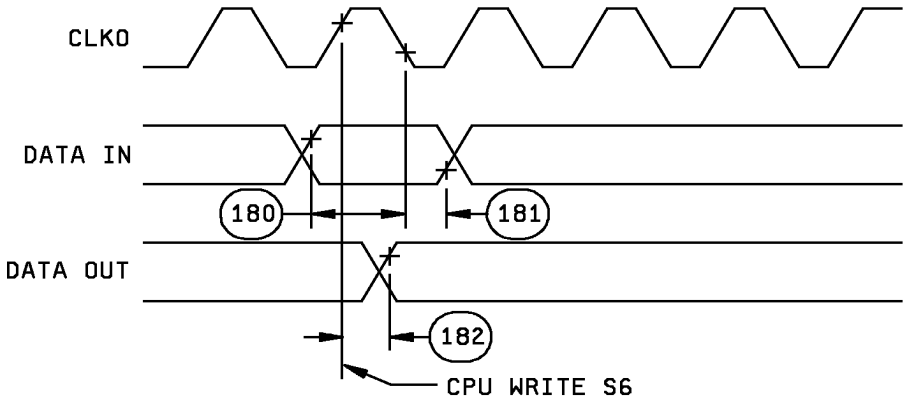


INTERNAL MASTER CHIP-SELECT TIMING

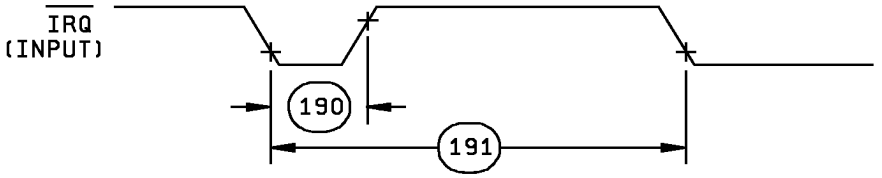


EXTERNAL MASTER CHIP-SELECT TIMING

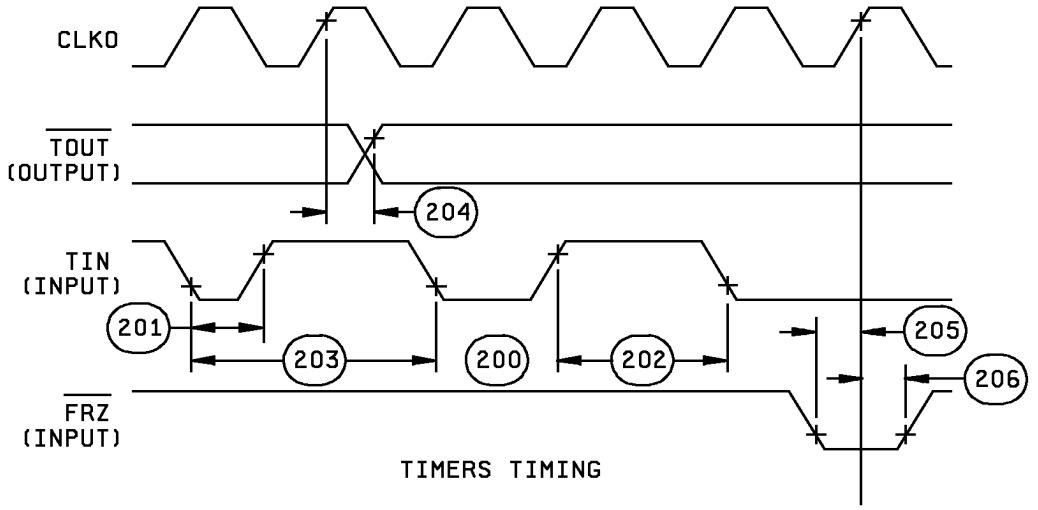
FIGURE 4. Timing waveforms - Continued.



PARALLEL I/O DATA IN/DATA OUT TIMING

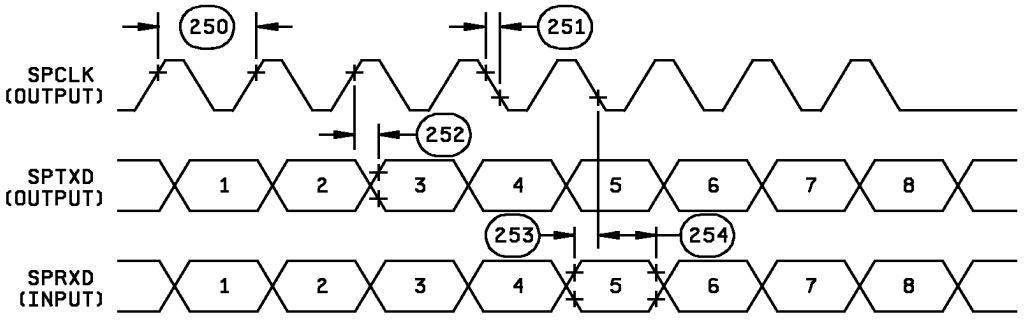


INTERRUPTS TIMING

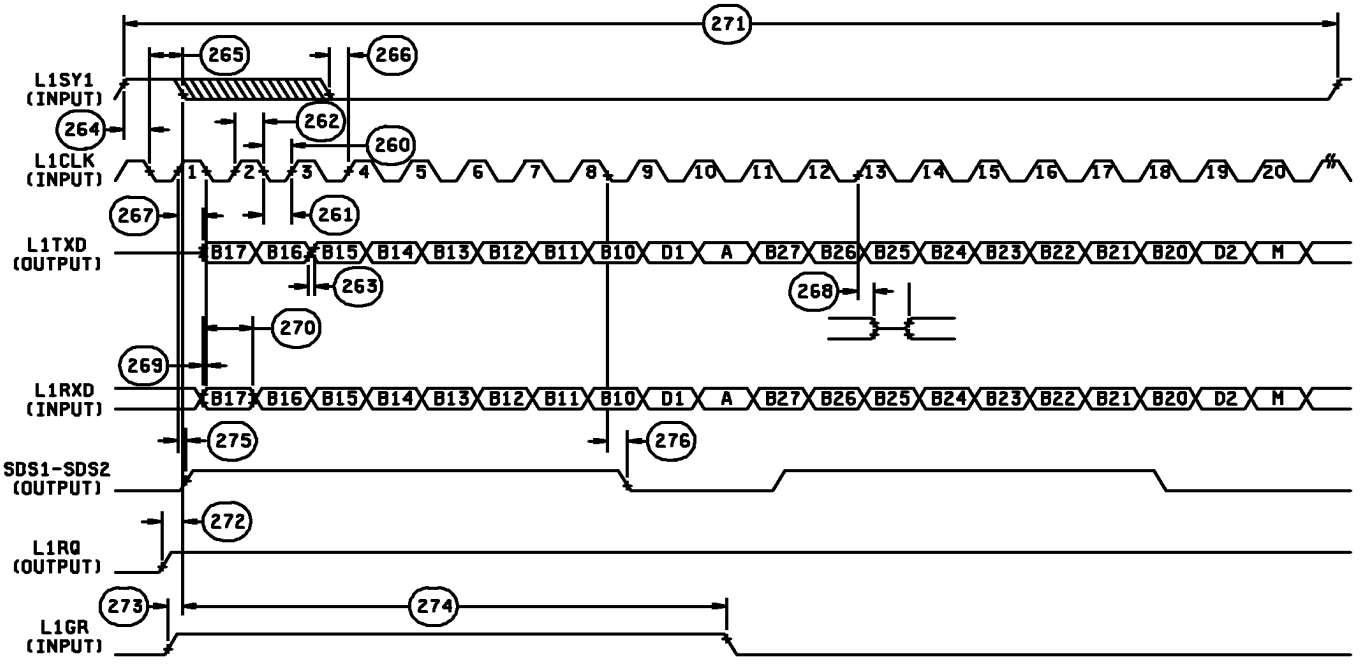


TIMERS TIMING

FIGURE 4. Timing waveforms - Continued.

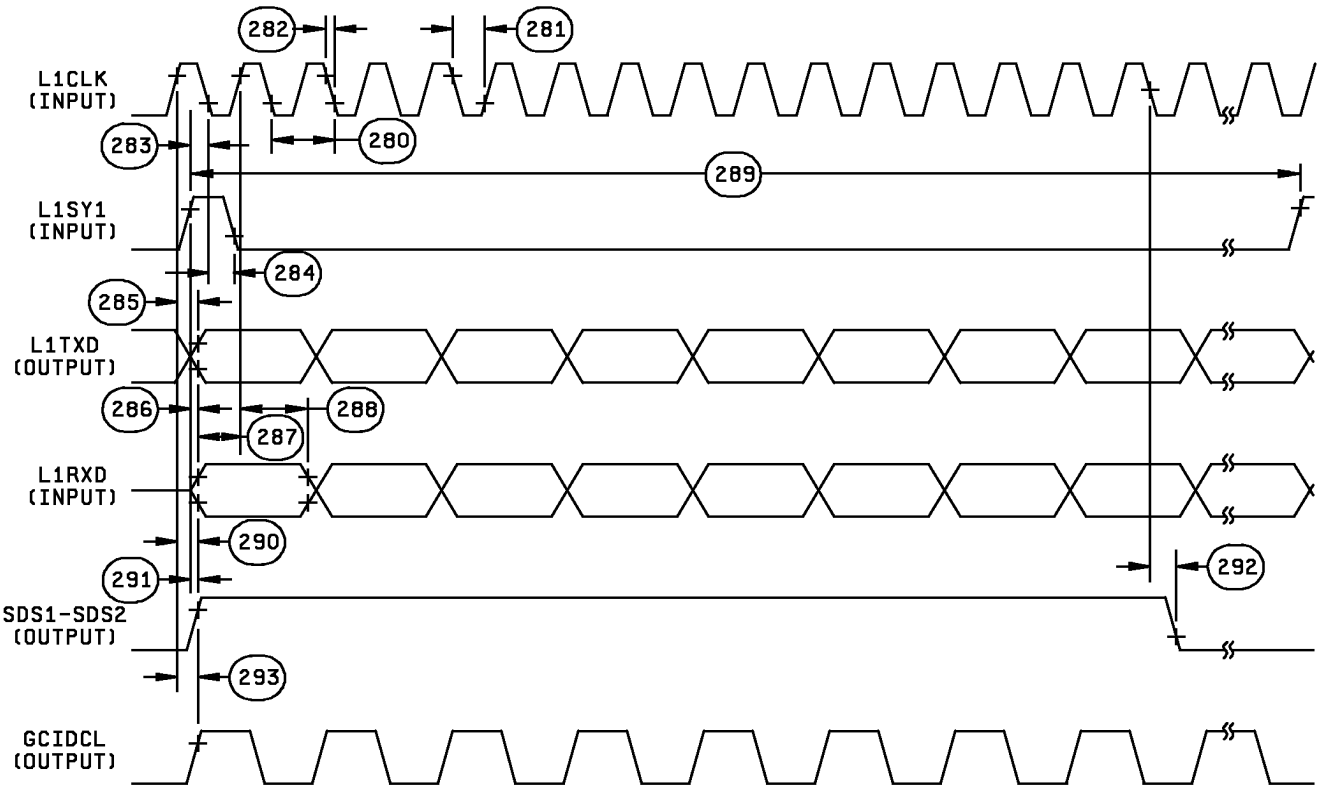


SERIAL COMMUNICATION PORT TIMING



IDL TIMING

FIGURE 4. Timing waveforms - Continued.



GCI TIMING

FIGURE 4. Timing waveforms - Continued.

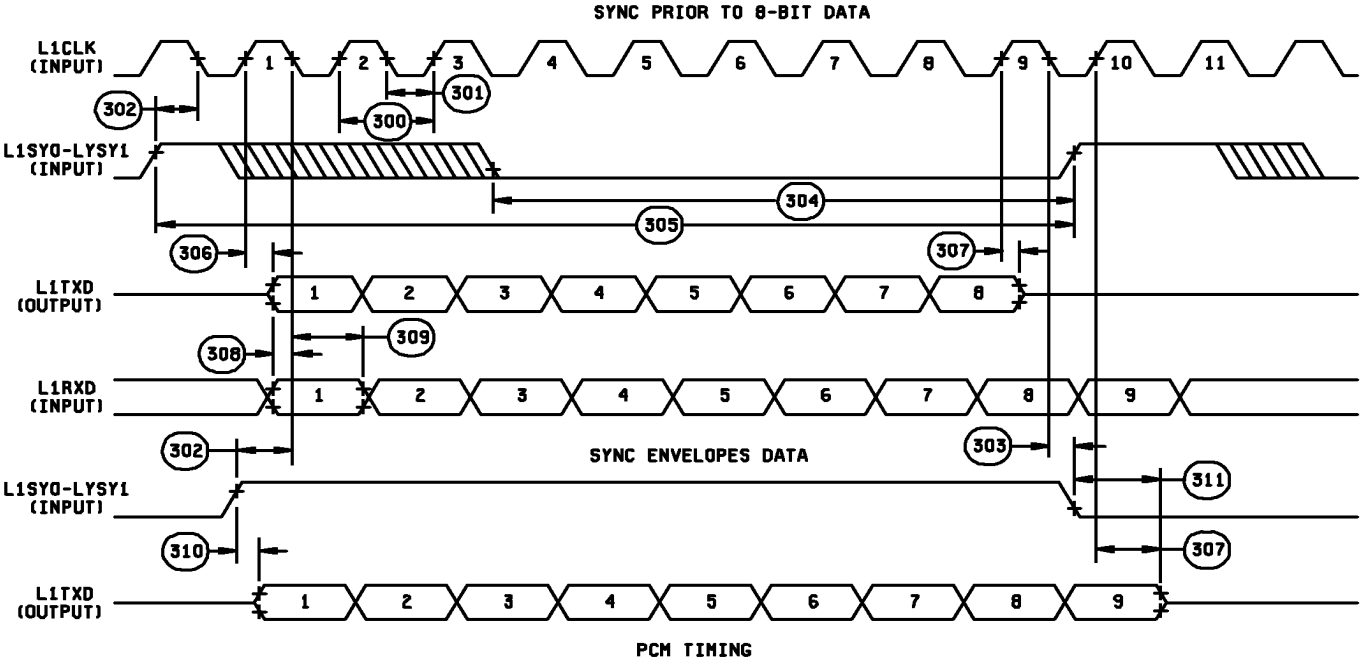


FIGURE 4. Timing waveforms - Continued.

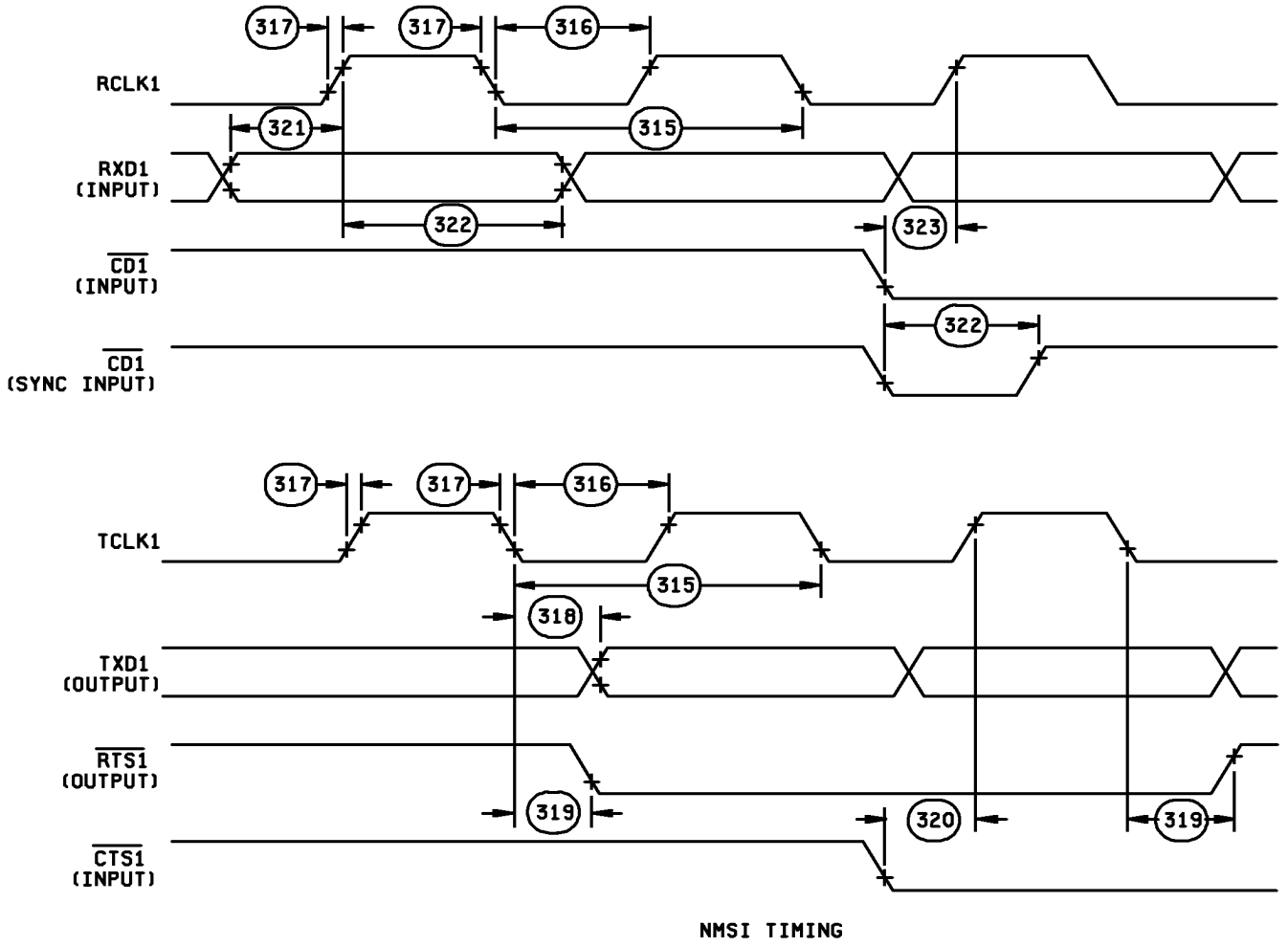


FIGURE 4. Timing waveforms - Continued.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample of 5 devices with zero failures shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	---
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	2, 8A, 10	2, 8A, 10	2, 8A, 10
Group D end-point electrical parameters (see 4.4)	2, 8A, 10	2, 8A, 10	2, 8A, 10
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 98-12-11

Approved sources of supply for SMD 5962-93159 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9315901QXA	18778	TS68302MR1B/C16
5962-9315901QXC	18778	TS68302MRB/C16
5962-9315901QYA	18778	TS68302MAB/C16

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
18778	Thomson Components and Tubes Corporation 40G Commerce Way Totowa, NJ 07511

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.