Signetics

54LS257A
Data Selector/Multiplexer

Quad 2-Line to 1-Line Data Selector/Multiplexer (3-State)

Product Specification

Military Logic Products

FEATURES
- **Multifunction capability**
- **Non-inverting data path**
- **3-State outputs**

DESCRIPTION
The 54LS257 has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources under control of a common Data Select input (S). The I_0 inputs are selected when the Select input is Low and the I_1 inputs are selected when the Select input is High. Data appears at the outputs in true (non-inverted) form from the selected outputs.

The 54LS257A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

Outputs are forced to a High impedance "off" state when the Output Enable input ($\overline{OE}$) is High. All but one device must be in the High impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. Design of the output enable signals must ensure that there is no overlap when outputs of 3-State devices are tied together.

ORDERING INFORMATION

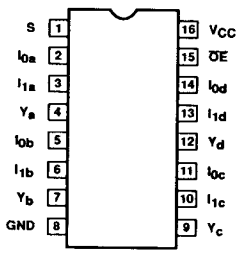
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54LS257A/BEA
16-Pin Ceramic FlatPack	54LS257A/BFA
20-Pin Ceramic LLCC	54LS257A/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54LS
S	Inputs	2LSUL
Other	Inputs	1LSUL
All	Outputs	30LSUL

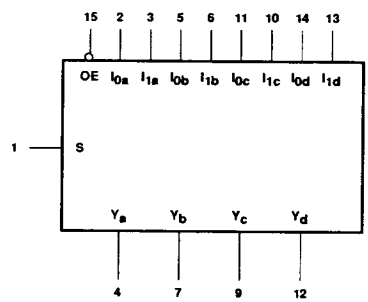
NOTE: A 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



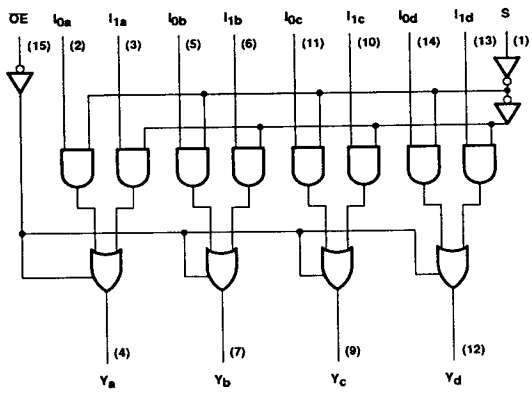
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

For LLCC pin assignments, see JEDEC Standard No. 2

FUNCTION TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{OE}$	S	I_0	I_1	Y
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High voltage level
L = Low voltage level
X = Don't care
(Z) = High impedance (off) state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1.0	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max			0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5	V
I_{OZH}	Offstate output current, High-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 2.7V				20	µA
I_{OZL}	Offstate output current, Low-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 0.4V				-20	µA
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V	S input			0.2	mA
			Other inputs			0.1	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V	S input			40	µA
			Other inputs			20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V	S input			-0.8	mA
			Other inputs			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-30		-130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max	I_{CCH} Outputs High		6.2	10	mA
			I_{CCL} Outputs Low		10	16	mA
			I_{CCZ} Outputs Off		12	19	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

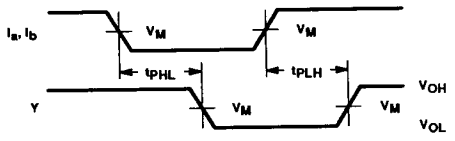
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1		18 18	ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 1		21 21	ns
t_{PZH}	Output enable to High level	Waveform 2		30	ns
t_{PZL}	Output enable to Low level	Waveform 3		30	ns
t_{PHZ}	Output disable from High level	Waveform 2, C_L = 5pF[5]		30	ns
t_{PLZ}	Output disable from Low level	Waveform 3, C_L = 5pF[5]		25	ns
t_{PHZ}	Output disable from High level	Waveform 2, C_L = 50pF		46	ns
t_{PLZ}	Output disable from Low level	Waveform 3, C_L = 50pF		27	ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and + 125°C, V_{CC} = 5.0V[6]

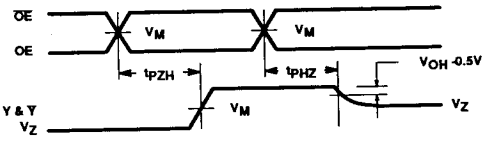
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1		23 23	ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 1		27 27	ns
t_{PZH}	Output enable to High level	Waveform 2		39	ns
t_{PZL}	Output enable to Low level	Waveform 3		39	ns
t_{PHZ}	Output disable from High level	Waveform 2, C_L = 5pF[5]		39	ns
t_{PLZ}	Output disable from Low level	Waveform 3, C_L = 5pF[5]		33	ns
t_{PHZ}	Output disable from High level	Waveform 2, C_L = 50pF		60	ns
t_{PLZ}	Output disable from Low level	Waveform 3, C_L = 50pF		35	ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all outputs open and all possible inputs grounded while achieving the stated output conditions.
5. Guaranteed by the 50pF limits, but not tested.
6. These parameters are guaranteed, but not tested.

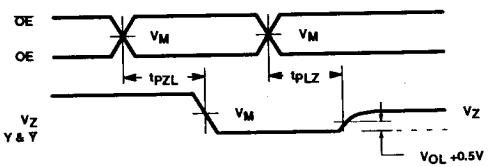
AC WAVEFORMS



Waveform 1. Waveform for Non-Inverting Outputs



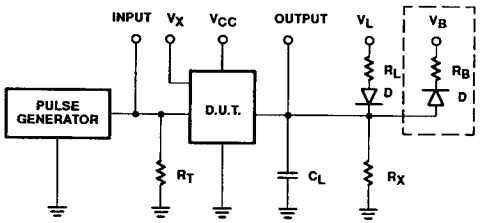
Waveform 2. 3-State Enable Time to High Level and Disable Time from High Level



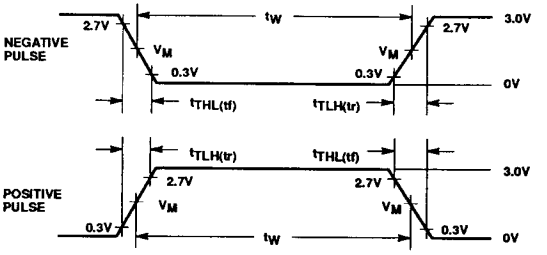
Waveform 3. 3-State Enable Time to Low Level and Disable Time from Low Level

FAMILY	V_M	V_{MZL}	V_{MZH}	V_Z
54LSXXX	1.3V	0.7V	1.9V	1.45V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 3-State Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS							
	R_L	R_X	V_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	110Ω	2.4kΩ	2.1V	1.3V	1MHz	500ns	≤15ns	≤6ns

Optional load for 54LSXXX only: R_B = 631Ω; V_B = 5.5V for all tests except T_{PHZ}; V_B = -0.6V for T_{PHZ} test.

DEFINITIONS:

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

APPLICATION DIAGRAM