Octal D-type transparent latch (3-State)

54ABT573

FEATURES

- 54ABT573 is the broadside pinout version of 54ABT373
- Inputs and outputs on opposite side of package allow easy interface to Microprocessors
- 3-State outputs for bus interfacing common output enable
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 54ABT573 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 54ABT573 device is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates. The 54ABT573 is functionally identical to the 54ABT373 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

ORDERING INFORMATION

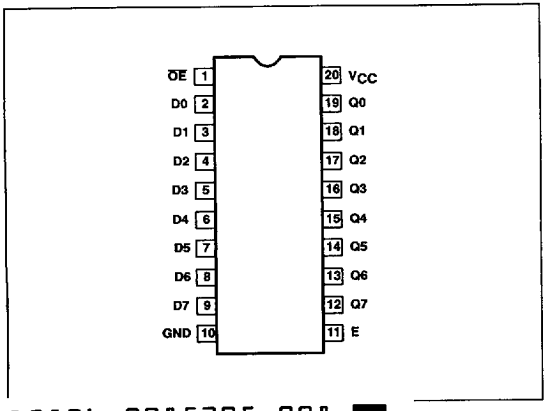
DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
20-Pin Ceramic DIP	54ABT573/BRA	GDIP1-T20
20-Pin Ceramic LLCC	54ABT573/B2A	CQCC2-N20

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

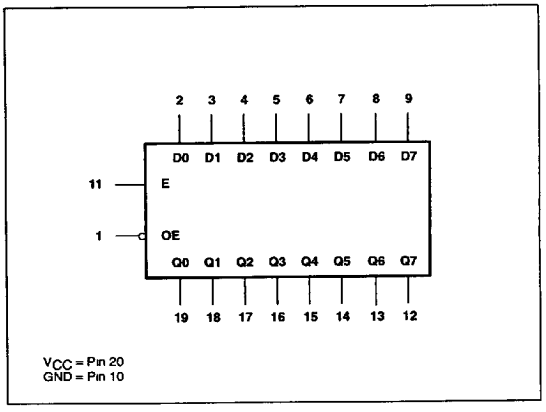
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output enable input (active Low)
2, 3, 4, 5 6, 7, 8, 9	D0 - D7	Data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q0 - Q7	3-State outputs
11	E	Enable input (active High)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

PIN CONFIGURATION

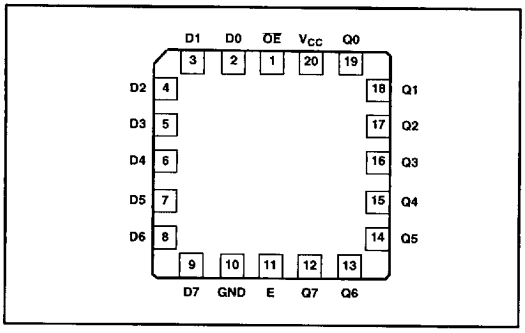


LOGIC SYMBOL



Octal D-type transparent latch (3-State) 54ABT573

LLCC LEAD CONFIGURATION

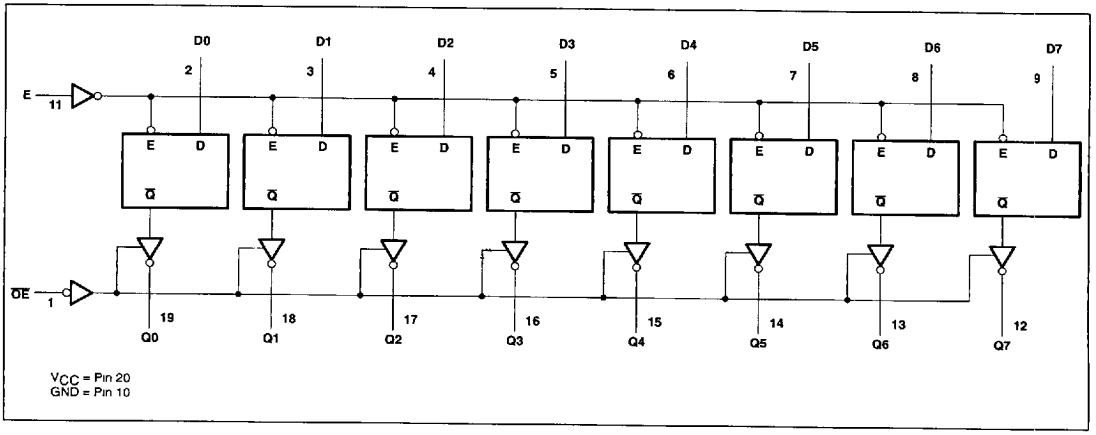


FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
OE	E	Dn	REGISTER	Q0 - Q7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	l h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X Dn	NC Dn	Z Z	Disable outputs

H = High voltage level
h = High voltage level one setup time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one setup time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage range		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage range[3]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage range[3]	Output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	Output in Low state	96	mA
T_{STG}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		-24	mA
I_{OL}	Low-level output current		48	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-55	+125	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = MAX, V_I = V_{IL} or V_{IH} unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -55 to +125°C		
			MIN	TYP[2]	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V, I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output to voltage	V_{CC} = 4.5V; I_{OH} = -3mA	2.5	3.0		2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA	3.0	3.5		3.0		V
		V_{CC} = 4.5V; I_{OH} = -24mA	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 48mA		0.42	0.55		0.55	V
I_I	Input leakage current	V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_O = 2.7V, V_I = V_{IL} or 3.0V[8]		0.5	10		10	µA
I_{OZL}	3-State output Low current	V_O = 0.5V, V_I = V_{IL} or 3.0V[8]		-0.5	-10		-10	µA
I_O	Short-circuit output current[4]	V_O = 2.5V, V_I = GND or V_{CC}	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	Outputs High, V_I = GND or V_{CC}		0.5	250		250	µA
I_{CCL}		Outputs Low, V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		Outputs 3-State, V_I = GND or V_{CC}		0.5	250		250	µA
ΔI_{CC}	Additional supply current per input pin[5]	One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA
I_{OFF}	Power OFF leakage current	V_{CC} = 0.0V, V_I or $V_O \leq$ 4.5V	-100	1.0	100			µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V, V_O = 5.5V			50		50	µA

AC ELECTRICAL CHARACTERISTICS

GND = 0V, $t_R = t_F = 2.5ns$, $C_L = 50pF$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -55°C to +125°C, V_{CC} = +5.0V ± 10%		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	Waveform 13	1.9 2.2	3.2 4.2	5 4 5.7	1.4 1.6	6.4 6.7	ns ns
t_{PLH} t_{PHL}	Propagation delay E to Qn	Waveform 12	2.2 3.2	4.0 5.2	6.1 6.7	2.0 2 8	7.1 7.5	ns ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	Waveform 15 Waveform 16	1.2 2.7	3.2 4.7	4.7 6.2	0.8 2.0	6.2 7.2	ns ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	Waveform 15 Waveform 16	2.5 2.0	4.9 4.2	6.4 6.0	2.2 1.4	7.7 7.0	ns ns

AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F = 2.5ns$, $C_L = 50pF$, $R_L = 500\Omega$

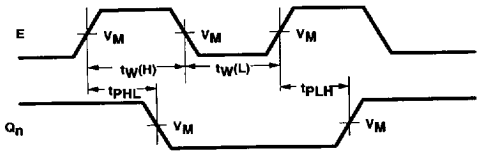
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -55°C to +125°C, V_{CC} = +5.0V ± 0.5V		
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time[6] Dn to E	Waveform 14	2.0 2.0			2.5 2.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time6 Dn to E	Waveform 14	2 0 2.0			2.5 2.5		ns ns
$t_w(H)$	E pulse width[7] High or Low	Waveform 12	3.3			3.3		ns

NOTES:

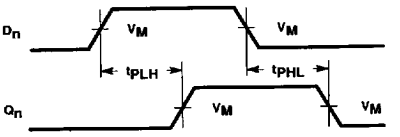
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
4. Not more than one output should be tested at a time, and the4 duration of the test should not exceed one second.
5. This is the increase in supply current for each input at 3.4V.
6. t_{set} and t_{hold} limits that are less than 3.0ns are guaranteed, but are only tested to a 3.0ns limit due to tester limitations.
7. t_w limits that are less than 6.0ns are guaranteed, but are only tested to a 6 0ns limit due to tester limitations.
8. To accommodate tester limitations, I_{OZ} tests are tested with V_{IH} = 3.0V, but 2.0V V_{IH} is guaranteed.

AC WAVEFORMS

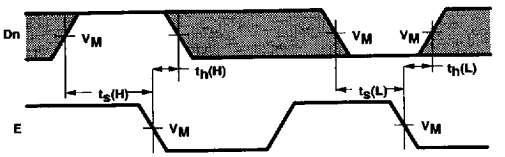
V_M = 1.5V, V_{IN} = GND to 3.0V



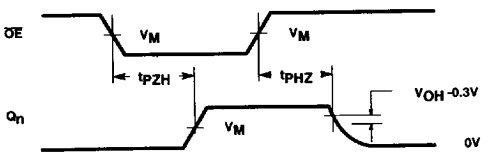
Waveform 12. Propagation Delay, Enable to Output, and Enable Pulse Width



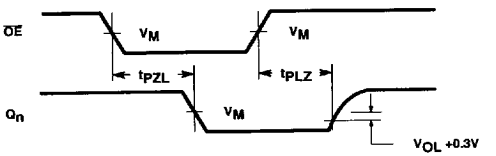
Waveform 13. Propagation Delay Data to Outputs



Waveform 14. Data Setup and Hold Times

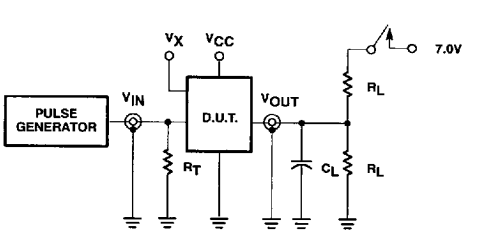


Waveform 15. 3-State Output Enable Time to High Level and Output Disable Time from High Level

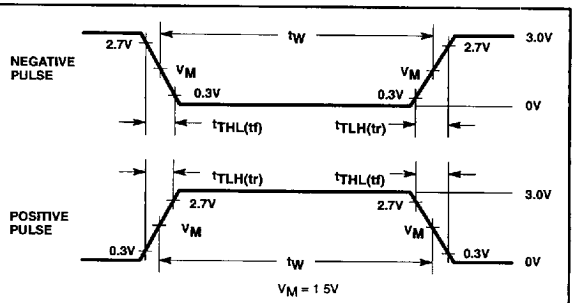


Waveform 16. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed open

INPUT PULSE REQUIREMENTS					
Family	Amplitude	Rep. Rate	t_W	t_R	t_F
54ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.