MOTOROLA

Quad 2-Input Multiplexer/Latch

ELECTRICALLY TESTED PER:
MPG 10573

The 10573 is a quad two channel multiplexer with latch. It incorporates common clock and common data select inputs. The select input determines which data input is enabled. A high (H) level enables data inputs D00, D20, and D30 and a low (L) level enables data inputs D01, D11, D21, and D31. Any change on the data input will be reflected at the outputs while the clock is low.

The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not effect the output information.

- 380 mW Max/Pkg (No Load)
- t_{pd} = 2.5 ns typ (All Output Loaded)
- t_r, t_f = 2.0 ns typ (20% - 80%)

3

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
Q0	1	5	2	51 Ω to V_{TT}
Q1	2	6	3	51 Ω to V_{TT}
D11	3	7	4	GND
D10	4	8	5	OPEN
D01	5	9	7	GND
D00	6	10	8	OPEN
Clock	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
Select	9	13	12	OPEN
D31	10	14	13	GND
D30	11	15	14	OPEN
D21	12	16	15	GND
D20	13	1	17	OPEN
Q3	14	2	18	51 Ω to V_{TT}
Q2	15	3	19	51 Ω to V_{TT}
V_{CC}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

TRUTH TABLE

Inputs		Output
Select	Clock	$Q0_{n+1}$
H	L	D00
L	L	D01
Ø	L	$Q0_n$

Ø = Don't Care

Military 10573

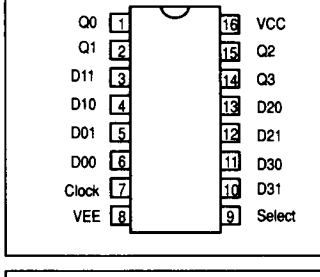
MPO

AVAILABLE AS

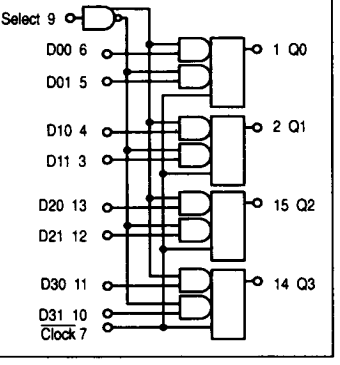
1) JAN: N/A
2) SMD: N/A
3) 883: 10573/BXAJC
X = CASE OUTLINE AS FOLLOWS:

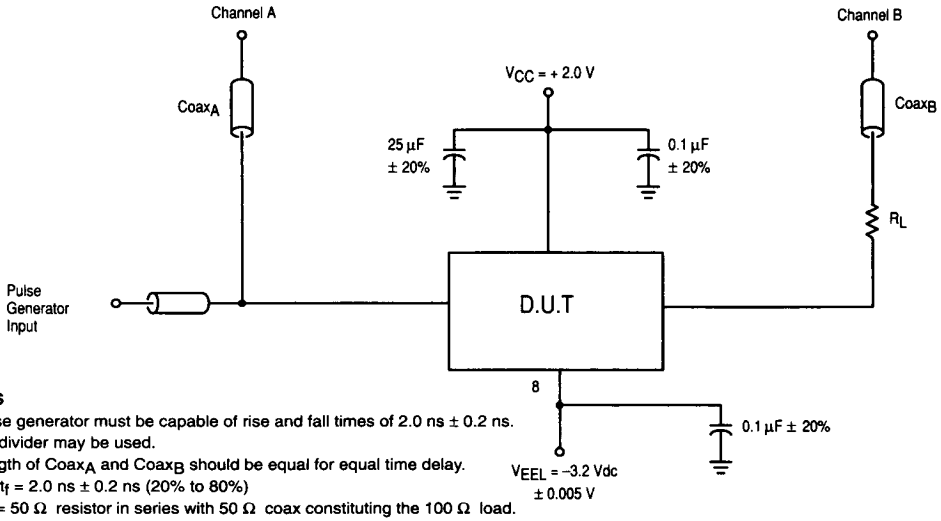
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns.
2. 2:1 divider may be used.
3. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
4. $t_r = t_f$ = 2.0 ns ± 0.2 ns (20% to 80%)
5. R_L = 50 Ω resistor in series with 50 Ω coax constituting the 100 Ω load.
6. Unused outputs should be loaded 100 Ω to ground

NOTES

V_{IN} has the following characteristics:

a) PW ≥ 20 ns.
b) f_{IN} = 1.0 MHz.
c) t_r and t_f = 1.0 ns ± 0.1 ns. (20% - 80%)

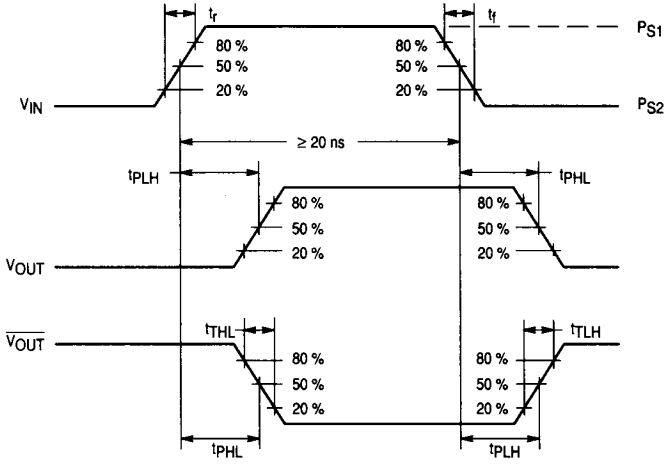


Figure 1. Switching Test Circuit and Waveforms

10573
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	3, 5, 10, 12				8	16	1, 2, 14, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	3 - 7, 9 - 13	3, 5, 10, 12	7, 9	3 - 7, 9 - 13	8	16	1, 2, 14, 15
V_{OL1}	Low Output Voltage	- 1.85	- 1.60	- 1.82	- 1.525	- 1.92	- 1.635	V	3 - 7, 9 - 13	3, 5, 7, 10 - 13	3 - 7, 9 - 13	7, 9	8	16	1, 2, 14, 15
V_{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	- 0.88	V					8	16	1, 2, 14, 15
I_{EE}	Power Supply Drain Current	- 66		- 73		- 73		mA					8	16	8
I_{IH}	Input Current High		250		425		425	µA	7, 9				8	16	7, 9
I_{IH1}	Input Current High		295		500		500	µA	3 - 6, 10 - 13				8	16	3 - 7, 10 - 13
I_{IL}	Input Current Low	0.5		0.3		0.5		µA			3 - 7, 9 - 13		8	16	3 - 7, 10 - 13

10573
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND							
		Subgroup 9		Subgroup 10		Subgroup 11										
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	V_{IH}	V_{IL}	P. U. T.
t_{TLH}	Rise Time	1.5	3.5	1.4	7.5	1.0	4.2	ns	3 - 7, 9 - 13	1, 2, 14, 15	16	8	3, 5, 10, 12			1, 2, 14, 15
t_{THL}	Fall Time	1.5	3.5	1.4	7.5	1.0	4.2	ns	3 - 7, 9 - 13	1, 2, 14, 15	16	8	3, 5, 10, 12			1, 2, 14, 15
t_{pd}	Propagation Delay Select to Q	1.3	5.7	1.2	7.0	1.0	6.5	ns	3 - 7, 9 - 13	1, 2, 14, 15	16	8	3, 5, 10, 12			1, 2, 14, 15
t_{pd}	Propagation Delay Data to Q	1.0	3.5	1.1	5.5	0.8	3.9	ns	3 - 7, 9 - 13	1, 2, 14, 15	16	8	3, 5, 10, 12			1, 2, 14, 15
t_{pd}	Propagation Delay Clock to Q	1.6	6.8	1.4	7.5	1.6	7.5	ns	3 - 7, 9 - 13	1, 2, 14, 15	16	8	3, 5, 10, 12			1, 2, 14, 15
t_{set}	Setup Time Select to Q	3.0		3.0		4.0		ns	3 - 7, 9 - 13	1, 2, 14, 15	16	8		9	9	1
t_{set}	Setup Time Data to Q	2.0		2.0		2.0		ns	3 - 7, 9 - 13	1, 2, 14, 15	16	8		5, 6	5, 6	1
t_{hold}	Hold Time Data Input	2.5		2.5		2.5		ns	3 - 7, 9 - 13	1, 2, 14, 15	16	8		9	9	1
t_{hold}	Hold Time Select Input	1.5		1.5		1.5		ns	3 - 7, 9 - 13	1, 2, 14, 15	16	8		5, 6	5, 6	1