

Power management system IC

Features

- Two 5V low-drop voltage regulators (250mA, 100mA continuous mode)
- Low stand-by current: V_{BAT} stby, 7 μ A; V_1 stby, 45 μ A, (75 μ A in cycl. sense)
- Window watchdog and fail-safe output
- Interrupt output
- Wake-up logic with cyclic contact monitoring
- LIN 2.1 compliant (SAEJ2602 compatible) transceiver
- 24 bit SPI interface for mode control and diagnostic
- Output drivers
- 4 High side drivers for e.g. LED or HALL ($R_{DSon,typ} = 7 \Omega$)
- 1 High side driver Out_HS ($R_{DSon,typ} = 1 \Omega$)
- 2 Relay drivers ($R_{DSon,typ} = 2 \Omega$)
- Outputs are short circuit protected
- 2 Op amp's for current sensing in GND return lines
- Temperature warning and thermal shutdown



Applications

- Automotive ECU' s such as door zone and body control modules.

Description

The L9952GXP is a power management system IC containing two low drop regulators with advanced contact monitoring and additional peripheral functions.

The integrated standard serial peripheral interface (SPI) controls all L9952GXP operation modes and provides driver diagnostic functions.

Table 1. Device summary

| Package | Order codes | |
|-------------|-------------|---------------|
| | Tube | Tape and reel |
| PowerSSO-36 | L9952GXP | L9952GXPTR |

Contents

| | | |
|----------|---------------------------------------|-----------|
| 1 | Pin definitions and functions | 8 |
| 2 | Description | 11 |
| 2.1 | Voltage regulator | 11 |
| 2.1.1 | Voltage regulator: V1 | 11 |
| 2.1.2 | Voltage regulator: V2 | 11 |
| 2.2 | Power control in operating modes | 12 |
| 2.2.1 | Active mode | 12 |
| 2.2.2 | Flash mode | 12 |
| 2.2.3 | V1 standby mode | 12 |
| 2.2.4 | VBAT standby mode | 12 |
| 2.3 | Wake up events | 13 |
| 2.4 | Functional overview (truth table) | 14 |
| 2.5 | Wake up inputs | 16 |
| 2.6 | Hall sensor ports: WU3,4, Dig_Out 3,4 | 16 |
| 2.7 | Interrupt | 17 |
| 2.8 | Cyclic contact supply | 17 |
| 2.9 | Window – watchdog | 17 |
| 2.10 | Fail safe output | 19 |
| 2.11 | Reset – generator | 19 |
| 2.12 | V1, V2 fail | 20 |
| 2.13 | Low side driver outputs Rel1, Rel2 | 20 |
| 2.14 | PWM inputs | 20 |
| 2.15 | Operational amplifiers | 21 |
| 2.16 | LIN bus interface | 21 |
| 2.17 | Error handling | 22 |
| 2.17.1 | Dominant TxD time out | 22 |
| 2.17.2 | Short to battery time out | 22 |
| 2.17.3 | Short to ground mode | 22 |
| 2.18 | Wake up (from LIN) | 22 |
| 2.18.1 | Normal wake up | 22 |
| 2.18.2 | Wake up from short to GND condition | 22 |

| | | |
|----------|--|-----------|
| 2.18.3 | RxD pin in V1 standby | 22 |
| 2.19 | LINPU | 23 |
| 2.20 | Serial Peripheral Interface (SPI) | 23 |
| 2.20.1 | Chip Select Not (CSN) | 23 |
| 2.20.2 | Serial Data In (DI) | 24 |
| 2.20.3 | Serial Data Out (DO) | 24 |
| 2.20.4 | Serial Clock (CLK) | 24 |
| 2.20.5 | Data registers | 24 |
| 3 | Protection and diagnosis | 25 |
| 3.1 | Power supply fail | 25 |
| 3.1.1 | Over voltage | 25 |
| 3.1.2 | Under voltage | 25 |
| 3.2 | Temperature warning and thermal shutdown | 25 |
| 3.3 | SPI diagnosis | 25 |
| 3.4 | High side driver outputs | 27 |
| 3.5 | Low side driver outputs Rel1, Rel2 | 27 |
| 4 | Absolute maximum ratings | 28 |
| 5 | ESD protection | 29 |
| 6 | Thermal data | 30 |
| 6.1 | Operating junction temperature | 30 |
| 6.2 | Temperature warning and thermal shutdown | 30 |
| 6.3 | Package and PCB thermal data | 31 |
| 7 | Electrical characteristics | 34 |
| 7.1 | Supply and supply monitoring | 34 |
| 7.2 | Oscillator | 35 |
| 7.3 | Power-on reset (Vs) | 35 |
| 7.4 | Voltage regulator V1 | 35 |
| 7.5 | Voltage regulator V2 | 36 |
| 7.6 | Reset generator (V1 supervision) | 37 |
| 7.7 | Watchdog | 37 |

| | | |
|-----------|---|-----------|
| 7.8 | High side outputs | 39 |
| 7.8.1 | Output (Out_HS) | 39 |
| 7.8.2 | Outputs (OUT1...4) | 40 |
| 7.9 | Relay drivers | 40 |
| 7.10 | Wake up inputs (WU1..WU4) | 41 |
| 7.11 | Wake up input (INH) | 42 |
| 7.12 | LIN | 42 |
| 7.13 | Operational amplifier | 47 |
| 7.14 | SPI | 48 |
| 7.14.1 | Input: CSN | 48 |
| 7.14.2 | Inputs: CLK, DI, PWM 1, PWM 2 | 48 |
| 7.14.3 | Input PWM 2 Vth for flash mode | 49 |
| 7.14.4 | DI timing | 49 |
| 7.14.5 | DO, FSO, Dig_Out3,4 | 50 |
| 7.14.6 | DO timing | 50 |
| 7.14.7 | CSN timing | 51 |
| 8 | SPI control and status registers | 54 |
| 8.1 | SPI registers | 54 |
| 8.1.1 | Control register 0 | 55 |
| 8.1.2 | Control register 1 | 56 |
| 8.1.3 | Control register 2 | 59 |
| 8.1.4 | Status register 0 | 61 |
| 8.1.5 | Status register 1 | 62 |
| 9 | Package and packing information | 64 |
| 9.1 | ECOPACK® packages | 64 |
| 9.2 | PowerSSO-36 package information | 64 |
| 9.3 | PowerSSO-36 packing information | 66 |
| 10 | Revision history | 67 |

List of tables

| | | |
|-----------|--|----|
| Table 1. | Device summary | 1 |
| Table 2. | Pins definitions and functions | 8 |
| Table 4. | Functional overview (truth table) | 14 |
| Table 5. | Absolute maximum ratings | 28 |
| Table 6. | ESD protection | 29 |
| Table 7. | Operating junction temperature | 30 |
| Table 8. | Temperature warning and thermal shutdown | 30 |
| Table 9. | Thermal parameters | 33 |
| Table 10. | Supply and supply monitoring. | 34 |
| Table 11. | Oscillator. | 35 |
| Table 12. | Power-on Reset (Vs) | 35 |
| Table 13. | Voltage regulator V1 | 35 |
| Table 14. | Voltage regulator V2. | 36 |
| Table 15. | Reset generator | 37 |
| Table 16. | Watchdog | 37 |
| Table 17. | High side outputs (Out_HS) | 39 |
| Table 18. | High side outputs (OUT 1..4) | 40 |
| Table 19. | Relay drivers. | 40 |
| Table 20. | Wake up inputs(WU1...WU4) | 41 |
| Table 21. | Wake up input (INH) | 42 |
| Table 22. | LIN receiver | 42 |
| Table 23. | LIN DC parameters. | 43 |
| Table 24. | LIN transmitter | 44 |
| Table 25. | LIN timing | 44 |
| Table 26. | LIN DC values. | 45 |
| Table 27. | Operational amplifier. | 47 |
| Table 28. | SPI (Input CSN) | 48 |
| Table 29. | Inputs: CLK, DI, PWM 1, PWM 2 | 48 |
| Table 30. | Input PWM2 Vth for flash mode | 49 |
| Table 31. | DI timing | 49 |
| Table 32. | DO, FSO, Digout3,4 | 50 |
| Table 33. | DO timing | 50 |
| Table 34. | CSN timing | 51 |
| Table 35. | SPI registers | 54 |
| Table 36. | Control register 0 | 55 |
| Table 37. | Configuration bit HSxx | 55 |
| Table 38. | Configuration bit OUT_HSx | 55 |
| Table 39. | Configuration bit RELx | 55 |
| Table 40. | Configuration bit On_V2x | 55 |
| Table 41. | Configuration bit TRIG, GO_VBAT, GO_V1 | 56 |
| Table 42. | Control register 1 | 56 |
| Table 43. | Configuration bit Wx | 56 |
| Table 44. | Configuration bit Ux | 57 |
| Table 45. | Configuration bit Lx | 57 |
| Table 46. | Configuration bit Txx. | 58 |
| Table 47. | Configuration bit INT_enable | 58 |
| Table 48. | Control register 2 | 59 |
| Table 49. | Configuration bit OLT_HSx, VSLOCK Out, O_HS_REC, LINPU and TXD_TOUT. | 59 |

| | | |
|-----------|---|----|
| Table 50. | Configuration bit LEVx | 59 |
| Table 51. | Configuration bit ICxx | 60 |
| Table 52. | Configuration bit LIN slope, LS_ovuv and ICMP | 60 |
| Table 53. | Status register 0 | 61 |
| Table 54. | Configuration bit HSx_OL, HSx_OC and Relx_OC | 61 |
| Table 55. | Configuration bit SHT5V2, WUx, INH, LIN and Cold Start | 61 |
| Table 56. | Status register 1 | 62 |
| Table 57. | Configuration bit OV, UV, TW, TSDx and Vx Fail | 62 |
| Table 58. | Configuration bit STx | 62 |
| Table 59. | Configuration bit Rx, WDx, TRIG, SHT_GND, SHT_BAT and DOM_TXD | 63 |
| Table 60. | PowerSSO-36 mechanical data | 64 |
| Table 61. | Document revision history | 67 |

List of figures

| | | |
|------------|---|----|
| Figure 1. | Block diagram | 8 |
| Figure 2. | Pins configuration | 10 |
| Figure 3. | Operating modes, main states | 15 |
| Figure 4. | Watchdog | 18 |
| Figure 5. | FSO | 19 |
| Figure 6. | NReset | 19 |
| Figure 7. | Lin master pull up | 21 |
| Figure 8. | Protection and diagnosis | 26 |
| Figure 9. | PowerSSO-36 PC board. | 31 |
| Figure 10. | PowerSSO-36 thermal resistance junction ambient Vs. PCB copper area (V1 ON) | 32 |
| Figure 11. | PowerSSO-36 thermal impedance junction ambient single pulse (V1 ON) | 32 |
| Figure 12. | PowerSSO-36 thermal fitting model (V1 ON) | 33 |
| Figure 13. | Watchdog timing | 38 |
| Figure 14. | Watchdog, closed and open window tolerances and save trigger area | 39 |
| Figure 15. | LIN transmit, receive timing | 46 |
| Figure 16. | SPI - Input timing | 51 |
| Figure 17. | SPI - Edges timing | 52 |
| Figure 18. | SPI - CSN low to high transition | 53 |
| Figure 19. | SPI - High to low transition | 53 |
| Figure 20. | PowerSSO-36 package dimensions | 64 |
| Figure 21. | PowerSSO-36 tube shipment (no suffix). | 66 |
| Figure 22. | PowerSSO-36 tape and reel shipment (suffix "TR") | 66 |

1 Pin definitions and functions

Figure 1. Block diagram

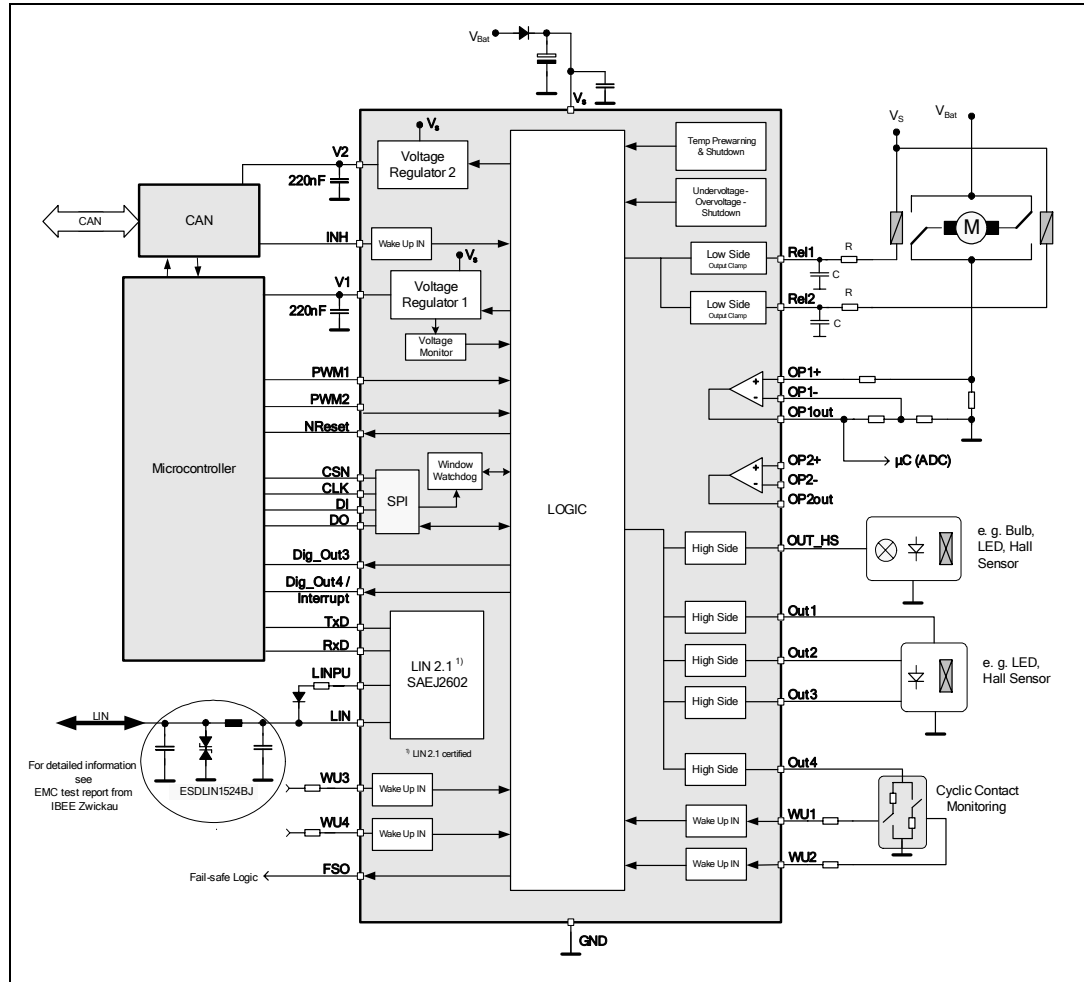


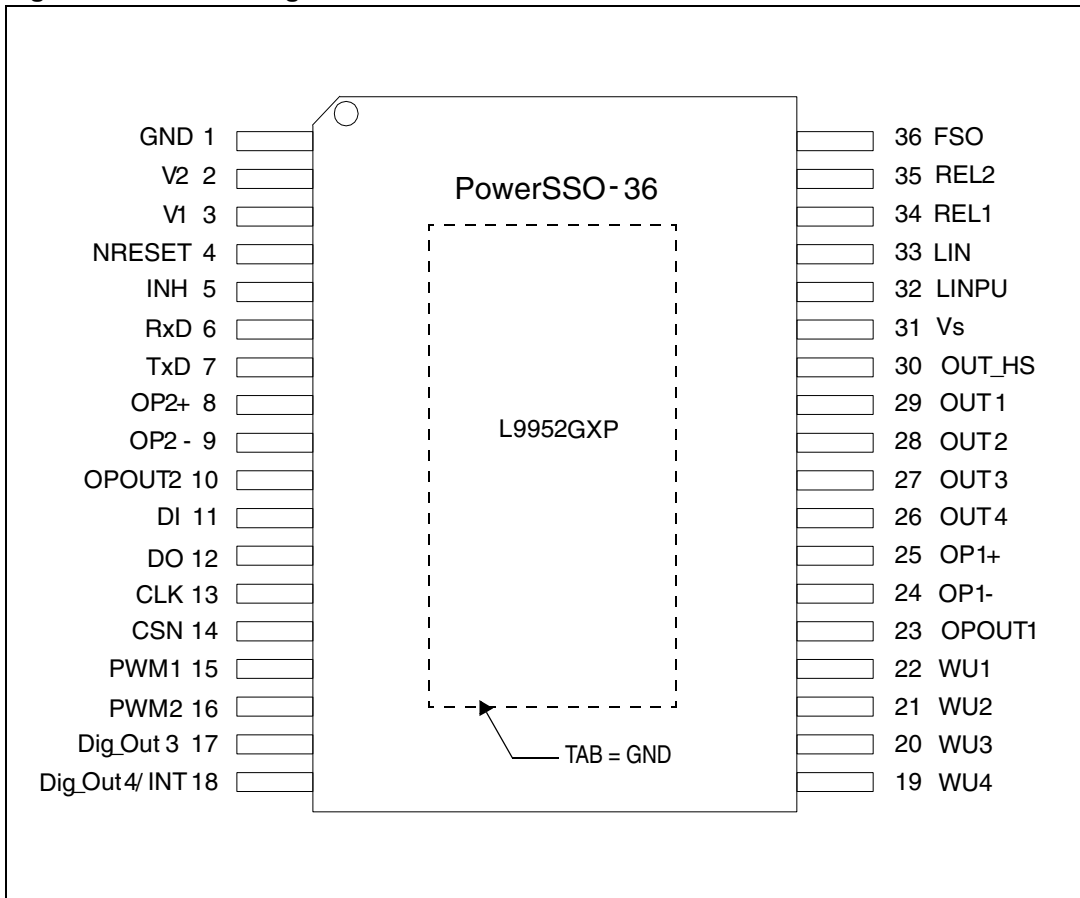
Table 2. Pins definitions and functions

| Pin name | PowerSS0-36 | Function |
|----------|-------------|--|
| GND | 1 | Ground |
| V2 | 2 | Voltage regulator 2 output : 5 V supply for external loads e.g. IR receiver, potentiometer |
| V1 | 3 | Voltage regulator 1 output : 5 V supply e.g. micro controller, Can transceiver |
| NReset | 4 | NReset output to micro controller - Internal pull-up of typ. 100KΩ (reset state = low) |
| INH | 5 | Wake-up input e.g. from CAN transceiver |
| RxD | 6 | Receiver output of the LIN 2.1 transceiver |

Table 2. Pins definitions and functions (continued)

| Pin name | PowerSS0-36 | Function |
|---------------------|-------------|--|
| TxD | 7 | Transmitter input of the LIN 2.1 transceiver |
| OP2+ | 8 | Non inverting input of operational sense amplifier |
| OP2- | 9 | Inverting input of operational sense amplifier |
| OP2 _{OUT} | 10 | Output of operational sense amplifier |
| DI | 11 | SPI : serial data input |
| DO | 12 | SPI : serial data output |
| CLK | 13 | SPI : serial clock input |
| CSN | 14 | SPI : chip select not input |
| PWM1 | 15 | Pulse width modulation input |
| PWM2 | 16 | Pulse width modulation input |
| Dig_Out3 | 17 | Digital output |
| Dig_Out4/INT | 18 | Digital output (configurable as Interrupt Output) |
| Wu _{4..1} | 19 to 22 | Wake-up input: input pins for static or cyclic monitoring of external contacts |
| OP1 _{OUT} | 23 | Output of operational sense amplifier |
| OP1- | 24 | Inverting input of operational sense amplifier |
| OP1+ | 25 | Non inverting input of operational sense amplifier |
| Out _{4..1} | 26 to 29 | High side driver (7 Ω , typ.) - to supply e.g. LED' s, HALL sensors or external contacts |
| Out_HS | 30 | High side drivers (1 Ω , typ.) - to supply e.g. LED' s, Bulbs, HALL sensors or external contacts |
| Vs | 31 | Power supply voltage |
| LINPU | 32 | LIN master pull up |
| LIN | 33 | LIN bus line |
| Rel1 | 34 | Low side driver (2 Ω , typ.) - e.g. relay |
| Rel2 | 35 | Low side driver (2 Ω , typ.) - e.g. relay |
| FSO | 36 | Fail safe output - used to supervise or control applications in case of watchdog and/or V1 under-voltage failure (e.g. to activate emergency lights) |

Figure 2. Pins configuration



2 Description

2.1 Voltage regulator

The L9952GXP contains 2 independent and fully protected low drop voltage regulators, which are designed for very fast transient response.

The output voltage is stable with loads capacitors $\geq 220\text{nF}$.

2.1.1 Voltage regulator: V1

The voltage regulator V1 provides 5V supply voltage and up to 250mA continuous load current for the external digital logic (micro controller, CAN transceiver ...). In addition the regulator V1 drives the L9952GXP internal 5V loads. The voltage regulator is protected against overload and over-temperature. An external reverse current protection has to be provided by the application circuitry to prevent the output capacitor from being discharged by negative transients or low input voltage. The output voltage precision is better than $\pm 2\%$ (incl. temperature drift and line-/load regulation) for operating mode; respectively $\pm 3\%$ during low current mode. Current limitation of the regulator ensures fast charge of external bypass capacitors. The output voltage is stable for ceramic load capacitors $\geq 220\text{nF}$.

If device Temperature exceeds TSD1 threshold, all outputs (Hsx, Lsx, V2, LIN) will be deactivated except V1. Hence the micro controller has the possibility for interaction or error logging. In case of exceeding TSD2 threshold ($\text{TSD2} > \text{TSD1}$), also V1 will be deactivated (see state chart Fig. 3.1: "Protection and diagnosis"). A timer is started and the voltage regulator is deactivated for $t_{\text{TSD}} = 1\text{sec}$. During this time, all other wakeup sources (CAN, LIN, and WU1...4) are disabled. After 1 sec, the voltage regulator will try to restart automatically. If TSD2 occurs within one minute and for 8 consecutive times, the L9952GXP enters the V_{BAT} - standby mode.

In case of short to GND at "V1" after initial turn on ($V1 < 2\text{V}$ for at least 4ms) the L9952GXP enters the V_{BAT} - standby mode. Reactivation (wake-up) of the device can be achieved with signals from CAN, LIN, WU1..4, SPI.

2.1.2 Voltage regulator: V2

The voltage regulator V2 supplies additional 5V loads (e.g. Logic components, external sensors, external potentiometers). The continuous load current is 50mA. The regulator provides accuracy better than $\pm 3\%$ @ 50mA (4% @ 100mA) load current.

In case of short to GND at "V2" after initial turn on ($V2 < 2\text{V}$ for at least 4ms) the V2 regulator is switched off. Micro processor has to send a clear command to reactivate the V2 regulator.

V2 is protected against:

- Overload
- Over temperature
- Short circuit (short to ground and battery supply voltage)
- Reverse biasing

2.2 Power control in operating modes

The L9952GXP can be operated in 4 different operating modes:

- Active
- Flash
- V_1 - standby
- V_{BAT} - standby

A cyclic monitoring of wake-up inputs is available in stand-by modes.

2.2.1 Active mode

All functions are available.

2.2.2 Flash mode

To disable the watchdog feature a FLASH program mode is available.

The mode can be entered by $V_{PWM2} \geq 9V$

In this case all other functions are the same as in active mode

Watchdog can be disabled as well as soon as L9952GXP enters the V1 standby mode (see section 2.9 for details)

Note: "High" level for flash mode selection is $V_{PWM2} \geq 9V$. For all other operation modes, standard 5V logic signals are required. For proper operation PWM1 must not be set to a voltage level above standard 5V logic.

2.2.3 V_1 standby mode

Outputs and internal loads are switched off. To supply the micro controller in a low power mode, the voltage regulator1 (V1) remains active. The intention of the V1 standby mode is to preserve the RAM contents. A cyclic contact supply and wake-up input sense feature (for cyclic monitoring of external contacts) can be activated by SPI.

2.2.4 V_{BAT} standby mode

To achieve minimum current consumption during V_{BAT} standby mode, all L9952GXP functions (except the ones for wake up functionality) are switched off.

In V_{BAT} - standby mode the current consumption of the L9952GXP is reduced to 7 μ A, typical (without cyclic sense feature selected).

The transitions from active mode to either V_1 -standby or V_{BAT} - standby are controlled by SPI.

V_{BAT} - standby mode is dominant; i.e. if both bits, V_1 - standby and V_{BAT} - standby are set to "1", the L9952GXP will enter V_{BAT} - standby mode.

2.3 Wake up events

A wake-up from standby mode will switch the device to active mode. This can be initiated by one or more of the following sources:

- Change of the LIN state at LIN bus interfaces
- A current at the INH pin ($I \geq 200\mu\text{A}$) controlled by the CAN-transceiver (the CAN transceiver is not a part of the IC).
- Positive/negative edge at wake up pins WU1...WU4 -> change of level after going into stand-by
- Change of open-load state at OUT1 to 4
- SPI access in V1-standby mode (CSN is low and first rising edge on CLK)

Table 3. Wake up events

| Wake up source | Description |
|--------------------------|--|
| LIN | Always active |
| INH | Always active |
| WU1...4 | Can be individually disabled via SPI |
| Open Load at HS outputs | Can be individually disabled via SPI |
| SPI Access | Always active (except in V_{BAT} - standby mode) |
| High level at PWM2 input | $V_{\text{PWM2}} > 9\text{V}$ ⁽¹⁾ |

1. Only if internal oscillator is running (e. g. in cyclic sense configuration or after wake-up request).

All wake-up events (except wake-up by LIN, INH or SPI from V1standby mode) generate a Reset pulse (NReset low for 2ms).

Wake-up events from V1standby by LIN, INH or SPI do not cause a Reset and the Reset generation is blocked for 2ms, i. e. a watchdog failure during this timeframe will not cause a reset.

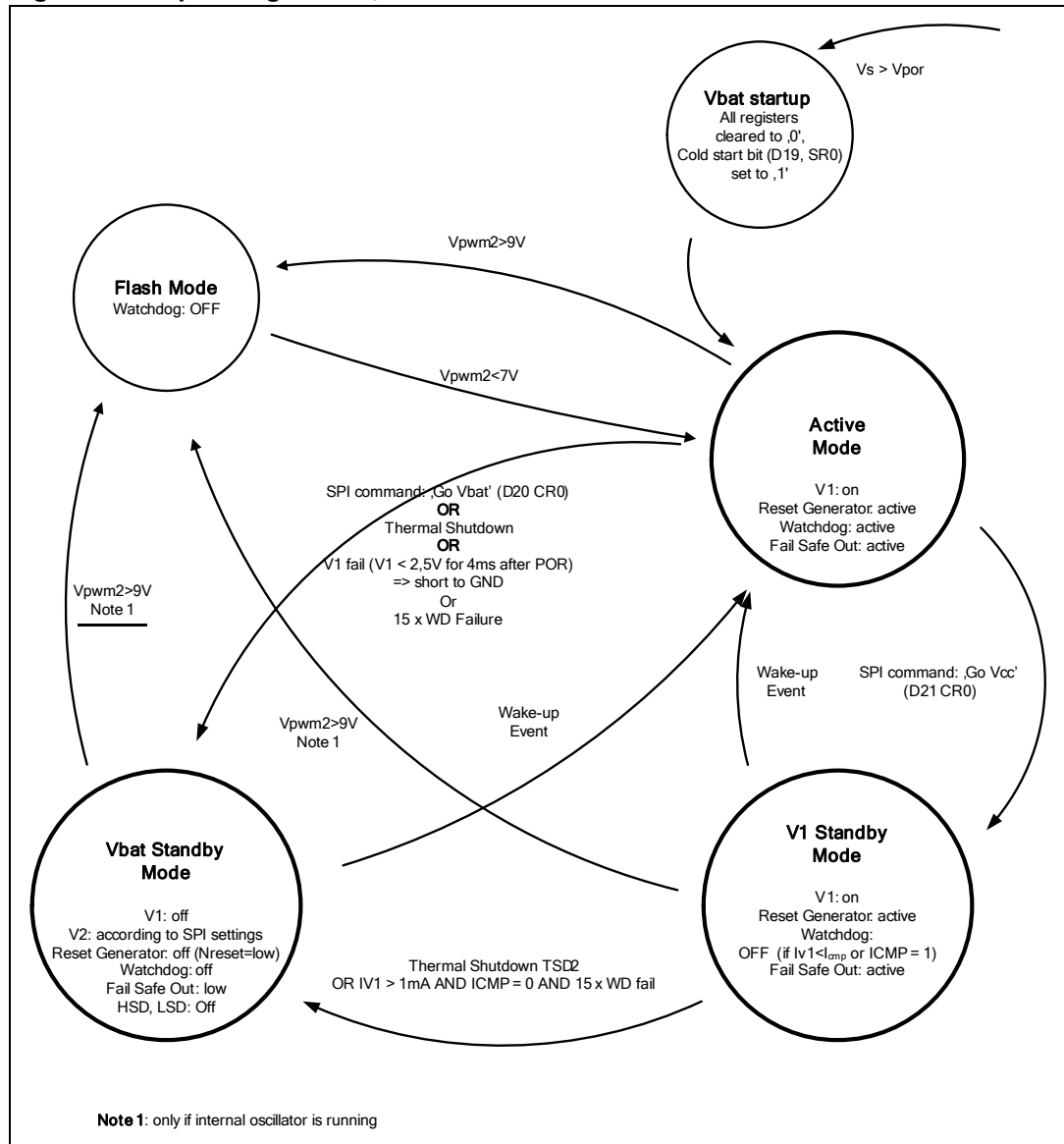
2.4 Functional overview (truth table)

Table 4. Functional overview (truth table)

| | Function | Comments | Operating modes | | |
|--------|------------------------|------------------------|-------------------------------------|--|--|
| | | | Active mode | V ₁ -standby static mode (cyclic sense) | V _{BAT} -standby static mode (cyclic sense) |
| 2.3.1 | Voltage-regulator, V1 | VOUT= 5V | On | On ⁽¹⁾ | Off |
| 2.3.2 | Voltage-regulator, V2 | VOUT= 5V | On / Off ⁽²⁾ | On ⁽²⁾ / Off | On ⁽²⁾ / Off |
| 2.3.3 | Reset-generator | | On | On | Off |
| 2.3.4 | Window watchdog | V ₁ monitor | On | Off if (I _{V1} < I _{CMP} and I _{CMP} =0) or I _{CMP} = 1 | Off |
| 2.3.5 | Wake up | | Off ⁽³⁾ | Active ⁽⁴⁾ | Active ⁽⁴⁾ |
| 2.3.6 | HS-cyclic supply | Oscillator timebase | On / Off | On ⁽²⁾ / Off | On ⁽²⁾ / Off |
| 2.3.7 | Relay driver | | On | Off | Off |
| 2.3.8 | Operational amplifiers | | On | Off | Off |
| 2.3.9 | LIN line driver | LIN 2.1 | On | Off | Off |
| 2.3.10 | LIN line receiver | | On | On | On |
| 2.3.11 | FSO | Fail-safe output | Hi – no error Lo – WD or V1 fail | Hi – no error Lo – WD or V1 fail ⁽⁵⁾ | Lo -> because V1= off |
| 2.3.12 | Oscillator | | On | ⁽⁶⁾ | ⁽⁶⁾ |
| 2.3.13 | Vs-Monitor | | On | ⁽⁷⁾ | ⁽⁷⁾ |

1. Supply the processor in low current mode
2. Only active when selected via SPI
3. Input Status can be read by SPI (Status Register 0); Inputs should be configured for static sense (Control Register 2)
4. Unless disabled by SPI
5. Watchdog is active in V1 standby mode, until I(V1) is below I_{CMP} current threshold
6. Activation = ON if cyclic sense is selected
7. Cyclic activation = pulsed ON during cyclic sense

Figure 3. Operating modes, main states



2.5 Wake up inputs

The de-bounced digital inputs WU1...WU4 can be used to wake up the L9952GXP from standby modes. These inputs are sensitive to any level transition (positive and negative edge)

For static contact monitoring, a filter time of 64 μ s is implemented at WU1-4. The filter is started when the input voltage passes the specified threshold. At $V_{in} > 1V$ and $V_{in} < (V_s - 2V)$, a Wake-up request is processed. During Wake-up request, the internal oscillator and other circuit blocks are activated in order to allow more accurate monitoring of the inputs.

In addition to the continuous sensing (static contact monitoring) at the wake up inputs, a cyclic wake up feature is implemented. This feature allows periodical activation of the wake-up inputs to read the status of the external contacts. The periodical activation can be linked to Timer 1 (0.5sec to 4.0sec in 0.5sec steps) or Timer 2 (50ms). The input signal is filtered with a filter time of 16us after a programmable delay (80us or 800us). A Wake-up will be processed if the status has changed versus the previous cycle.

The Outputs OUT_HS and OUT1-4 can be used to supply the external contacts with the timing according to the cyclic monitoring of the wake-up inputs.

If the wake-up inputs are configured for cyclic sense mode (Icxx in control register 2), the same input filter timing (Timer1 or Timer2) and the corresponding input filter delay (control register 2) must be used for the HS Outputs (Hsxx in control register 0) which supply the external contact switches.

In Standby mode, the inputs WU1-4 are SPI configurable for pull-up or pull-down current source configuration according to the setup of the external contacts (pull-up for active low contacts, pull-down for active high contacts). In active mode the inputs have a pull down resistor of 100 kOhm (typ).

In Active mode, the input status can be read by SPI (Status Register 0). Static sense should be configured (Control Register 2) before the read operation is started (In cyclic sense configuration, the input status is updated according to the cyclic sense timing; Therefore, reading the input status in this mode may not reflect the actual status).

2.6 Hall sensor ports: WU3,4, Dig_Out 3,4

Applications like Hall sensor outputs need high processing speed. The 12V signals connected to the wakeup inputs WU3 and WU4 can be looped through to the digital outputs Dig_Out 3 and Dig_Out 4 (5V) in order to avoid read out of the input state by SPI.

The setup is programmable by SPI.

The open load states of the High Side Drivers OUT1 and OUT2 can be looped through the digital outputs Dig_Out3 and Dig_Out4 without delay. In addition, the status of OUT1 and OUT2 can be accessed through the SPI interface. This feature is intended for 2-pin HALL sensors. Open Load information is only valid during ON state.

The Open Load threshold at pins OUT1...4 can be switched from $I_{OLD1} = 2mA$ to $I_{OLD2} = 8 mA$ via SPI .

2.7 Interrupt

Dig_Out4 can be configured via SPI as Interrupt output (INT) by setting Bit 20 / CR1:INT_enable='1'.

This configuration will enable the following behaviour:

- INT pin is pulled high for 2ms in case of any wake-up from V1 standby mode (WU inputs, LIN, INH, SPI, open load HS, $I_{V1} > I_{CMP_ris}$)
- Wake-up events from V1 standby do not generate a reset (i.e. NRESET is not pulled low)
- The Dig_Out4 settings in CR1 (Bits 12..14) will be ignored

2.8 Cyclic contact supply

In V1 and V_{BAT} - standby mode, any high side driver output (OUT1..4, OUTHS) can be used to periodically supply external contacts.

The timing is selectable by SPI

Timer 1: period is X sec, the on-time is 10ms resp. 20ms

With $X \in \{0.5, 1.0, 1.5, \dots 4\}$

Timer 2: period is 50ms, the on- time is 100us resp. 1ms:

Note: Cyclic sense setup: if cyclic sense feature is used for wake-up inputs (Icxx in control register 2), same input filter timing (Timer1 or Timer2) must be used for HS Outputs (Hsxx in control register 0).

2.9 Window – watchdog

During normal operation the watchdog monitors the micro controller within a nominal trigger cycle of 10ms.

In V_{BAT} -standby , V1-standby and Flash program modes, the watchdog circuit is automatically disabled. However, the watchdog will remain enabled in V1-standby mode until the current at V1 decreases below I_{CMP_fall} . The V1 current monitoring can be disabled, if the I_{CMP} bit (CR2, D20) is set to '1'.

After 'power-on', 'standby mode' or reset, the window watchdog starts with a long open window (65ms). The long open window allows the micro controller to run its own setup and then to trigger the watchdog via the SPI. The trigger is finally accepted when the CSN input becomes HIGH after the transmission of the SPI word.

A correct watchdog trigger will start the window watchdog with a closed window (< 6ms) followed by an open window (< 10ms), see timing diagrams. Subsequently, the micro controller has to serve the watchdog by alternating the watchdog trigger bit (CR0, D19). The "negative" or "positive" edge has to meet the open window time. A correct watchdog trigger signal will immediately start the next closed window.

After 8 watchdog failures in sequence, the V1 regulator is switched off for 200ms. In case of 7 further watchdog failures, the V1 regulator is completely turned off and the device goes into V_{BAT} .standby mode until a wakeup occurs. (e.g. via LIN, CAN/INH).

The watchdog is triggered by toggling the trigger bit (CR0, D19).

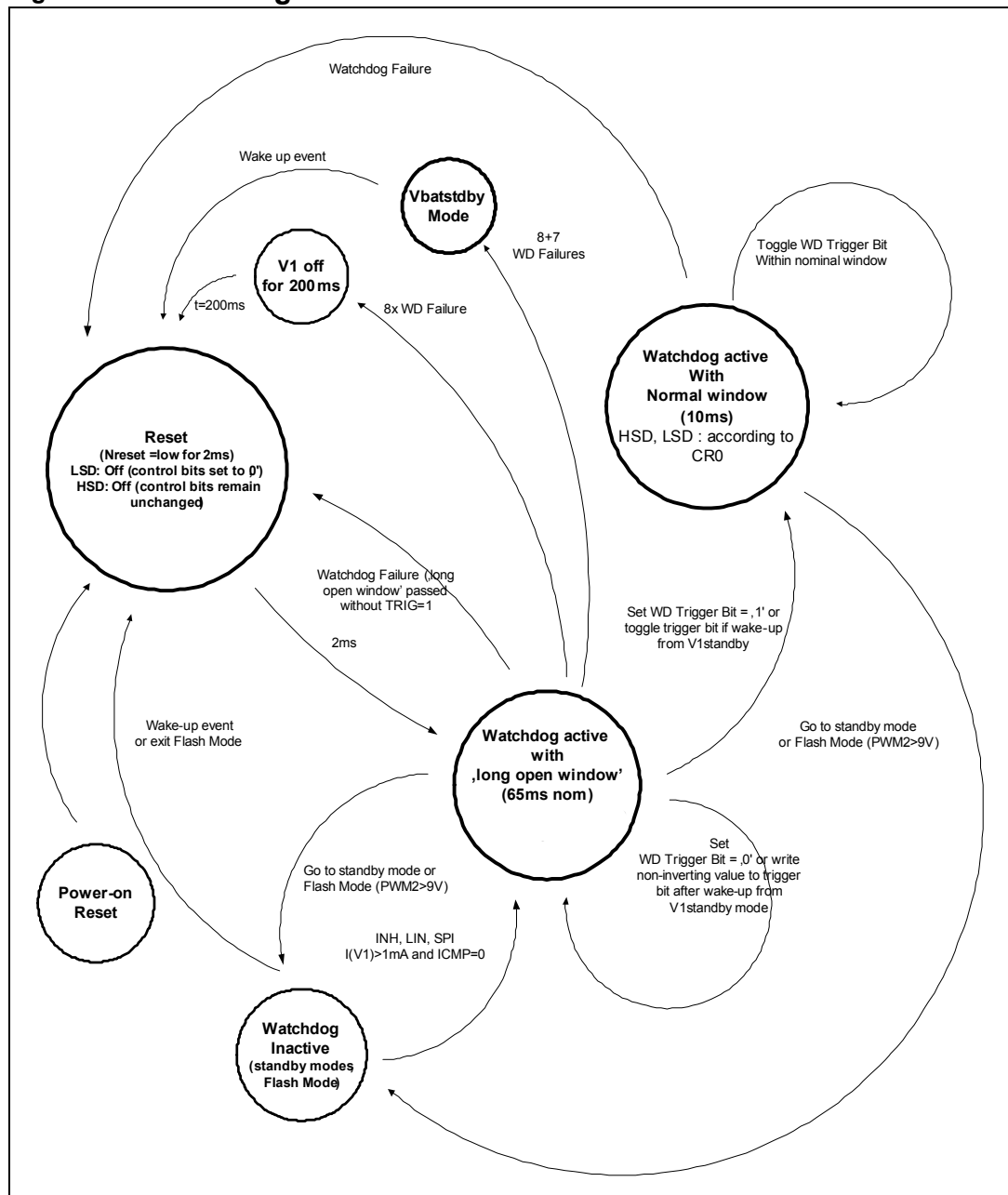
Note: The active trigger window will be reset after each correct trigger write operation.

In case of reset (NReset low for 2ms) the trigger bit is set to "0".

In case of a WD failure, the outputs (Lsx, Hsx, V2) are switched off and NReset is pulled low for 2ms.

Writing to control register 0 without inverting the WD trigger bit is possible at any time.

Figure 4. Watchdog



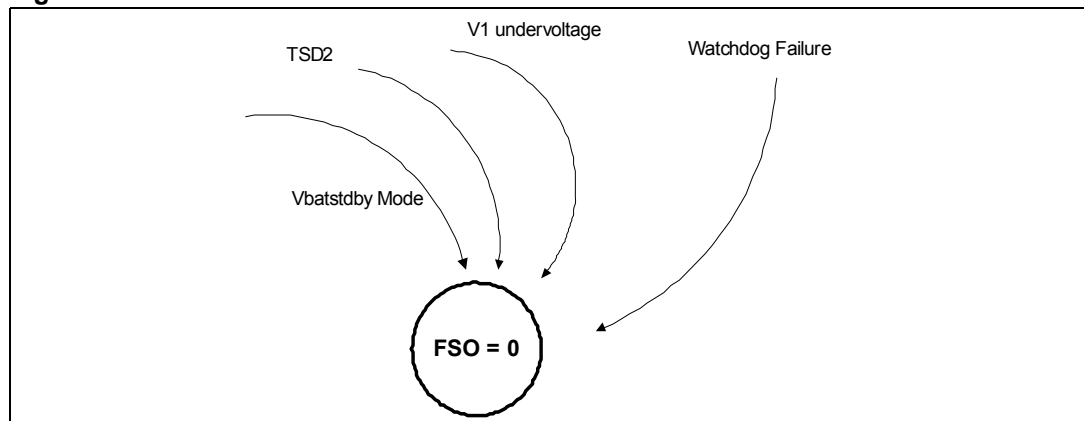
2.10 Fail safe output

After power-on ($V_s > V_{POR}$) or wakeup from V_{BAT} -standby mode, the output FSO is set to "HIGH", if V1 is above the V1 threshold. FSO is set to "LOW" in case of V1 under voltage or watchdog failure.

During V1-standby mode, FSO is HIGH unless a V1 under-voltage or watchdog reset occurs. WD remains enabled in V1 standby mode until I_{V1} drops below 150uA. In V_{BAT} -standby mode, FSO is low. At exit from V_{BAT} -standby mode, it goes to high as soon as V1 is stable.

At wakeup FSO remains high, provided that the watchdog is triggered successfully. It is set low if the watchdog is not served during the long open window of if a V1 under-voltage occurs.

Figure 5. FSO

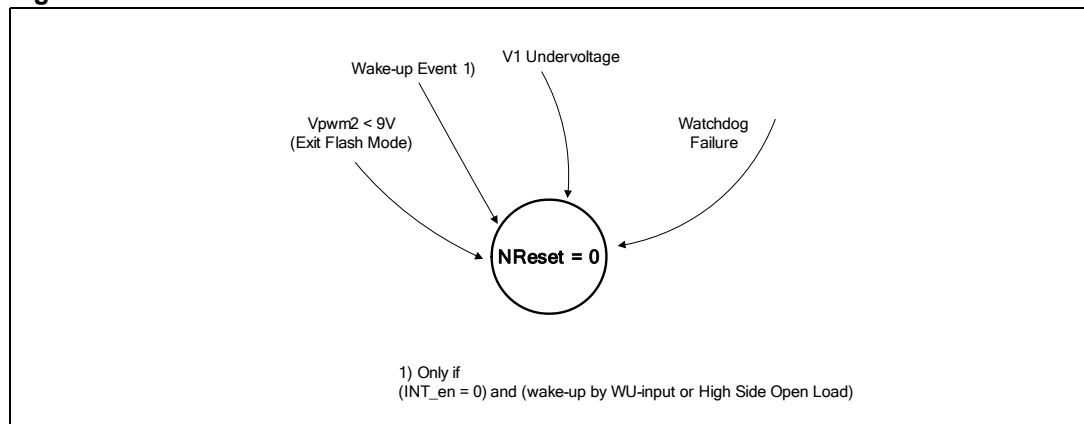


2.11 Reset – generator

IF V1 is turned on and the voltage exceeds the V1 reset threshold, the reset output "NRESET" is switched to "HIGH" after a 2ms reset delay time. This is necessary for a defined start of the micro controller when the application is switched on.

As soon as an under voltage condition of the output voltage ($V1 < VRT$) for more than 8us appears, the reset output is switched low again.

Figure 6. NReset



2.12 V1, V2 fail

The V_1 , and V_2 regulator output voltages are monitored.

In case of a drop below the V_1 , V_2 – fail thresholds ($V_{1,2} < 2V$, typ for $t > 2\mu s$), the $V_{1,2}$ - fail bits are latched. The fail bits are cleared by a dedicated SPI command.

If 4ms after turn on of the regulator the $V_{1,2}$ voltage is below the $V_{1,2}$ fail thresholds, (independent for V_1, V_2), the L9952GXP will identify a short circuit condition at the related regulator output and the regulator will be switched off.

In case of a V_1 failure the device enters V_{BAT} - standby mode automatically.

In case of a V_2 failure the SHT5V2 bit (SR0 Bit12) is set.

2.13 Low side driver outputs Rel1, Rel2

The outputs Rel1, Rel2 ($R_{DSon} = 2 \Omega$ typ. @25 °C) are specially designed to drive relay loads.

Typical relays used have the following characteristics:

Relay type 1:

- closed armature: $R = 160 \Omega \pm 10\%$, $L = 300mH$
- open armature: $R = 160 \Omega \pm 10\%$, $L = 240mH$

Relay type 2:

- closed armature: $R = 220 \Omega \pm 10\%$, $L = 420mH$
- open armature: $R = 220 \Omega \pm 10\%$, $L = 330mH$

The outputs provide an active output zener clamping (40V) feature for the demagnetisation of the relay coil, even though a load dump condition exists. In case of watchdog failure the relay drivers will be switched off and the low side driver control bits are cleared.

- Note:*
- 1 *Due to relays bouncing, high dV/dt and/or dI/dt transients may occur on the low side driver outputs. In case high currents are switched (for example window lift motor), due to parasitic capacitive inductive coupling from load side of relays to the relays coils, the Absolute Maximum Ratings of the Low Side driver outputs may be exceeded. In order to avoid this, it is recommended to place a 10nF capacitor at the Rel1, Rel2 outputs to GND.*
 - 2 *If a hard short circuit to V_{BAT} is possible at the "Low Side Driver" outputs, an RC network is required with $T_{RC} > 1\mu s$, $R \geq 1 \Omega$ (see block diagram, the value is given for an output short circuit of given $dI/dt = 5A/\mu s$).*

2.14 PWM inputs

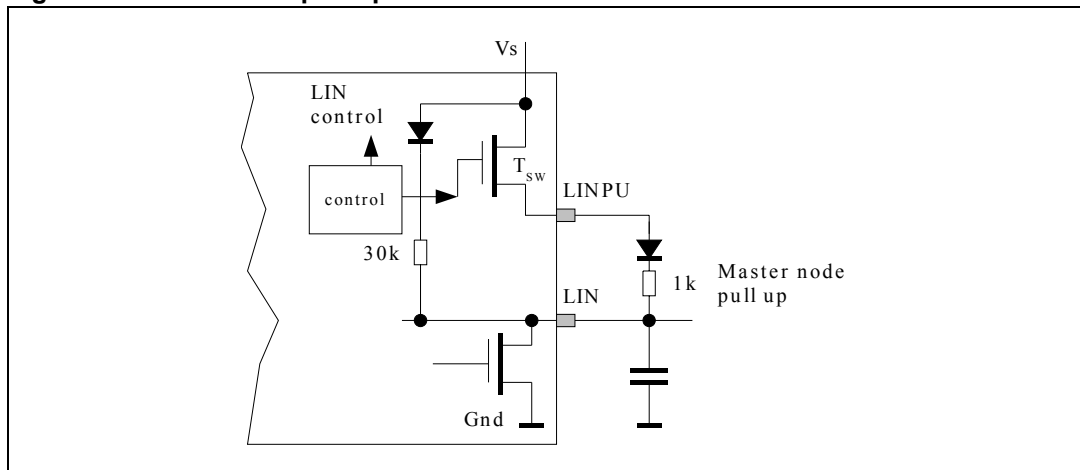
The inputs PWM 1,2 can be used to control the output drivers Out1..4 and OUT_HS with a PWM signal. Each PWM input can be mapped individually to each of the above listed outputs according to the SPI settings.

2.15 Operational amplifiers

The operational amplifiers are especially designed to be used for sensing and amplifying the voltage drop across ground connected shunt resistors. Therefore the input common mode range includes - 0.2 ... 3V.

The operational amplifiers are designed for GND + 3V... GND – 0.2V input voltage swing and rail-to-rail output voltage range. All Pins (positive, negative and outputs) are available to be able to operate in non-inverting and inverting mode. Both operational amplifiers are on-chip compensated for stability over the whole operating range within the defined load impedance.

Figure 7. Lin master pull up



A dedicated built-in switch “Tsw” enables the LIN to act as a master. (see chapter 2.18)

2.16 LIN bus interface

General requirements:

- Speed communication up to 20kbit/s
- LIN 2.0 compliant (SAEJ2602 compatible) transceiver
- Function range from +40V to -18V DC at LIN Pin
- GND disconnection fail safe at module level
- Off mode: does not disturb network
- GND shift operation at system level
- Microcontroller Interface with CMOS compatible I/O pins.
- Pull up resistor internal.
- ESD: immunity against automotive transients per ISO7637 specification (see application note)
- Matched output slopes and propagation delay

In order to further reduce the current consumption in standby mode, the integrated LIN bus interface offers an ultra low current consumption.

2.17 Error handling

The L9952GXP provides the following 3 error handling features which are not described in the LIN Spec. V2.1, but are realized in different stand alone LIN transceivers / micro controllers to switch the application back to normal operation mode.

2.17.1 Dominant TxD time out

If TXI is in dominant state (low) for more than 12ms (typ) the transmitter will be disabled until TXI becomes recessive (high). This feature can be disabled via SPI.

2.17.2 Short to battery time out

If TXI changes to dominant (low) state but RXI signal does not follow within 40 μ s, the transmitter will be disabled until TXI becomes recessive (high).

2.17.3 Short to ground mode

A wake up caused by a message on the bus will start the voltage regulator and the micro controller to switch the application back to normal operation mode.

2.18 Wake up (from LIN)

In standby mode the L9952GXP can receive a wake up from LIN bus. For the wake up feature the L9952GXP logic differentiates two different conditions.

2.18.1 Normal wake up

Normal wake up can occur when the LIN transceiver was set in standby mode while LIN was in recessive (high) state. A dominant level at LIN for at least 40 μ s, will switch the L9952GXP to active mode.

2.18.2 Wake up from short to GND condition

If the LIN transceiver was set in standby mode while LIN was in dominant (low) state, recessive level at LIN for at least 40 μ s, will switch the L9952GXP to active mode.

2.18.3 RxD pin in V1 standby

In V1 standby condition the RxD is a tristate pin.

2.19 LINPU

The LINPU (LIN pull up) signal is set by L9952GXP logic in order to drive the LIN transceiver in master mode. The master mode is realized by an internal high side switch and an external diode in series with an external 1k resistor. In master mode the high side switch is closed causing an external pull up path in parallel to the internal one (diode & 30k resistor).

HS (high side) characteristics:

- HS does not have an over current protection.
- The HS remains active in standby mode.
- Switch off only in case of over temperature (TSD2 = thermal shutdown #2).
- Typical R_{DSon} , 10 Ω .

The Linpu is activated by default (LIN master mode) and can be switched off with a SPI command (see register 2) to reduce current in case of LIN shorted to ground.

2.20 Serial Peripheral Interface (SPI)

A 24 bit SPI command (2 addresses + 22 data bits) is used for bi-directional communication with the micro controller.

During active mode, the SPI:

- 1) triggers the watchdog
- 2) controls the modes and status of all L9952GXP modules (incl. input and output drivers)
- 3) provides driver output diagnostic
- 4) provide L9952 diagnostic (incl. over temperature warning, L9952GXP operation status)

Note: During stand-by modes, the SPI is generally deactivated.

The SPI can be driven by a micro controller with its SPI peripheral running in following mode:

CPOL=0 and CPHA=0.

For this mode input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

This device is not limited to micro controller with a build-in SPI. Only three CMOS-compatible output pins and one input pin will be needed to communicate with the device. A fault condition can be detected by setting CSN to low. If CSN = 0, the DO-pin will reflect the global error flag (fault condition) of the device which is a logical -"OR" of all over current, Vs-over / under voltage, temperature warning/shutdown and V1 Fail bits. The micro controller can poll the status of the device without the need of a full SPI-communication cycle.

2.20.1 Chip Select Not (CSN)

The input pin is used to select the serial interface of this device. When CSN is high, the output pin (DO) will be in high impedance state. A low signal activates the output driver and a serial communication can be started. The state during CSN = 0 is called a communication frame.

2.20.2 Serial Data In (DI)

The input pin is used to transfer data serial into the device. The data applied to the DI will be sampled at the rising edge of the CLK signal and shifted into an internal 24 bit shift register. At the rising edge of the CSN signal the contents of the shift register will be transferred to Data Input Register. The writing to the selected Data Input Register is only enabled if exactly 24 bits are transmitted within one communication frame (i.e. CSN low). If more or less clock pulses are counted within one frame the complete frame will be ignored. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame.

Note: Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected IC's is recommended.

2.20.3 Serial Data Out (DO)

The data output driver is activated by a logical low level at the CSN input and will go from high impedance to a low or high level depending on the global error flag (fault condition). The first rising edge of the CLK input after a high to low transition of the CSN pin will transfer the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK will shift the next bit out.

2.20.4 Serial Clock (CLK)

The CLK input is used to synchronize the input and output serial bit streams. The data input (DI) is sampled at the rising edge of the CLK and the data output (DO) will change with the falling edge of the CLK signal. The SPI can be driven with a CLK frequency up to 1MHz.

2.20.5 Data registers

The device has 3 Control registers and 2 Status registers. The first two bits (D22+D23) at the DI-Input are used to select one of the Control registers. All bits are first shifted into an input shift register. After the rising edge of CSN the contents of the input shift register will be written to the selected Control register only if a frame of exact 24 bits is detected. If the Control register 1 is selected for data transfer, the Status register 1 will be transferred to the DO during the current communication frame. For the selection of Control register 0 or Control register 2, the Status register 0 is transferred to DO.

3 Protection and diagnosis

3.1 Power supply fail

Over and under-voltage detection on Vs.

3.1.1 Over voltage

If the supply voltage Vs reaches the over voltage threshold (V_{SOV})

- The outputs HS1..4, OUT_HS, Rel1,2, and LIN are switched to high impedance state (load protection)
- The over voltage bit is set and can be cleared with the clear bit (CR1,CLR)
- Automatic recovery after Vs over-voltage; selectable via SPI (CR2, bit4)

3.1.2 Under voltage

If the supply voltage Vs drops below the under voltage threshold voltage (V_{SUUV})

- The outputs HS1..4, OUTHS, Rel1,2, and LIN are switched to high impedance state (load protection)
- The under voltage bit is set
- Automatic recovery after Vs under-voltage; selectable via SPI (CR2, bit4)

3.2 Temperature warning and thermal shutdown

See state chart: " Protection and diagnosis".

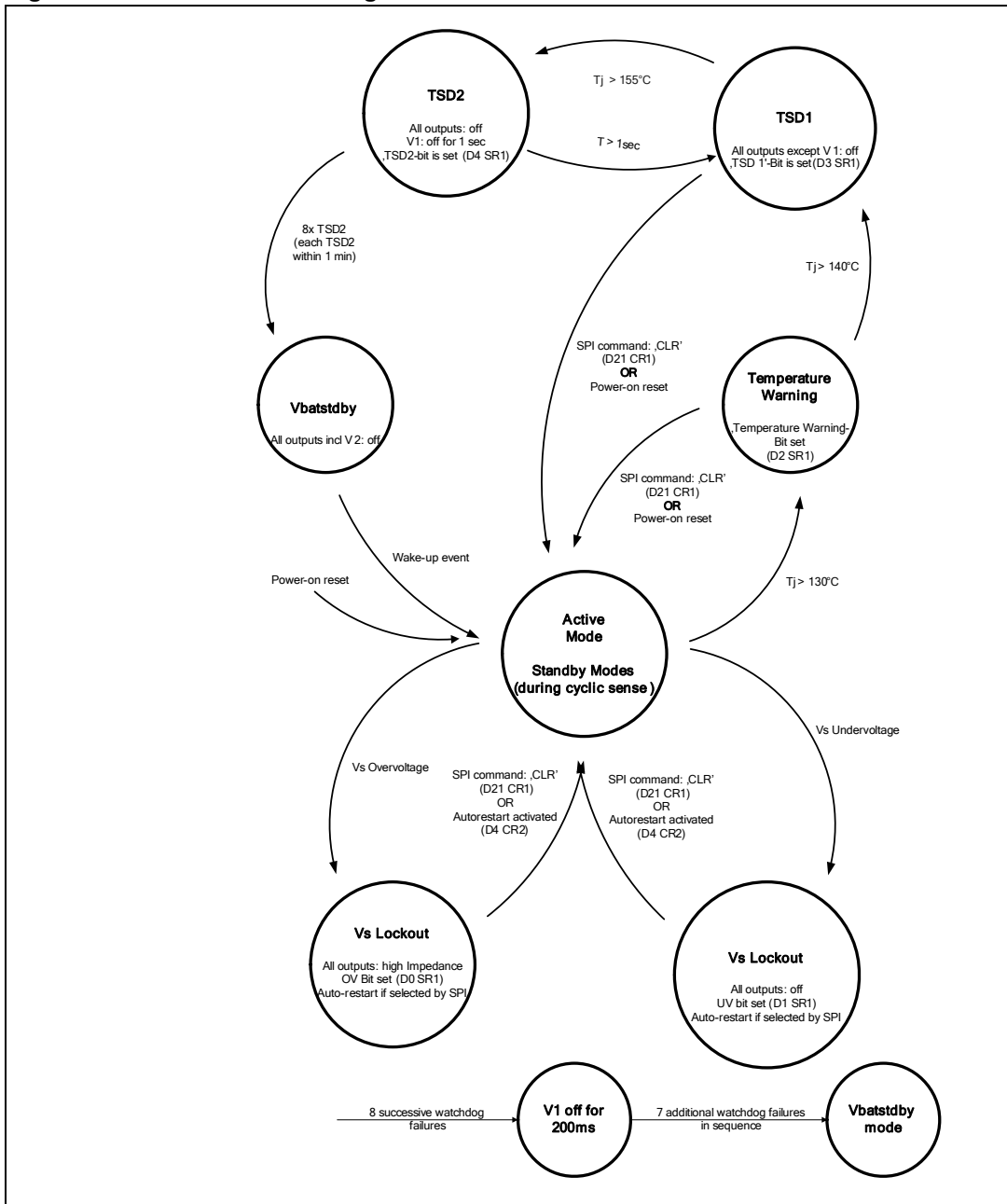
3.3 SPI diagnosis

Digital diagnosis features are provided by SPI:

- V1 reset threshold programmable
- Over temperature including pre warning
- Open load separately for each output stage
- Overload status
- Vs-supply over/under voltage
- V1 and V2 fail bit
- Status of the WU1...4, LIN and INH pin
- Cold start bit
- Number of unsuccessful V1 restarts after thermal shutdown
- Number of sequential watchdog failures
- Status of watchdog trigger bit TRIG: (SR1, Bit 16)
- LIN status (short to ground, short to V_{BAT} , dominant TxD)

See the following state chart: "Protection and diagnosis".

Figure 8. Protection and diagnosis



3.4 High side driver outputs

The component provides a total of 4 high side outputs Out1...4, ($7\ \Omega$ typ. @ 25C) to drive e.g. LED' s or hall sensors and 1 high side output OUT_HS with $1\ \Omega$ typ. @ 25 C).

The high side outputs are protected against

- Over- and under voltage
- Overload (short circuit)
- Over temperature with pre warning

If the output current exceeds the current shutdown threshold the output transistor is turned off and the corresponding diagnosis bit of the output is set.

The switches are automatically disabled in case of reset condition, Vs-under, Vs-over voltage or thermal shutdown (TSD1&2).

For OUT_HS an auto recovery feature is available in active mode.

If the OUT_HS output current exceeds the current shutdown threshold, the output transistor is turned off and the corresponding diagnosis bit of the output is set.

Via SPI command the auto recovery feature can be enabled in order to restart the driver in case of over current shutdown. This over current recovery feature is intended for loads which have an initial current higher than the over current limit of the output (e.g. Inrush current of cold light bulbs).

The device itself can not distinguish between a real overload and a non linear load like a light bulb. A real overload condition can only be qualified by time. As an example, the micro controller can switch on light bulbs by setting the over current recovery bit for the first 50ms. After clearing the recovery bit, the output will be automatically disabled if the overload condition still exists.

The status of all high side outputs (over-current, open load) can be monitored by SPI interface.

In case of a watchdog failure, the high side drivers are switched off. The control bits are not cleared, i.e. the drivers will go to the previous state once the watchdog failure condition disappears.

ESD structures are configured for nominal currents only. If external loads are connected to different grounds, the current load must be limited to this nominal current.

Note: Loss of ground or ground shift with externally grounded loads.

3.5 Low side driver outputs Rel1, Rel2

The outputs provide an active output zener clamping feature for the demagnetisation of the relay coil, even though a load dump condition exists. For safety reasons the relay drivers are linked with the Watchdog: in case of failure, or missing trigger signal the relay drivers will switch off.

4 Absolute maximum ratings

Table 5. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|--|---|---------------------|------|
| V_S | DC supply voltage / "jump start" | -0.3 to +28 | V |
| | Single pulse / $t_{max} < 400$ ms "transient load dump" | -0.3 to +40 | V |
| V_1 | Stabilized supply voltage, logic supply | -0.3 to +5.25 | V |
| V_2 | Stabilized supply voltage | -0.3 to +28 | V |
| V_{DI} , V_{CLK} V_{TXD} , V_{CSN} V_{DO} , V_{RXD} V_{NRESET} , V_{FSO} $V_{DIGOUT3,4}$ | Logic input / output voltage range | -0.3 to $V_1+0.3$ | V |
| V_{INH} V_{PWM1} , V_{PWM2} , V_{REL1} , V_{REL2} , | Wake up input voltage range PWM input voltage range Low side output voltage range | -0.3 to +40 | V |
| $V_{OUT1..4}$, V_{OUTH} | High side output voltage range | -0.3 to $V_S + 0.3$ | V |
| $V_{WU1..4}$, | Wake up input voltage range | -0.3 to $V_S + 0.3$ | V |
| V_{OP1+} , V_{OP1-} , V_{OP2+} , V_{OP2-} , | Opamp1 input voltage range Opamp2 input voltage range | -0.3 to $V_1 + 0.3$ | V |
| V_{OPOUT1} , V_{OPOUT2} | Analog Output voltage range | -0.3 to $V_S + 0.3$ | V |
| V_{LIN} , V_{LINPU} | LIN bus I/O voltage range | -20 to +40 | V |
| I_{Input} | Current injection into V_S related input pins | 5 | mA |

Note: All maximum ratings are absolute ratings. Leaving the limitation of any of these values may cause an irreversible damage of the integrated circuit !

5 ESD protection

Table 6. ESD protection

| Parameter | Value | Unit |
|-------------------------------------|---------|------|
| All pins, except LIN ⁽¹⁾ | +/- 2 | kV |
| All output pins ⁽²⁾ | +/- 4 | kV |
| LIN ⁽³⁾ | +/- 1.5 | kV |
| LIN ⁽⁴⁾ | +/- 8 | kV |
| All pins (charge device model) | +/- 500 | V |
| Corner pins (charge device model) | +/- 750 | V |
| All pins ⁽⁵⁾ | +/- 200 | V |

1. HBM (human body model, 100pF, 1.5 k Ω) according to MIL 883C, Method 3015.7 or EIA/JESD22A114-A
2. HBM with all none zapped pins grounded
3. Without external components
4. Acc. DIN EN61000-4-2 (330 Ω , 150pF), with external components:
 - Diode, type ESDLIN1524BJ
 - SMD Ferrite bead, type TDKMMZ2012Y202B
 - Capacitor C=220pF
 For detailed information please see EMC report from IBEE Zwickau (available on request)
5. Acc. Machine Model: C=220pF; L=0.75 μ H; R=10 Ω

6 Thermal data

6.1 Operating junction temperature

Table 7. Operating junction temperature

| Item | Symbol | Parameter | Value | Unit |
|-------|--------|--------------------------------------|---------------------------------|------|
| 6.1.1 | T_j | Operating junction temperature | - 40 to 150 | °C |
| 6.1.2 | RthjA | Thermal resistance junction- ambient | See Figure 10 . | °C/W |

6.2 Temperature warning and thermal shutdown

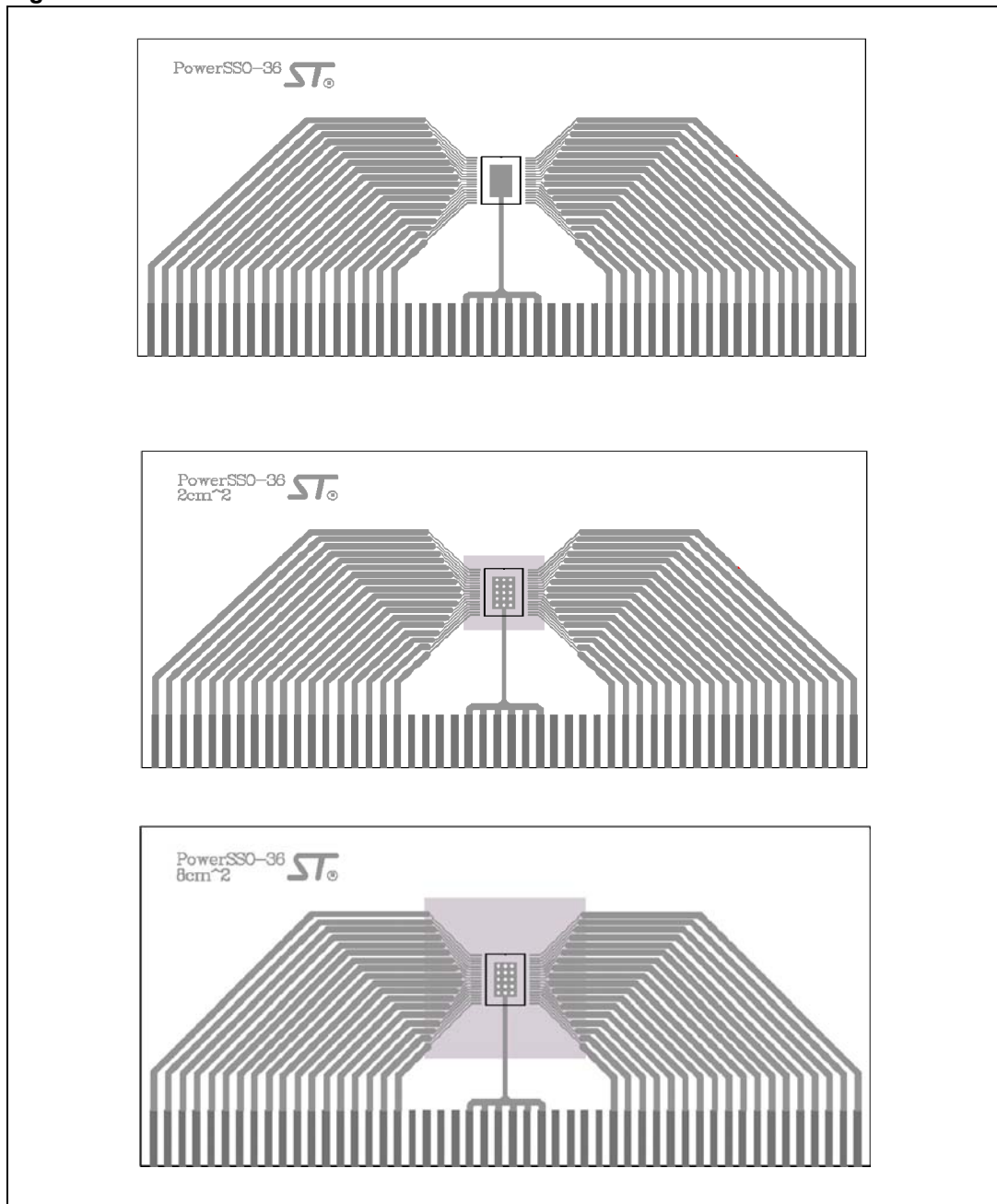
Table 8. Temperature warning and thermal shutdown

| Item | Symbol | Parameter | Min. | Typ. | Max. | Unit | | |
|-------|-----------------|--|------------|-------------|------|------|-----|----|
| 6.2.1 | $T_{W\ ON}$ | Thermal over temperature warning threshold | | $T_j^{(1)}$ | 120 | 130 | 140 | °C |
| 6.2.2 | $T_{SD1\ OFF}$ | Thermal shutdown junction temperature 1 | | $T_j^{(1)}$ | 130 | 140 | 150 | °C |
| 6.2.3 | $T_{SD2\ OFF}$ | Thermal shutdown junction temperature 2 | | $T_j^{(1)}$ | 140 | 155 | 170 | °C |
| 6.2.4 | $T_{SD2\ ON}$ | | Hysteresis | | 5 | | °C | |
| 6.2.5 | $T_{SD12\ hys}$ | | | | | | | |

1. Non-overlapping

6.3 Package and PCB thermal data

Figure 9. PowerSSO-36 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (board finish thickness 1.6 mm +/- 10% board double layer, board dimension 129x60, board Material FR4, Cu thickness 0.070mm (front and back side), thermal vias separation 1.2 mm, thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 0.025 mm).

Figure 10. PowerSSO-36 thermal resistance junction ambient Vs. PCB copper area (V1 ON)

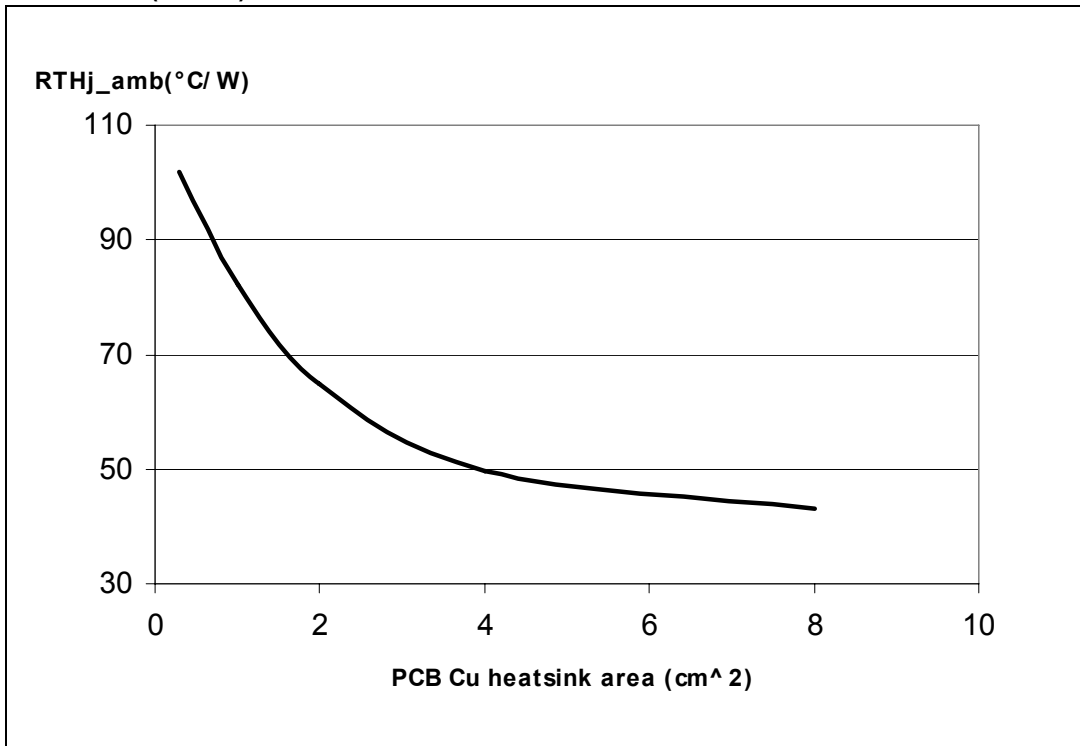
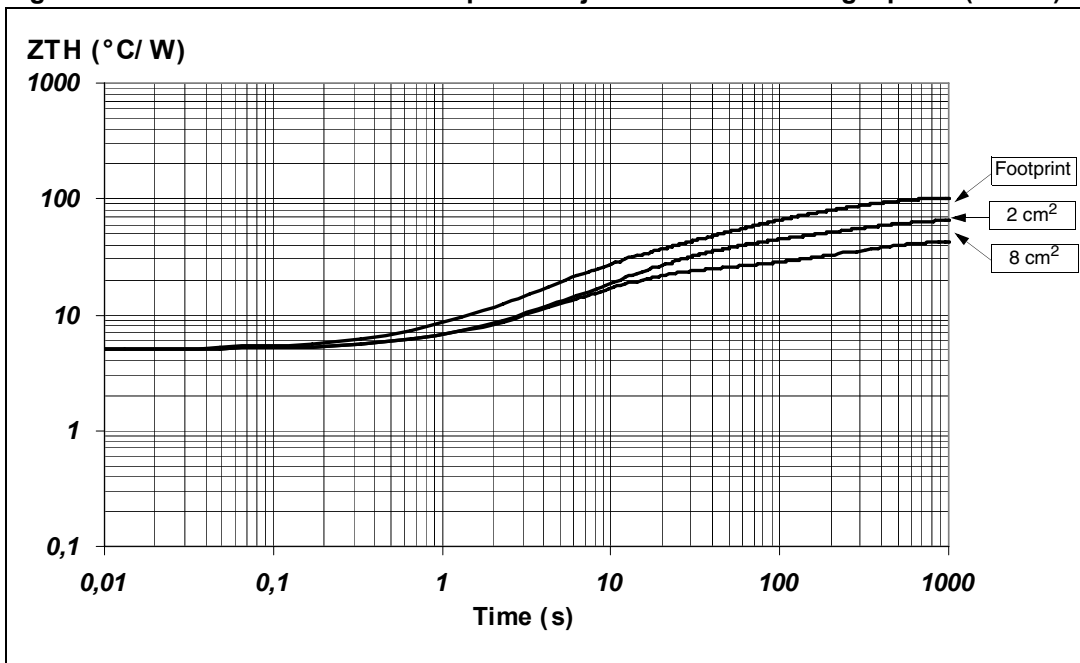


Figure 11. PowerSSO-36 thermal impedance junction ambient single pulse (V1 ON)



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 12. PowerSSO-36 thermal fitting model (V1 ON)

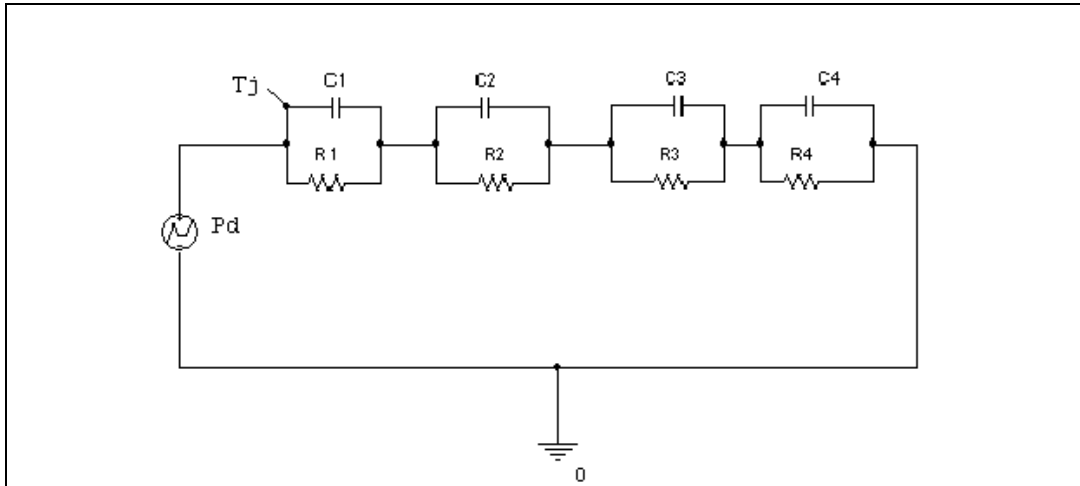


Table 9. Thermal parameters

| Area/island (cm ²) | Footprint | 2 | 8 |
|--------------------------------|-----------|-----|-----|
| R1 (°C/W) | 5 | | |
| R2 (°C/W) | 18 | 10 | 10 |
| R3 (°C/W) | 29 | 22 | 7,8 |
| R4 (°C/W) | 51 | 29 | 21 |
| C1 (W.s/°C) | 0,0003 | | |
| C2 (W.s/°C) | 0,35 | 1 | 1 |
| C3 (W.s/°C) | 1,5 | 1,3 | 1,3 |
| C4 (W.s/°C) | 5 | 15 | 15 |

7 Electrical characteristics

7.1 Supply and supply monitoring

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. $6V \leq V_S \leq 18V$; $4.8V \leq V1 \leq 5.2V$; all outputs open; $T_j = -40^\circ\text{C} \dots 130^\circ\text{C}$, unless otherwise specified.

Table 10. Supply and supply monitoring

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|--------|----------------|---|---|------|------|------|---------|
| 7.1.1 | V_S | Supply voltage range | | 6 | 13.5 | 18 | V |
| 7.1.2 | V_{SUV} | VS UV-threshold voltage | V_S increasing / decreasing | 5.11 | | 5.81 | V |
| 7.1.3 | V_{hyst_UV} | Undervoltage hysteresis | | 0.04 | 0.1 | 0.15 | V |
| 7.1.4 | V_{SOV} | VS OV-threshold voltage | V_S increasing / decreasing | 18 | | 22 | V |
| 7.1.5 | V_{hyst_OV} | Overvoltage hysteresis | Hysteresis | 0.5 | 1 | 1.5 | V |
| 7.1.6 | $I_{V(act)}$ | Current consumption in active mode | $V_S=12V$, TxD LIN high, V2 on, Outputs off $I_{V1}=I_{V2}=0A$ | | 2.7 | 20 | mA |
| 7.1.7 | $I_{V(BAT)}$ | Current consumption in V_{BAT} - standby mode | $V_S=12V$, both voltage regulators deactivated, no wake-up request | 1 | 7 | 10 | μA |
| 7.1.8 | $I_{V(BAT)CS}$ | Current consumption in V_{BAT} - standby mode | $V_S=12V$, both voltage regulators deactivated, (cyclic sense) | 40 | 75 | 100 | μA |
| 7.1.9 | $I_{V(V1)}$ | Current consumption in V_1 -standby mode | $V1=5V$, $V_S=12V$, Voltage regulator V1 active, without cyclic sense, no wake-up request | 10 | 45 | 70 | μA |
| 7.1.10 | $I_{V(BATWU)}$ | Current consumption in V_{BAT} -standby mode with a pending wake up request | $1.5V < V_{WU} < (V_S - 3V)$ | | 220 | 320 | μA |
| 7.1.11 | $I_{V(V1WU)}$ | Current consumption in V_1 - standby mode with a pending wake up request | $1.5V < V_{WU} < (V_S - 3V)$ | | 300 | 410 | μA |

7.2 Oscillator

$6V \leq V_S \leq 18V$; all outputs open; $T_j = -40^\circ\text{C} \dots 130^\circ\text{C}$, unless otherwise specified.

Table 11. Oscillator

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|-------|------------------|-----------------------|----------------------|-------|------|------|------|
| 7.2.1 | F_{CLK} | Oscillation frequency | $V_S = 6V \dots 18V$ | 0.808 | 1.01 | 1.35 | MHz |

7.3 Power-on reset (Vs)

All outputs open; $T_j = -40^\circ\text{C} \dots 130^\circ\text{C}$, unless otherwise specified.

Table 12. Power-on Reset (Vs)

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|-------|------------------------|----------------------------|----------------|------|------|------|------|
| 7.3.1 | $V_{\text{THUP_POR}}$ | V_{POR} threshold | | 2.8 | 3.45 | 4.1 | V |
| 7.3.2 | $V_{\text{Hys_POR}}$ | Hysteresis | | | 200 | | mV |

7.4 Voltage regulator V1

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. $5.25V \leq V_S \leq 27V$; $T_j = -40^\circ\text{C} \dots 130^\circ\text{C}$, unless otherwise specified.

Table 13. Voltage regulator V1

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|-------|--------|---|---|------|------|-------|------|
| 7.4.1 | V1 | Output voltage | | | 5.0 | | V |
| 7.4.2 | V1 | Output voltage tolerance Active mode | $I_{\text{LOAD}} = 1\text{mA} \dots 100\text{mA}$, $V_S = 13.5V$ | | | +/- 2 | % |
| 7.4.3 | Vhc1 | Output voltage tolerance Active mode, high current | $I_{\text{LOAD}} = 100\text{mA} \dots 250\text{mA}$, $V_S = 13.5V$ | | | +/- 3 | % |
| | | | $I_{\text{LOAD}} = 250\text{mA}$ $V_S = 13.5V$, $T_j > 80^\circ\text{C}$ | | | +/- 4 | % |
| 7.4.4 | VSTB1 | Output voltage tolerance in low current mode | $0\text{mA} \leq I_{\text{LOAD}} \leq I_{\text{CMP}}$ $V_S = 13.5V$ | | | +/- 4 | % |
| 7.4.5 | VDP1 | Drop-out voltage in undervoltage conditions | $I_{\text{LOAD}} = 50\text{mA}$, $V_S = 4.5V$ | | 0.2 | 0.4 | V |
| | | | $I_{\text{LOAD}} = 100\text{mA}$, $V_S = 4.5V$ | | 0.3 | 0.5 | V |
| 7.4.6 | ICC1 | Output current in active mode | Max. continuous load current | | | 250 | mA |

Table 13. Voltage regulator V1 (continued)

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|--------|----------|---|--|--------------|--------------|------|------|
| 7.4.7 | ICCmax1 | Short circuit output current | Current limitation | 400 | 600 | 950 | mA |
| 7.4.8 | Cload1 | Load capacitor1 | Ceramic ⁽¹⁾ | 0.22 | | | µF |
| 7.4.9 | tTSD | V1 deactivation time after thermal shutdown | | | 1 | | s |
| 7.4.10 | ICMP_ris | Current comp. rising threshold | Rising current | 0.9 | 2.5 | 4 | mA |
| 7.4.11 | ICMP_fal | Current comp. falling threshold | Falling current Tj= -40°C...130°C Tj= 25°C...130°C | 0.75 0.85 | 1.95 1.95 | | mA |
| 7.4.12 | ICMP_hys | Current comp. hysteresis | | | 0.5 | | mA |
| 7.4.13 | V1fail | V1 fail threshold | V1 forced | | 2 | | V |

1. Placement close to the PAD

7.5 Voltage regulator V2

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. $5.25V \leq V_S \leq 27V$; $T_j = -40^\circ C \dots 130^\circ C$, unless otherwise specified.

Table 14. Voltage regulator V2

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|-------|--------------------|--|--|------|------------|------------|--------|
| 7.5.1 | V ₂ | Output voltage | | | 5.0 | | V |
| 7.5.2 | V ₂ | Output voltage tolerance Active mode | I _{LOAD} = 1mA ... 50mA, V _S = 13.5V | | | +/- 3 | % |
| 7.5.3 | V _{hc1} | Output voltage tolerance Active mode, high current | I _{LOAD} = 50mA ... 100mA, V _S = 13,5V | | | +/- 4 | % |
| 7.5.4 | V _{STB2} | Output voltage tolerance in low current mode | I _{LOAD} = 0uA ... 1mA V _S = 13,5V | | | +/- 5 | % |
| 7.5.5 | V _{DP2} | Drop-out voltage | I _{LOAD} = 25mA, V _S = 5 V I _{LOAD} = 50mA, V _S = 5 V | | 0,3 0.4 | 0,4 0.7 | V V |
| 7.5.6 | ICC2 | Output current in Active mode | Max. continuous load current | | | 100 | mA |
| 7.5.7 | ICCmax2 | Short circuit output current | Current limitation | 200 | 300 | 500 | mA |
| 7.5.8 | C _{load} | Load capacitor | Ceramic ⁽¹⁾ | 0.22 | | | µF |
| 7.5.9 | V2 _{fail} | V2 fail threshold | V2 forced | | | 2 | V |

1. Placement close to the PAD

7.6 Reset generator (V1 supervision)

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin. $5.25V < V_S = 18V$; $T_j = -40$ to 130 °C, unless otherwise specified.

Table 15. Reset generator

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|-------|-------------|------------------------------|----------------------------------|------|------|------|------------|
| 7.6.1 | V_{RT1} | Reset threshold voltage1 | V_S, V_{V1} inc. / decreasing | 4.5 | 4.63 | 4.75 | V |
| 7.6.2 | V_{RT2} | Reset threshold voltage2 | V_S, V_{V1} inc. / decreasing | 4.25 | 4.37 | 4.5 | V |
| 7.6.3 | V_{RESET} | Reset pin low output voltage | $V1 > 1V$, $I_{RESET} = 1mA$ | | 0,2 | 0,4 | V |
| 7.6.4 | R_{RESET} | Reset pull up int. resistor | | 60 | 110 | 204 | k Ω |
| 7.6.5 | t_{RR} | Reset reaction time | @Iload = 1mA | 6 | | 40 | μs |
| 7.6.6 | | V1 under-voltage filter time | | | 16 | | μs |

7.7 Watchdog

$6V < V_S < 18V$; $4.8V < V1 < 5.2V$; $T_j = -40$ to 130 °C, unless otherwise specified

Table 16. Watchdog ⁽¹⁾

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|-------|-----------|---------------------------|----------------|-------|------|-------|------|
| 7.7.1 | t_{LW} | Long open window | | 48,75 | 65 | 81,25 | ms |
| 7.7.2 | t_{CW} | Closed window | | 4.5 | 6 | 7.5 | ms |
| 7.7.3 | t_{OW} | Open window | | 7.5 | 10 | 12.5 | ms |
| 7.7.4 | t_{WDR} | Watchdog reset pulse time | | 1.5 | 2 | 2.5 | ms |

1. See [Figure 13](#).

Figure 13. Watchdog timing

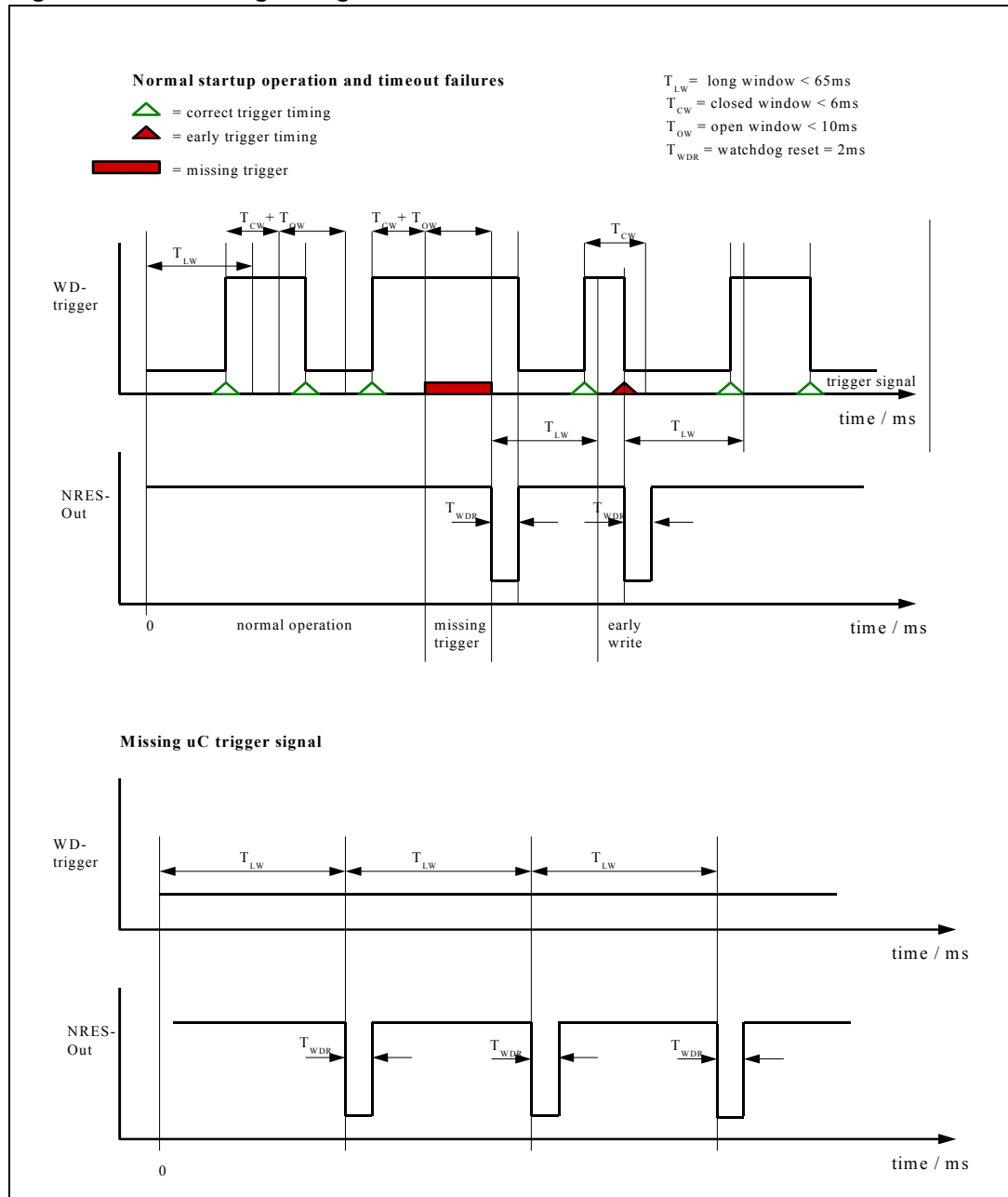
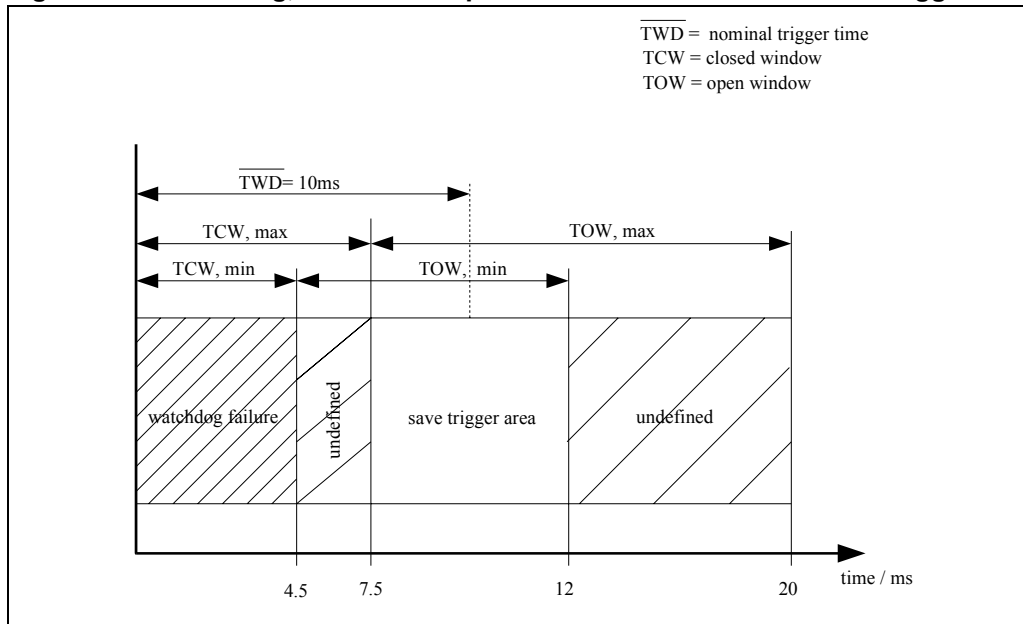


Figure 14. Watchdog, closed and open window tolerances and save trigger area



7.8 High side outputs

7.8.1 Output (Out_HS)

The voltages are referred to gnd and currents are assumed positive, when the current flows into the pin. $6\text{V} \leq V_S \leq 18\text{V}$; $4.8\text{V} \leq V_1 \leq 5.2\text{V}$; $T_j = -40^\circ\text{C} \dots 130^\circ\text{C}$, unless otherwise specified.

Table 17. High side outputs (Out_HS)

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|-------|------------------------------------|---|---------------------------|------|--------------------------|------|------------------------|
| 7.8.1 | $R_{\text{DSON}}^{\text{OUT_HS}}$ | Static Drain Source On-resistance to supply (IOUT_HS=150mA) | $T_j = 25^\circ\text{C}$ | 0 | 1.0 | 1.5 | Ω |
| | | | $T_j = 125^\circ\text{C}$ | 0 | 1.6 | 3 | Ω |
| 7.8.2 | t_{dONHS} | Switch on delay time | 0.2 VS | 10 | 35 | 60 | μs |
| 7.8.3 | t_{dOFFHS} | Switch off delay time | 0.8VS | 40 | 95 | 150 | μs |
| 7.8.4 | t_{dSDHS} | Short circuit filter time | Tested by scan chain | | 64* T_{OSC} | | |
| 7.8.5 | t_{dARHS} | Auto recovery filter time | Tested by scan chain | | 400* T_{OSC} | | |
| 7.8.6 | dV_{out}/dt | Slew rate | | 0.2 | 0.5 | 0.8 | $\text{V}/\mu\text{s}$ |
| 7.8.7 | I_{OSDHS} | Short circuit shutdown current | | 480 | 900 | 1320 | mA |
| 7.8.8 | I_{OLD} | Open load detection current | | 40 | 80 | 120 | mA |

7.8.2 Outputs (OUT1...4)

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin. $6V \leq V_S \leq 18V$; $4.8V \leq V_1 \leq 5.2V$; $T_j = -40^\circ\text{C} \dots 130^\circ\text{C}$, unless otherwise specified.

Table 18. High side outputs (OUT 1..4)

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|--------|-----------------------|-------------------------------------|---|------|-------------------------|------|------------------|
| 7.8.11 | R_{DSON} | On – resistance | $I_{\text{LOAD}} = 60\text{mA} @ T_j = +25^\circ\text{C}$ | 0 | 7 | 12 | Ω |
| 7.8.12 | I_{OUT} | Short circuit shutdown current | $8V < V_S < 16V$ | 140 | 235 | 330 | mA |
| 7.8.13 | I_{OLD1} | Open load detection current 1 | Selectable via SPI | 0.8 | 2 | 4 | mA |
| 7.8.14 | I_{OLD2} | Open load detection current 2 | | 6 | 8 | 13 | mA |
| 7.8.15 | SR | Slew rate | | 0.2 | 0.5 | 0.8 | V/ μs |
| 7.8.16 | t_{dONHS} | Switch ON delay time | $0.2 V_S$ | 10 | 35 | 60 | μs |
| 7.8.17 | t_{dOFFHS} | Switch OFF delay time | $0.8 V_S$ | 40 | 95 | 150 | μs |
| 7.8.18 | t_{SCF} | Short circuit filter time | Tested by scan chain | | 64* T_{OSC} | | |
| 7.8.19 | $I_{\text{FW}}^{(1)}$ | Loss of GND current (ESD structure) | | 100 | | | mA |

1. Parameter guaranteed by design

7.9 Relay drivers

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin. $6V \leq V_S \leq 18V$; $4.8V \leq V_1 \leq 5.2V$; $T_j = -40$ to 130°C , unless otherwise specified.

Table 19. Relay drivers

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|-------|--------------------|---|--|------|------|------|---------------|
| 7.9.1 | R_{DSON} | DC output resistance | $I_{\text{LOAD}} = 100\text{mA} @ T_j = +25^\circ\text{C}$ | 0 | 2 | 3 | Ω |
| 7.9.2 | I_{OUT} | Short circuit shutdown current | $8V < V_S < 16V$ | 250 | 375 | 500 | mA |
| 7.9.3 | V_Z | Output clamp voltage ⁽¹⁾ | $I_{\text{LOAD}} = 100\text{mA}$ | 40 | | 48 | V |
| 7.9.4 | t_{ONHL} | Turn on delay time to 10% V_{OUT} | | 5 | 50 | 100 | μs |
| 7.9.5 | t_{OFFLH} | Turn off delay time to 90% V_{OUT} | | 5 | 50 | 100 | μs |

Table 19. Relay drivers (continued)

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|-------|-----------|---------------------------|----------------------|------|------------------|------|------------|
| 7.9.6 | t_{SCF} | Short circuit filter time | Tested by scan chain | | 64* T_{OSC} | | |
| 7.9.7 | SR | Slew Rate | | 0.2 | 2 | 4 | V/ μ s |

1. The output is capable to switch off relay coils with the impedance of $R_L=160\Omega$; $L = 300mH$ ($R_L=220\Omega$; $L= 420mH$); at $V_S = 40V$ (Load dump condition)

7.10 Wake up inputs (WU1..WU4)

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin. $6V \leq V_S \leq 18V$; $T_j = -40$ to $130\text{ }^\circ\text{C}$, unless otherwise specified.

Table 20. Wake up inputs⁽¹⁾(WU1..WU4)

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|--------|-----------------|---|---|-----------------------------------|-------------|-------------|------------|
| 7.10.1 | V_{WUthp} | Wake-up negative edge threshold voltage | | 0.4 Vs | 0.45 Vs | 0.5 Vs | V |
| 7.10.2 | V_{WUthn} | Wake-up positive edge threshold voltage | | 0.5 Vs | 0.55 Vs | 0.6 Vs | V |
| 7.10.3 | V_{HYST} | Hysteresis | | 0.05 Vs | 0.1 Vs | 0.15 Vs | V |
| 7.10.4 | t_{WU} | Minimum time for wake-up | | 51 | 64 | 77 | μ s |
| 7.10.5 | I_{WU_stbby} | Input current in standby mode | $1.5V < V_{IN} < (V_S - 3V)$ | 10 | 20 | 30 | μ A |
| 7.10.6 | R_{WU_act} | Input resistor to GND in active mode and in standby mode during wake-up request | | 100 | 275 | 450 | k Ω |
| 7.10.7 | Nn | Number of samples | During OUT_HS on, cyclic sense mode (100us cyclic HS on time) | 2 (at 80 μ s and 100 μ s) | | | |
| 7.10.8 | V_{wuthl} | Pending wake up request low threshold | | 1.0 | 1.25 | 1.5 | V |
| 7.10.9 | V_{wuthh} | Pending wake up request high threshold | | $V_S - 3$ | $V_S - 2.2$ | $V_S - 1.4$ | V |

1. Defines whether the inputs W1..4 are configured with current source or current sink in standby mode.

7.11 Wake up input (INH)

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin. $6V \leq V_S \leq 18V$; $T_j = -40$ to 130 °C, unless otherwise specified.

Table 21. Wake up input (INH)

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|--------|--------------|------------------------------------|---|------------------------------------|------|------|---------|
| 7.11.1 | I_{INHth} | Wake-up activate threshold current | | 30 | 75 | 120 | μA |
| 7.11.2 | I_{INHUth} | Wake-up passive threshold current | | 30 | 70 | 120 | μA |
| 7.11.3 | I_{INHhys} | Wake-up current hysteresis | | | 10 | 20 | μA |
| 7.11.4 | t_{WU} | Minimum time for wake-up | | 51 | 64 | 77 | μs |
| 7.11.5 | Nn | Number of samples | During OUT_HS on, cyclic sense mode (100 μs cyclic HS on time) | 2 (at 80 μs and 100 μs) | | | |

7.12 LIN

Compatible to Lin 2.1 for Baud rates up to 20 kBit/s

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

$6V \leq V_S \leq 18V$; $4.8V \leq V1 \leq 5.2V$; $T_j = -40$ °C... 130 °C, unless otherwise specified.

Table 22. LIN receiver

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|--------|---------------|-------------------------------|---|------|------|------|---------|
| | | LIN receiver | | | | | |
| 7.12.1 | V_{TXDLOW} | Input voltage dominant level | Normal mode, V1=5V | 1 | 1.3 | | V |
| 7.12.2 | $V_{TXDHIGH}$ | Input voltage recessive level | Normal mode, V1=5V | | 2.2 | 2.5 | V |
| 7.12.3 | V_{TXDHYS} | $V_{TXDHIGH} - V_{TXDLOW}$ | Normal mode, V1=5V | 0.5 | 0.8 | | V |
| 7.12.4 | I_{TXDPU} | TXD pull up current | Normal and V1-standby mode , V1=5V | -5 | -30 | -60 | μA |
| 7.12.5 | I_{TXDPD} | TXD pull-down current | V_{BAT} - standby mode, $V_{TXDHIGH}$ V1=5V | 5 | 30 | 60 | μA |
| 7.12.6 | V_{RXDLOW} | Output voltage dominant level | Normal mode, V1=5V, 2mA | | 0.2 | 1.5 | V |

Table 22. LIN receiver (continued)

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---------|-----------------------|--|--|-------------------------|------------------------|-------------------------|------|
| LIN | | LIN receiver | | | | | |
| 7.12.7 | V _{RXDHIGH} | Output voltage recessive level | Normal mode, V ₁ =5V, 2mA | 4.5 | | | V |
| 7.12.8 | V _{THdom} | Receiver threshold voltage recessive to dominant state | | 0.4 V _S | 0.45 V _S | 0.5 V _S | V |
| 7.12.9 | V _{THrec} | Receiver threshold voltage dominant to recessive state | | 0.5 V _S | 0.55 V _S | 0.6 V _S | V |
| 7.12.10 | V _{THhys} | Receiver threshold hysteresis | V _{THrec} - V _{THdom} | 0.07 V _S | 0.1 V _S | 0.175 V _S | V |
| 7.12.11 | V _{THcnt} | Receiver tolerance center value | (V _{THrec} + V _{THdom}) / 2 | 0.475 V _S | 0.5 V _S | 0.525 V _S | V |
| 7.12.12 | V _{THwkup} | Receiver wakeup threshold voltage | | 1.0 | 1.5 | 2 | V |
| 7.12.13 | V _{THwkdown} | Receiver wakeup threshold voltage | | 3.5 V _S | 2.5 V _S | 1.5 V _S | V |
| 7.12.14 | T _{bus} | Dominant time for wakeup via bus | Sleep mode edge: rez.- dom. | | 64 | | μs |

Table 23. LIN DC parameters

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---------|---------------------------|--|---|------|------|------|------|
| LIN | | DC parameters | | | | | |
| 7.12.15 | I _{LINDomSC} | Transmitter input current limit in dominant state | V _{TxD} = V _{TxDlow} V _{LIN} = V _{batmax} = 18V | 40 | 100 | 180 | mA |
| 7.12.16 | I _{bus_PAS_dom} | Input leakage current at the receiver incl. Pull-Up resistor | V _{TxD} = V _{TxDhigh} V _{LIN} = 0V, V _{BAT} = 12V, Slave mode | -1 | | | mA |
| 7.12.17 | I _{bus_PAS_drec} | Transmitter input current in recessive state | V _{TxD} = V _{TxDhigh} 8V < V _{LIN} , V _{BAT} < 18V; V _{LIN} ≥ V _{BAT} | | | 20 | μA |
| 7.12.18 | I _{bus_NO_GND} | Input current if loss of GND at Device | GND = V _S , 0V < V _{LIN} < 18V V _{BAT} = 12V | -1 | | 1 | mA |
| 7.12.19 | I _{bus} | Input current if loss of Vbat at device | GND = V _S , 0V < V _{LIN} < 18V | | | 100 | μA |

Table 24. LIN transmitter (continued)

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---------|--------------|--------------------------------------|--|-----------|------|------|------------|
| | | LIN transmitter | | | | | |
| 7.12.20 | V_{LINdom} | LIN voltage level in dominant state | $V_{TXD} = V_{TXDlow}$ $I_{LIN} = 40mA$ | | | 1.2 | V |
| 7.12.21 | V_{LINrec} | LIN voltage level in recessive state | $V_{TXD} = V_{TXDhigh}$ $I_{LIN} = 10\mu A$ | 0.8 Vs | | | V |
| 7.12.22 | R_{LINup} | LIN output pull up resistor | $V_{LIN} = 0V$ | 20 | 40 | 60 | k Ω |

Table 25. LIN timing

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---------|-----------------|--|--|------|------|------|---------|
| | | LIN timing | | | | | |
| 7.12.24 | t_{TXpd_sym} | Symmetry of transmitter propagation delay time (rising vs. falling edge) | $t_{TXpd_sym} = t_{TXpdr} - t_{TXpdf}$ $V_s = 12V,$ $R_{bus} C_{bus}: 1 k\Omega, 1 nF$ | -2.5 | - | 2.5 | μs |
| 7.12.25 | t_{RXpd} | Receiver propagation delay time | $t_{RXpd} = \max(t_{RXpdr} t_{RXpdf})$ $t_{RXpdf} = t(0.5RXD) - t(0.45 V_{Lin})$ $t_{RXpdr} = t(0.5RXD) - t(0.55 V_{Lin})$ $C_{rx} = 20pF$ $V_s = 12V,$ $R_{bus} C_{bus}: 1 k\Omega, 1 nF; 660 \Omega, 6.8 nF; 500 \Omega, 10 nF$ | | - | 6 | μs |
| 7.12.26 | t_{RXpd_sym} | Symmetry of receiver propagation delay time (rising vs. falling edge) | $t_{RXpd_sym} = t_{RXpdr} - t_{RXpdf}$ | -2 | - | 2 | μs |

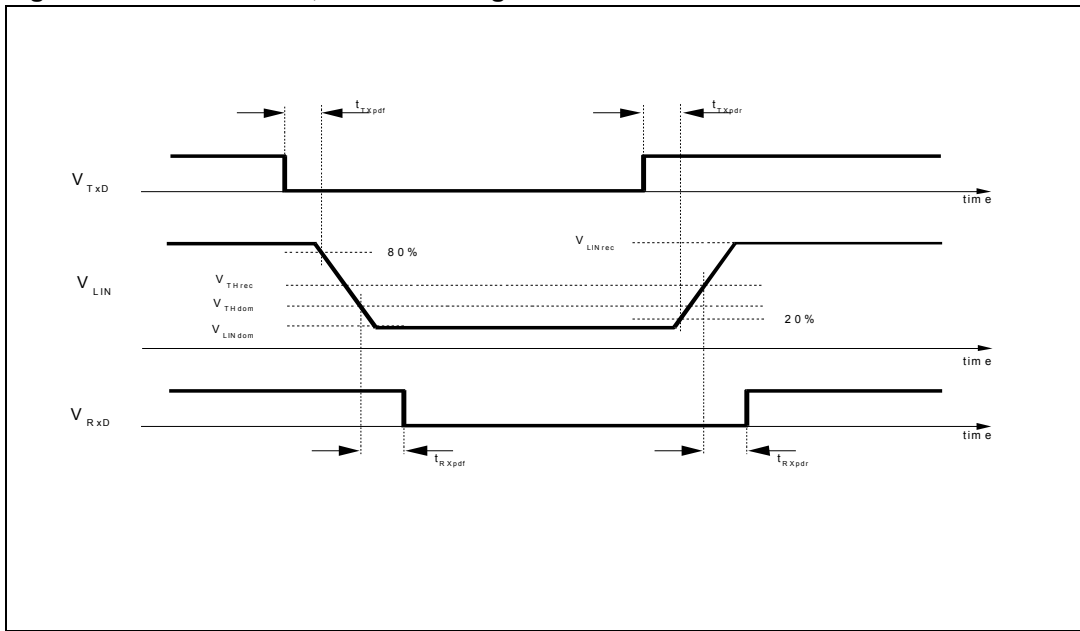
Table 25. LIN timing (continued)

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---------|--------|--------------|---|-------|------|-------|------|
| | | LIN timing | | | | | |
| 7.12.27 | D1 | Duty cycle 1 | THRec(max)=0.744*Vs THDom(max)=0.581*Vs Vs= 7...18V, tbit= 50us, D1=tbus_rec(min)/(2xtbit) Rbus, Cbus: 1 kΩ, 1 nF; 660 Ω, 6.8 nF; 500 Ω, 10 nF | 0.396 | - | | |
| 7.12.28 | D2 | Duty cycle 2 | THRec(min)=0.284*Vs; THDom(min)=0.422*Vs, Vs= 7.6 ...18V, tbit= 50μs, D1=tbus_rec(max)/(2xtbit) Rbus, Cbus: 1 kΩ, 1 nF; 660 Ω, 6.8 nF; 500 Ω, 10 nF | | - | 0.581 | |
| 7.12.29 | D3 | Duty cycle 3 | THRec(max)=0.778*Vs; THDom(max)=0.616*V, Vs= 7...18V tbit= 96μs, D3=tbus_rec(min)/(2xtbit) Rbus, Cbus: 1 kΩ, 1 nF; 660 Ω, 6.8 nF; 500 Ω, 10 nF | 0.417 | - | | |
| 7.12.30 | D4 | Duty cycle 4 | THRec(min)=0.251*Vs; THDom(min)=0.389*Vs, Vs= 7.6 ...18V, tbit= 96μs D1=tbus_rec(max)/(2xtbit) Rbus, Cbus: 1 kΩ, 1 nF; 660 Ω, 6.8 nF; 500 Ω,10 nF | | - | 0.59 | |

Table 26. LIN DC values

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---------|-------------------|-----------------|----------------|------|------|------|------|
| | | DC values | | | | | |
| 7.12.31 | R _{DSon} | ON resistance | | | 10.5 | 16 | Ω |
| 7.12.32 | I _{leak} | Leakage current | | | | 1 | μA |

Figure 15. LIN transmit, receive timing



7.13 Operational amplifier

The voltages are referred to gnd and currents are assumed positive, when the current flows into the pin. $6V \leq V_S \leq 18V$; $T_j = -40...130^\circ\text{C}$, unless otherwise specified.

Table 27. Operational amplifier

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---------|--------------------|-----------------------------|-------------------------------|-----------------------|------|----------------|------|
| 7.13.1 | GBW | GBW product | | 1 | 3.5 | 7.0 | MHz |
| 7.13.2 | AVOL _{DC} | DC open loop gain | | 80 | | | dB |
| 7.13.3 | PSRR | Power supply rejection | DC, Vin =150 mV | 80 | | | dB |
| 7.13.4 | V _{off} | Input offset voltage | | -5 | | +5 | mV |
| 7.13.5 | V _{ICR} | Common mode input range | | -0.2 | 0 | 3 | V |
| 7.13.6 | V _{OH} | Output voltage range high | Iload = 1mA to Gnd | 0.2 V _S | | V _S | V |
| 7.13.7 | V _{OL} | Output voltage range low | Iload = 1mA to V _S | 0 | | 0.2 | V |
| 7.13.8 | I _{lim+} | Output current limitation + | DC | 5 | 10 | 20 | mA |
| 7.13.9 | I _{lim-} | Output current limitation - | DC | -5 | -10 | -20 | mA |
| 7.13.10 | SR+ | Slew rate positive | | 1 | 4 | 10 | V/μs |
| 7.13.11 | SR- | Slew rate negative | | -1 | -4 | -10 | V/μs |

Note: The operational amplifier is on-chip stabilized for external capacitive loads $C_L \leq 25\text{pF}$ (all operating conditions)

7.14 SPI

7.14.1 Input: CSN

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. $6V \leq V_S \leq 18V$; $4.5V \leq V1 \leq 5.3V$; all outputs open; $T_j = -40^\circ\text{C} \dots 130^\circ\text{C}$, unless otherwise specified.

Table 28. SPI (Input CSN)

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|--------|----------------------|--|--|------|------|------|---------------|
| 7.14.1 | V_{CSNLOW} | Input voltage low level | Active mode, $V1 = 5V$ | 0.5 | 1.0 | 1.6 | V |
| 7.14.2 | V_{CSNHIGH} | Input voltage high level | Active mode, $V1=5V$ | 1 | 1.75 | 2.5 | V |
| 7.14.3 | V_{CSNHYS} | $V_{\text{CSNHIGH}} - V_{\text{CSNLOW}}$ | Active mode, $V1=5V$ | 0.5 | 1.0 | 1.5 | V |
| 7.14.4 | I_{CSNPU} | CSN pull up current | Active mode and V1 Standby mode, $V1=5V$ | -5 | -30 | -60 | μA |
| 7.14.5 | I_{CSNPD} | CSN pull-down current | In V_{bat} standby mode | 5 | 30 | 60 | μA |

7.14.2 Inputs: CLK, DI, PWM 1, PWM 2

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. $6V \leq V_S \leq 18V$; $4.5V \leq V1 \leq 5.3V$; all outputs open; $T_j = -40^\circ\text{C} \dots 130^\circ\text{C}$, unless otherwise specified.

Table 29. Inputs: CLK, DI, PWM 1, PWM 2

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---------|-----------------------|--|---|------|------|------|---------------|
| 7.14.6 | t_{set} | Delay time from standby to active mode | Switching from standby to active mode. Time until output drivers are enabled after CSN going to high. | | 160 | 300 | μs |
| 7.14.7 | $V_{\text{in L}}$ | Input low level | $V1 = 5 V$ | 1.0 | 2.05 | 2.5 | V |
| 7.14.8 | $V_{\text{in H}}$ | Input high level | $V1 = 5 V$ | 1.5 | 2.8 | 3.3 | V |
| 7.14.9 | $V_{\text{in Hyst}}$ | Input hysteresis | $V1 = 5 V$ | 0.4 | 0.75 | 1.5 | V |
| 7.14.10 | I_{in} | Pull down current at input | $V_{\text{in}} = 1.5 V$ | 5 | 30 | 60 | μA |
| 7.14.11 | $C_{\text{in}}^{(1)}$ | Input capacitance at input CSN, CLK, DI and PWM _{1,2} | $0V < V1 < 5.3V$ | | 10 | 15 | pF |
| 7.14.12 | f_{CLK} | SPI input frequency at CLK | | | | 1 | MHz |

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

7.14.3 Input PWM 2 Vth for flash mode

The voltages are referred to ground.

$6V \leq V_S \leq 18V$; $4.5V \leq V1 \leq 5.3V$; all outputs open; $T_j = -40^\circ\text{C} \dots 130^\circ\text{C}$, unless otherwise specified.

Table 30. Input PWM2 Vth for flash mode

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---------|--------------|--------------------------------|-------------------|------|------|------|------|
| 7.14.13 | V_{inL} | Input low level (Vin rising)) | $V1 = 5\text{ V}$ | 6.1 | 7.25 | 8.4 | V |
| 7.14.14 | V_{inH} | Input high level (Vin falling) | $V1 = 5\text{ V}$ | 7.4 | 8.4 | 9.4 | V |
| 7.14.15 | V_{inHyst} | Input hysteresis | $V1 = 5\text{ V}$ | 0.6 | 0.8 | 1.0 | V |

7.14.4 DI timing

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. $6V \leq V_S \leq 18V$; $4.5V \leq V1 \leq 5.3V$; all outputs open; $T_j = -40^\circ\text{C} \dots 130^\circ\text{C}$, unless otherwise specified.

Table 31. DI timing

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---------|----------------|--|-------------------|------|------|------|------|
| 7.14.16 | t_{CLK} | Clock period | $V1 = 5\text{ V}$ | 1000 | - | | ns |
| 7.14.17 | t_{CLKH} | Clock high time | $V1 = 5\text{ V}$ | 400 | - | | ns |
| 7.14.18 | t_{CLKL} | Clock low time | $V1 = 5\text{ V}$ | 400 | - | | ns |
| 7.14.19 | $t_{set\ CSN}$ | CSN setup time, CSN low before rising edge of CLK | $V1 = 5\text{ V}$ | 400 | - | | ns |
| 7.14.20 | $t_{set\ CLK}$ | CLK setup time, CLK high before rising edge of CSN | $V1 = 5\text{ V}$ | 400 | - | | ns |
| 7.14.21 | $t_{set\ DI}$ | DI setup time | $V1 = 5\text{ V}$ | 200 | - | | ns |
| 7.14.22 | $t_{hold\ DI}$ | DI hold time | $V1 = 5\text{ V}$ | 200 | - | | ns |
| 7.14.23 | t_{r_in} | Rise time of input signal DI, CLK, CSN | $V1 = 5\text{ V}$ | | - | 100 | ns |
| 7.14.24 | t_{f_in} | Fall time of input signal DI, CLK, CSN | $V1 = 5\text{ V}$ | | - | 100 | ns |

7.14.5 DO, FSO, Dig_Out3,4

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. $6V \leq V_S \leq 18V$; $4.5V \leq V1 \leq 5.3V$; all outputs open; $T_j = -40^\circ\text{C} \dots 130^\circ\text{C}$, unless otherwise specified.

Table 32. DO, FSO, Digout3,4

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---------|------------------|----------------------------|---|------|------|------|---------------|
| 7.14.25 | V_{DOL} | Output low level | $V1 = 5\text{ V}, I_D = -4\text{ mA}$ | | | 0.5 | V |
| 7.14.26 | V_{DOH} | Output high level | $V = 5\text{ V}, I_D = 4\text{ mA}$ | 4.5 | | | V |
| 7.14.27 | $I_{DOLK}^{(1)}$ | Tristate leakage current | $V_{CSN} = V1,$ $0\text{ V} < V_{DO} < V1$ | -10 | | 10 | μA |
| 7.14.28 | C_{DO} | Tristate input capacitance | $V_{CSN} = V1,$ $0\text{ V} < V1 < 5.3\text{ V}$ | | 10 | 15 | pF |

1. Not valid for FSO

7.14.6 DO timing

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. $6V \leq V_S \leq 18V$; $4.5V \leq V1 \leq 5.3V$; all outputs open; $T_j = -40^\circ\text{C} \dots 130^\circ\text{C}$, unless otherwise specified.

Table 33. DO timing

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---------|--------------------------|---|---|------|------|------|------|
| 7.14.29 | t_{rDO} | DO rise time | $C_L = 100\text{ pF},$ $I_{load} = -1\text{ mA}$ | - | 50 | 100 | ns |
| 7.14.30 | t_{fDO} | DO fall time | $C_L = 100\text{ pF},$ $I_{load} = 1\text{ mA}$ | - | 50 | 100 | ns |
| 7.14.31 | $t_{enDO\text{ tri L}}$ | DO enable time from tristate to low level | $C_L = 100\text{ pF},$ $I_{load} = 1\text{ mA}$ pull-up load to V1 | - | 50 | 250 | ns |
| 7.14.32 | $t_{disDO\text{ L tri}}$ | DO disable time from low level to tristate | $C_L = 100\text{ pF},$ $I_{load} = 4\text{ mA}$ pull-up load to V1 | - | 50 | 250 | ns |
| 7.14.33 | $t_{enDO\text{ tri H}}$ | DO enable time from tristate to high level | $C_L = 100\text{ pF},$ $I_{load} = -1\text{ mA}$ pull-down load to GND | - | 50 | 250 | ns |
| 7.14.34 | $t_{disDO\text{ H tri}}$ | DO disable time from high level to tristate | $C_L = 100\text{ pF},$ $I_{load} = -4\text{ mA}$ pull-down load to GND | - | 50 | 250 | ns |
| 7.14.35 | t_{dDO} | DO delay time | $V_{DO} < 0.3\text{ V}1,$ $V_{DO} > 0.7\text{ V}1,$ $C_L = 100\text{ pF}$ | - | 50 | 250 | ns |

7.14.7 CSN timing

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. $6V \leq V_S \leq 18V$; $4.5V \leq V1 \leq 5.3V$; all outputs open; $T_j = -40^\circ C \dots 130^\circ C$, unless otherwise specified.

Table 34. CSN timing

| Item | Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---------|-------------------|----------------------------------|---|------|------|------|---------|
| 7.14.36 | $t_{CSN_HI,min}$ | Minimum CSN HI time, active mode | Transfer of SPI-command to input register | 6 | - | - | μs |

Figure 16. SPI - Input timing

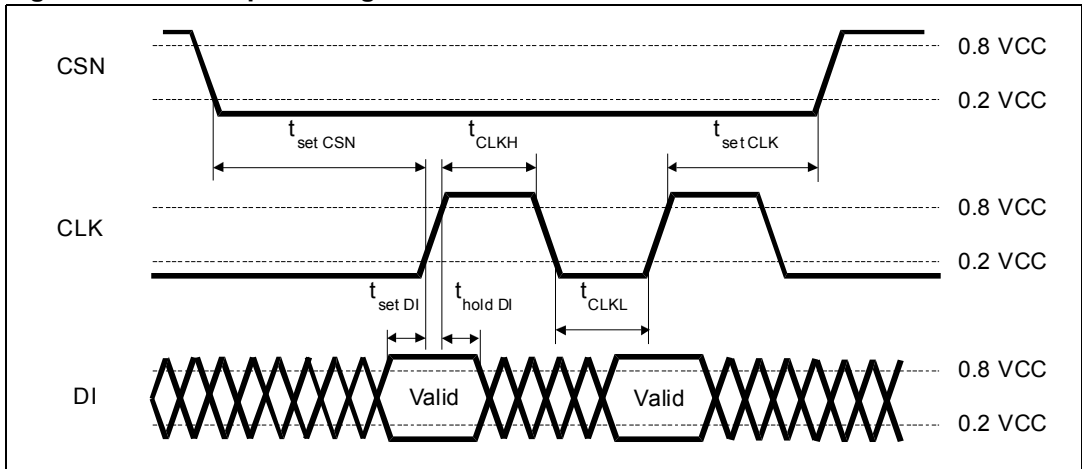


Figure 17. SPI - Edges timing

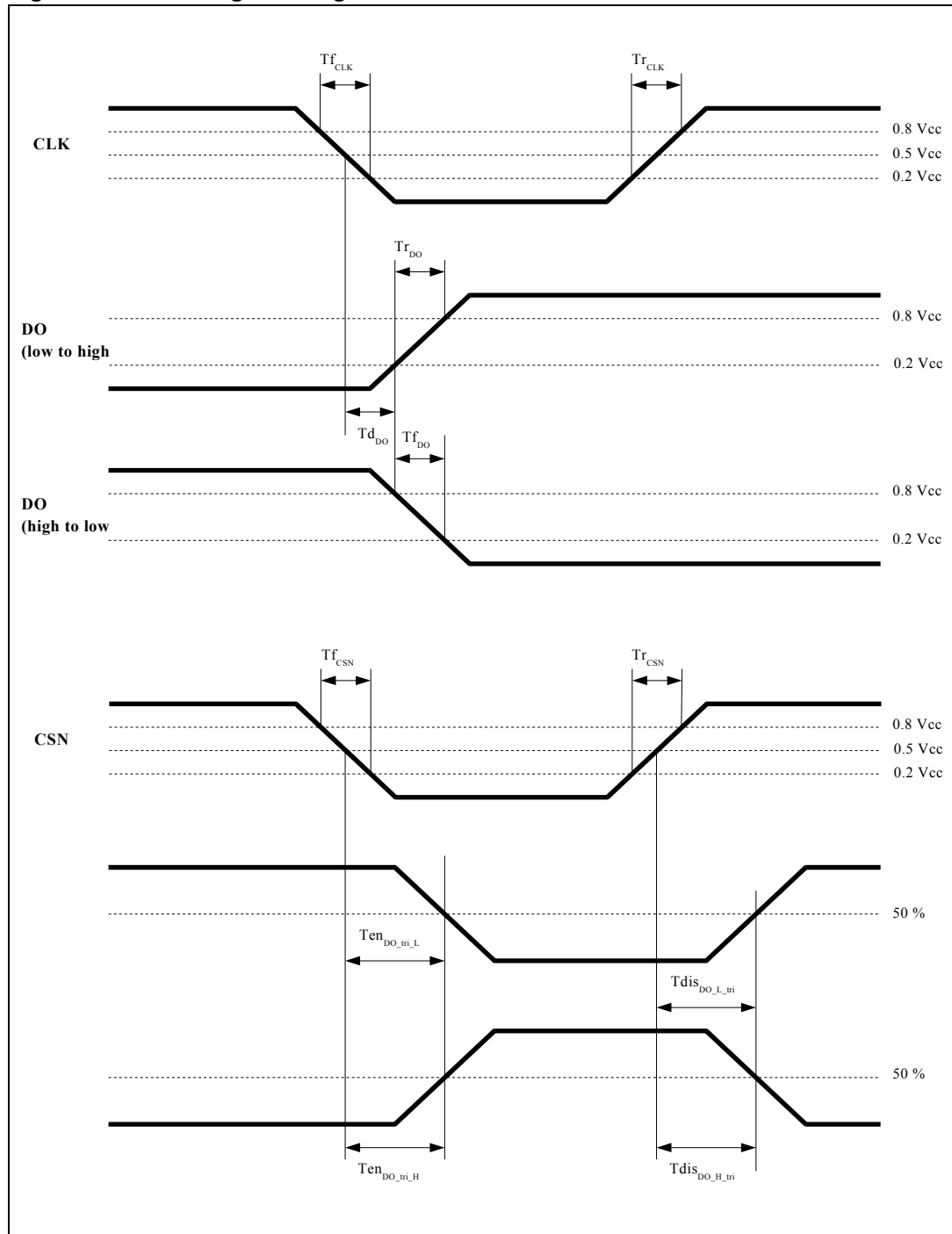


Figure 18. SPI - CSN low to high transition

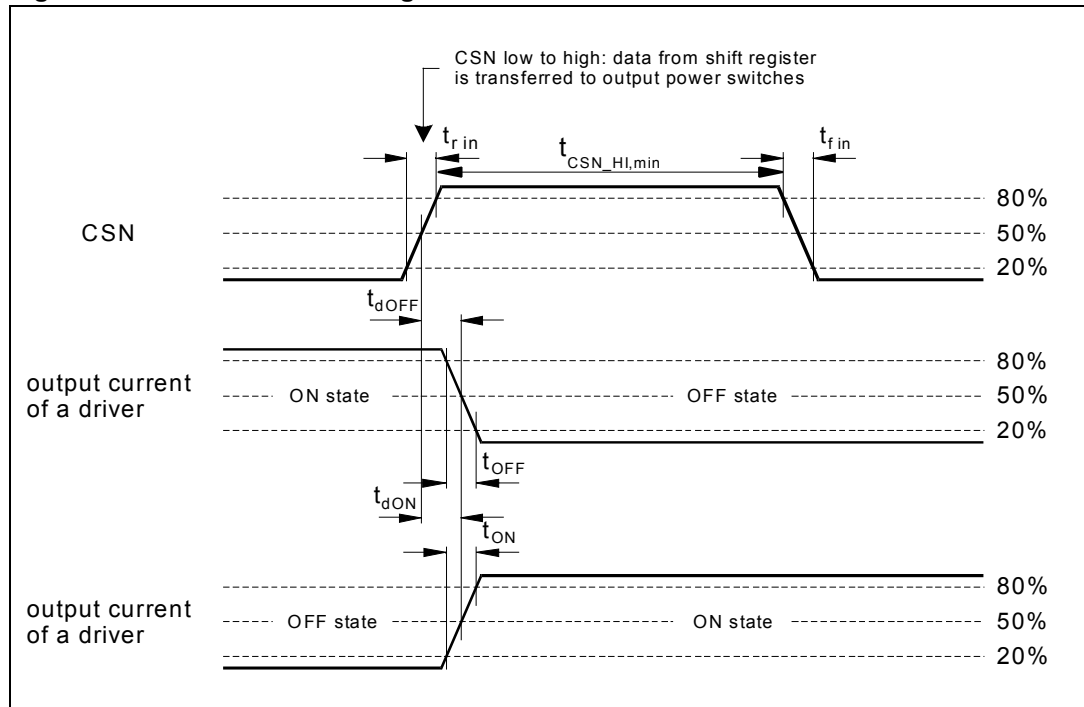
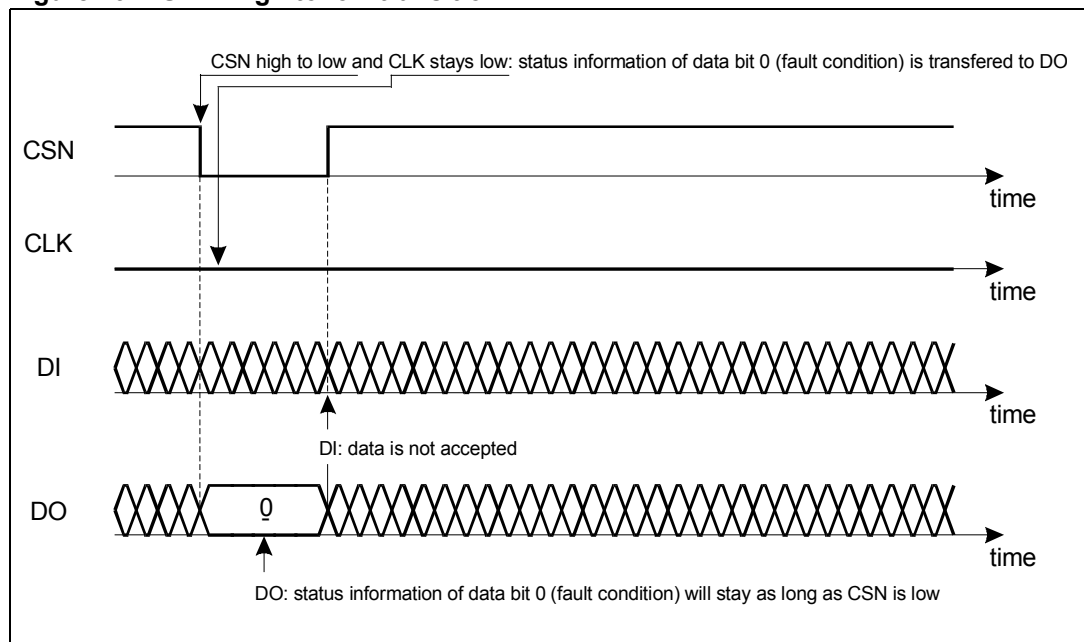


Figure 19. SPI - High to low transition



8 SPI control and status registers

8.1 SPI registers

24bit shift register: first 2 bits are address (A1,A0) and 22 bits are data.

During power-on reset, all registers are set to zero.

Table 35. SPI registers

| | | | | | | | | | | | | | | | | | | | | | | | |
|--------------------|--------|------------------|------------|-----------|---------|---------------------|-------|---------|---------|-------------|---------------|---------|-------|--------------------|-------------------|-----------------------|-----------------------|-----------|----------------|---------|---------|---------|-----|
| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D09 | D08 | D07 | D06 | D05 | D04 | D03 | D02 | D01 | D00 |
| A1 | A0 | Data | | | | | | | | | | | | | | | | | | | | | |
| Address | | | | | | | | | | | | | | | | | | | | | | | |
| [write] | | On5V2 | | | | On Signals | | | | | | | | | | | | | | | | | |
| Control Register 0 | GO VCC | GO VBAT | TRIG | ON V21 | ON V20 | REL 2 | REL 1 | OUT HS2 | OUT HS1 | OUT HS0 | HS 42 | HS 41 | HS 40 | HS 32 | HS 31 | HS 30 | HS 22 | HS 21 | HS 20 | HS 12 | HS 11 | HS 10 | |
| 0 | 0 | Address | | | | | | | | | | | | | | | | | | | | | |
| [write] | | Timer 2 | | Timer 1 | | | | Loop | | | Pullup / down | | | | Wakeup Sources OL | | | | Wakeup Sources | | | | |
| Control Register 1 | CLR | INT_en | T20 | T13 | T12 | T11 | T10 | L2 | L1 | L0 | U3 | U2 | U1 | U0 | W7 | W6 | W5 | W4 | W3 | W2 | W1 | W0 | |
| 0 | 1 | Address | | | | | | | | | | | | | | | | | | | | | |
| [write] | | Input config | | | | | | | | Reset level | | LIN | | Openload threshold | | | | | | | | | |
| Control Register 2 | RES | I _{CMP} | LS OVUV | LIN Slope | IC 41 | IC 40 | IC 31 | IC 30 | IC 21 | IC 20 | IC 11 | IC 10 | LEV 1 | LEV 0 | TXT TOUT | LINPU | O_HS REC | VLOCK OUT | OLT HS4 | OLT HS3 | OLT HS2 | OLT HS1 | |
| 1 | 0 | Address | | | | | | | | | | | | | | | | | | | | | |
| [read] | | Reserved | | Wakeup | | Wakeup input status | | | | Overcurrent | | | | | | Openload | | | | | | | |
| Status Register 0 | RES | RES | COLD START | LIN | INH | WU4 | WU3 | WU2 | WU1 | SHT5 V2 | Rel2 OC | Rel1 OC | HS OC | HS4 OC | HS3 OC | HS2 OC | HS1 OC | HS OL | HS4 OL | HS3 OL | HS2 OL | HS1 OL | |
| Err | Err | Address | | | | | | | | | | | | | | | | | | | | | |
| | | Reserved | | LIN State | | Watchdog Reset | | | | 5V Restarts | | | State | | | | | | | | | | |
| Status Register 1 | RES | RES | DOM TXD | SHT BAT | SHT GND | TRIG | WD 3 | WD 2 | WD 1 | WD 0 | R2 | R1 | R0 | ST1 | ST0 | VCC ₂ Fail | VCC ₁ Fail | TSD 2 | TSD 1 | TW | UV | OV | |
| Err | Err | Address | | | | | | | | | | | | | | | | | | | | | |

Note: During the shift in of the address bits, (2 clock periods) an internal error bit (Err) is fed to the DO output.

D23,D22 -> error flags (seen from DO)

The error flag is generated by logic OR combination of following error bits:

VCC_Fail1,2; TSD1,2; TW; OV,UW; OC_HS1..4; OC_OUTHS; OC_REL1..2; OC_V2

8.1.1 Control register 0

While writing to the control register 0, the status register 0 can be read at the DO-Output of the SPI.

Table 36. Control register 0

| | | | | 5V2 | | Driver ON Signals | | | | | | | | | | | | | | | | | |
|--------|-------|---------------------|------|--------|--------|-------------------|-------|---------|---------|---------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|---|
| Bit | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Access | w | w | w | w | w | w | w | w | w | w | w | w | w | w | w | w | w | w | w | w | w | w | w |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Name | GO V1 | GO V _{bat} | TRIG | ON V21 | ON V20 | REL 2 | REL 1 | OUT HS2 | OUT HS1 | OUT HS0 | HS 42 | HS 41 | HS 40 | HS 32 | HS 31 | HS 30 | HS 22 | HS 21 | HS 20 | HS 12 | HS 11 | HS 10 | |

Table 37. Configuration bit HSxx

| Name / state | | | Definition/ function |
|--------------|------|------|---|
| HSx2 | HSx1 | HSx0 | Defines the output configuration of the High Side Drivers 1-4 |

Table 38. Configuration bit OUT_HSx

| Name / state | | | Definition/ function |
|--------------|----------|----------|---|
| OUT_HS 2 | OUT_HS 1 | OUT_HS 0 | Defines the output configuration of the High Side Driver OUT_HS |
| 0 | 0 | 0 | Driver is OFF in all modes |
| 0 | 0 | 1 | Driver is ON in active mode, off in standby mode |
| 0 | 1 | 0 | Driver is cyclic ON with the timing of Timer 1 in active mode and standby modes |
| 0 | 1 | 1 | Driver is cyclic ON with the timing of Timer 2 in active mode and standby modes |
| 1 | 0 | 0 | Driver is controlled by the PWM1 Input |
| 1 | 0 | 1 | Driver is controlled by the PWM2 Input |

Table 39. Configuration bit RELx

| Name / state | | Definition/ function |
|--------------|--|--|
| RELx | | Defines the Output configuration of the low side relay drivers 1/2 |
| 0 | | Driver is OFF in all modes |
| 1 | | Driver is ON in active mode (off in standby mode) |

Table 40. Configuration bit On_V2x

| Name / state | | Definition/ function |
|--------------|--------|--|
| On_V21 | On_V20 | Defines in which modes the voltage regulator 2 is on |
| 0 | 0 | Voltage regulator 2 is OFF in all modes |

Table 40. Configuration bit On_V2x (continued)

| Name / state | | Definition/ function |
|--------------|---|--|
| 0 | 1 | Voltage regulator 2 is ON in ACTIVE mode; OFF in V ₁ -standby, V _{Bat} -standby |
| 1 | 0 | Voltage regulator 2 is ON in ACTIVE mode and V ₁ standby; OFF in V _{bat} -standby |
| 1 | 1 | Voltage regulator 2 is ON in all modes |

Table 41. Configuration bit TRIG, GO_VBAT, GO_V1

| | |
|---------|--|
| TRIG | Trigger bit for watchdog; inverted for each Trigger event invert this bit for a proper watchdog trigger. |
| GO_VBAT | "1" enters the V _{bat} -standby mode. (dominant mode, if both standby modes are selected) |
| GO_V1 | "1" enters the V ₁ -standby mode. |

8.1.2 Control register 1

While writing to the control register 1, the status register 1 can be read at the DO-Output of the SPI.

Table 42. Control register 1

| Bit | Cyclic Timer 1/2 | | | | | | | Loop | | | Pull up | | | | Wakeup Sources | | | | | | | | |
|--------|------------------|--------|-----|-----|-----|-----|-----|------|----|----|---------|----|----|----|----------------|----|----|----|----|----|----|----|---|
| | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Access | w | w | w | w | w | w | w | w | w | w | w | w | w | w | w | w | w | w | w | w | w | w | w |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Name | CLR | INT_EN | T20 | T13 | T12 | T11 | T10 | L2 | L1 | L0 | U3 | U2 | U1 | U0 | W7 | W6 | W5 | W4 | W3 | W2 | W1 | W0 | |

Table 43. Configuration bit Wx

| Name/state | | | | | | | | Definition/function |
|------------|----|----|----|----|----|----|----|--|
| W7 | W6 | W5 | W4 | W3 | W2 | W1 | W0 | Disables the corresponding wake up sources |
| x | x | x | x | x | x | x | 1 | Input WU1 is disabled as wake up source |
| x | x | x | x | x | x | 1 | x | Input WU2 is disabled as wake up source |
| x | x | x | x | x | 1 | x | x | Input WU3 is disabled as wake up source |
| x | x | x | x | 1 | x | x | x | Input WU4 is disabled as wake up source |
| x | x | x | 1 | x | x | x | x | Open load Appearance / Disappearance at OUT1 is disabled as wake up source |
| x | x | 1 | x | x | x | x | x | Open load Appearance / Disappearance at OUT2 is disabled as wake up source |
| x | 1 | x | x | x | x | x | x | Open load Appearance / Disappearance at OUT3 is disabled as wake up source |

Table 43. Configuration bit Wx (continued)

| Name/state | | | | | | | | Definition/function |
|------------|---|---|---|---|---|---|---|--|
| 1 | x | x | x | x | x | x | x | Open load Appearance / Disappearance at OUT4 is disabled as wake up source |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Default: all wake up sources are enabled |

Table 44. Configuration bit Ux

| Name/state | | | | Definition/function |
|------------|----|----|----|---|
| U3 | U2 | U1 | U0 | Defines whether the Inputs WU1..4 are configured with current source or current sink in standby mode. |
| x | x | x | 1 | Input WU1 configured with a current source in standby mode (R _{WU_act} pulldown resistor in active mode - see Table 20.) |
| x | x | 1 | x | Input WU2 configured with a current source in standby mode (R _{WU_act} pulldown resistor in active mode - see Table 20.) |
| x | 1 | x | x | Input WU3 configured with a current source in standby mode (R _{WU_act} pulldown resistor in active mode - see Table 20.) |
| 1 | x | x | x | Input WU4 configured with a current source in standby mode (R _{WU_act} pulldown resistor in active mode - see Table 20.) |
| 0 | 0 | 0 | 0 | Default: All Inputs configured with a current sink in standby (R _{WU_act} pulldown resistor in active mode - see Table 20.) |

Table 45. Configuration bit Lx

| Name/state | | | Definition/function | |
|------------|----|----|--|---------------|
| L2 | L1 | L0 | Defines which signal is looped to the Dig_Out3 and Dig_Out4 (see note) | |
| | | | Dig_Out3 | Dig_Out4 |
| 0 | 0 | 0 | WU3 (default) | WU4 (default) |
| 0 | 0 | 1 | HighZ | WU4 |
| 0 | 1 | 0 | WU3 | HighZ |
| 0 | 1 | 1 | WU3 | Open Load HS2 |
| 1 | 0 | 0 | Open Load HS1 | WU4 |
| 1 | 0 | 1 | Open Load HS1 | Open Load HS2 |
| 1 | 1 | 0 | Open Load HS1 | HighZ |
| 1 | 1 | 1 | HighZ | Open Load HS2 |

Table 46. Configuration bit Txx

| Name/state | | | Definition/function |
|------------|-----|-----|--|
| T12 | T11 | T10 | Defines the period of the cyclic sense Timer 1 which is selectable for Out 1..4 and Out_HS (see ON signals control register 0) |
| 0 | 0 | 0 | Period: 0.5 s |
| 0 | 0 | 1 | Period: 1.0 s |
| 0 | 1 | 0 | Period: 1.5 s |
| 0 | 1 | 1 | Period: 2.0 s |
| 1 | 0 | 0 | Period: 2.5 s |
| 1 | 0 | 1 | Period: 3.0 s |
| 1 | 1 | 0 | Period: 3.5 s |
| 1 | 1 | 1 | Period: 4.0 s |
| T13 | | | Defines the ON time for the cyclic sense Timer1 |
| 0 | | | ON time 10 ms |
| 1 | | | ON time 20 ms |
| T20 | | | Defines the ON time of the cyclic sense Timer 2 which is selectable for Out 1..4 and OUTHS (see ON Signals control register 0) |
| 0 | | | Period 50 ms / ON time 100 us |
| 1 | | | Period 50 ms / ON time 1ms |

Table 47. Configuration bit INT_enable

| Name/state | Definition/function |
|------------|---|
| INT_enable | |
| 0 | Interrupt Mode disabled (see Section 2.7) |
| 1 | Interrupt Mode enabled |
| CLR | Clears the contents of status register 0 and 1 |

Note: In V_{BAT} standby mode, DigOut 3 and DigOut4 are HighZ.

8.1.3 Control register 2

While writing to the control register 2, the status register 0 can be read at the DO-Output of the SPI.

Table 48. Control register 2

| Bit | Input filter configuration | | | | | | | | | | | | Reset level | | LIN | | Open load threshold | | | | | |
|--------|----------------------------|-------------------|---------|-----------|-------|-------|-------|-------|-------|-------|-------|-------|-------------|-------|----------|--------|---------------------|-------------|---------|---------|---------|---------|
| | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | W | | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W | W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Name | RES | I _{COMP} | LSO VUV | LIN Slope | IC 41 | IC 40 | IC 31 | IC 30 | IC 21 | IC 20 | IC 11 | IC 10 | LEV 1 | LEV 0 | TXDT Out | LINP U | O_HS REC | VS Lock Out | OLT HS4 | OLT HS3 | OLT HS2 | OLT HS1 |

Table 49. Configuration bit OLT_HSx, VSLOCK Out, O_HS_REC, LINPU and TXD_TOUT

| Name/state | Definition/function |
|------------|--|
| OLT_HSx | Open load threshold for the High Side Drivers Out1..4 0: I _{openload} = 2mA; 1: I _{openload} = 8mA |
| VSLOCK Out | Automatic recovery after VS Over/Under voltage “0” (default): Vs lockout is disabled, i.e. outputs will automatically recover (according to output settings in CR0) after Vs over / under - voltage conditions has disappeared “1”: Vs lockout is enabled, i.e. outputs will remain Off after Vs over / under voltage recovery conditions has disappeared, until the Vs over / under voltage Status Bits (SR1, bit s0,1) are cleared by CLR command (CR1, bit 21). |
| O_HS_REC | “1” = Recovery mode for OUT_HS Driver. |
| LINPU | “1” will disable the master pull up LINPU |
| TXD_TOUT | “1” will disable the dominant TxD time-out for the LIN Interface. |

Table 50. Configuration bit LEVx

| Name/state | | Definition/function |
|------------|------|--|
| LEV1 | LEV0 | Controls the reset level |
| 0 | 0 | Set the reset threshold to 4.65V, typ. |
| 0 | 1 | Set the reset threshold to 4.35V, typ. |
| 1 | X | Reserved (do not use for operation, set LEV1 to “0”) |

Table 51. Configuration bit ICxx

| Name/state | | Definition/function | |
|------------|-----------|---|---|
| IC(1..4)1 | IC(1..4)0 | Selects the filter configuration for the Wakeup Inputs WU1 to 4 | |
| IC11 | 0 | 0 | Filter with 64 us Filter time (static sense) |
| IC21 | 0 | 1 | Enable Filter after 80 us with a Filter time of 16 us (cyclic sensing), timer2 |
| IC31 | 1 | 0 | Enable Filter after 800 us with a Filter time of 16 us (cyclic sensing), timer2 |
| IC41 | 1 | 1 | Enable Filter after 800 us with a Filter time of 16 us (cyclic sensing), timer1 |

Table 52. Configuration bit LIN slope, LS_ovuv and ICMP

| Name/state | Definition/function |
|------------|--|
| LIN slope | Change LIN slope |
| 0 | High slew rate (default) |
| 1 | Low slew rate |
| LS_ovuv | Vs Over / Under voltage shutdown of REL1,2 (low side drivers) |
| 0 | Enable (default): REL1,2 turned Off in case of Vs Over/Undervoltage |
| 1 | Disable : REL1,2 remain On in case of Vs Over/Undervoltage |
| ICMP | Current supervision of V1 regulator in V ₁ -standby mode. |
| 0 | Enable (default) |
| 1 | Disable |
| RES | Reserved |

8.1.4 Status register 0

The contents of the status register 0 can be read implicitly, while accessing the control register 0 or control register 2.

Table 53. Status register 0

| Bit | Wakeup Inputs | | | | | | | | | Over current | | | | | | | | Open load | | | | |
|--------|---------------|-----|------------|-----|-----|------|------|------|------|--------------|---------|---------|-------|--------|--------|--------|--------|-----------|--------|--------|--------|--------|
| | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Name | RES | RES | Cold Start | LIN | INH | WU 4 | WU 3 | WU 2 | WU 1 | SHT5V2 | REL 2OC | REL 1OC | HS OC | HS 4OC | HS 3OC | HS 2OC | HS 1OC | HS OL | HS 4OL | HS 3OL | HS 2OL | HS 1OL |

Table 54. Configuration bit HSx_OL, HSx_OC and Relx_OC

| Name/state | Definition/function |
|------------|--|
| HS1..4_OL | Open load status from the High Side Driver OUT1..4. |
| 0 | No open load has been detected. |
| 1 | Open load has been detected. |
| HS_OL | Open load status from the High Side Driver OUT_HS |
| 0 | No open load has been detected. |
| 1 | Open load has been detected. |
| HS1..4_OC | Over current status from the High Side Driver OUT1..4. |
| 0 | No over current has been detected. |
| 1 | Over current has been detected. |
| HS_OC | Over current status from the High Side Driver OUT_HS. |
| 0 | No over current has been detected. |
| 1 | Over current has been detected. |
| Rel 1,2_OC | Over current status from Relais1,2 |
| 0 | No over current has been detected. |
| 1 | Over current has been detected. |

Table 55. Configuration bit SHT5V2, WUx, INH, LIN and Cold Start

| Name/state | Definition/function |
|------------|---|
| SHT5V2 | V2 short to ground at turn on; condition: V2 < 2V for more than 4ms. "1" = fail |
| WU4...WU1 | Status of the corresponding Inputs WU1..4 (according to filter settings in CR2) |

Table 55. Configuration bit SHT5V2, WUx, INH, LIN and Cold Start (continued)

| Name/state | Definition/function |
|------------|---|
| INH | Wakeup initiated through INH source |
| LIN | Wakeup initiated through LIN source |
| Cold Start | Set to high when the internal Power on Reset occurs. Will be cleared with the first SPI access. |

Note: RES = reserved bits.

8.1.5 Status register 1

The contents of the status register 1 can be read implicitly, while accessing the control register 1.

Table 56. Status register 1

| | | LIN state | | | | | WD resets | | | | | 5V restarts | | | State | | | | | | | | | |
|--------|-----|-----------|---------|---------|---------|------|-----------|------|------|------|----|-------------|----|-----|-------|---------|---------|-------|-------|----|----|----|---|--|
| Bit | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| Access | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r | r | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| Name | RES | RES | DOM TXD | SHT BAT | SHT GND | TRIG | WD 3 | WD 2 | WD 1 | WD 0 | R2 | R1 | R0 | ST1 | ST0 | V2 Fail | V1 Fail | TSD 2 | TSD 1 | TW | UV | OV | | |

Table 57. Configuration bit OV, UV, TW, TSDx and Vx Fail

| Name | Definition, function |
|---------|--|
| OV | Over voltage failure of Vs. |
| UV | Under voltage failure of Vs. |
| TW | Temperature Warning: the chip temperature exceeds 130°C |
| TSD1 | Thermal shutdown #1: The chip temperature exceeds 140°C All Outputs, except the voltage regulator 1 are switched off. |
| TSD2 | Thermal shutdown #2: The chip temperature exceeds 155°C All Outputs, including the voltage regulator 1 are switched off. |
| V1 Fail | The output of Voltage Regulator 1 failed for at least 2µs. Conditions: (V1<2V for >2µs) OR (V1<2V at 4ms after turn-on). '1'= fail |
| V2 Fail | The output of Voltage Regulator 2 failed for at least 2µs. Conditions: (V2<2V for >2µs) OR (V2<2V at 4ms after turn-on). '1'= fail |

Table 58. Configuration bit STx

| Name | | Mode |
|------|-----|---|
| ST1 | ST0 | |
| 0 | 0 | Active mode |
| 0 | 1 | V1-standby -> a readout is wake up condition -> active mode -> 00 is read |

Table 58. Configuration bit STx (continued)

| Name | | Mode |
|------|---|---|
| 1 | 0 | VBat-standby, a readout is not possible, as V1 is off |
| 1 | 1 | Flash Mode |

Table 59. Configuration bit Rx, WDx, TRIG, SHT_GND, SHT_BAT and DOM_TXD

| Name | Definition, function |
|-----------------|--|
| R2 R1 R0 | Number of unsuccessfully restarts after thermal shutdown |
| WD3 WD2 WD1 WD0 | Number of Watchdog time-outs ⁽¹⁾ |
| TRIG | Status of the Trigger bit from Control Register 0 |
| SHT_GND | LIN Short to ground |
| SHT_BAT | LIN Short to battery |
| DOM_TXD | Dominant TXT |
| RES | Reserved |

1. Bits are cleared at every valid WD trigger or when forced sleep mode is entered (after 15 WD failures have been detected)

9 Package and packing information

9.1 ECOPACK[®] packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com.

ECOPACK[®] is an ST trademark.

9.2 PowerSSO-36 package information

Figure 20. PowerSSO-36 package dimensions

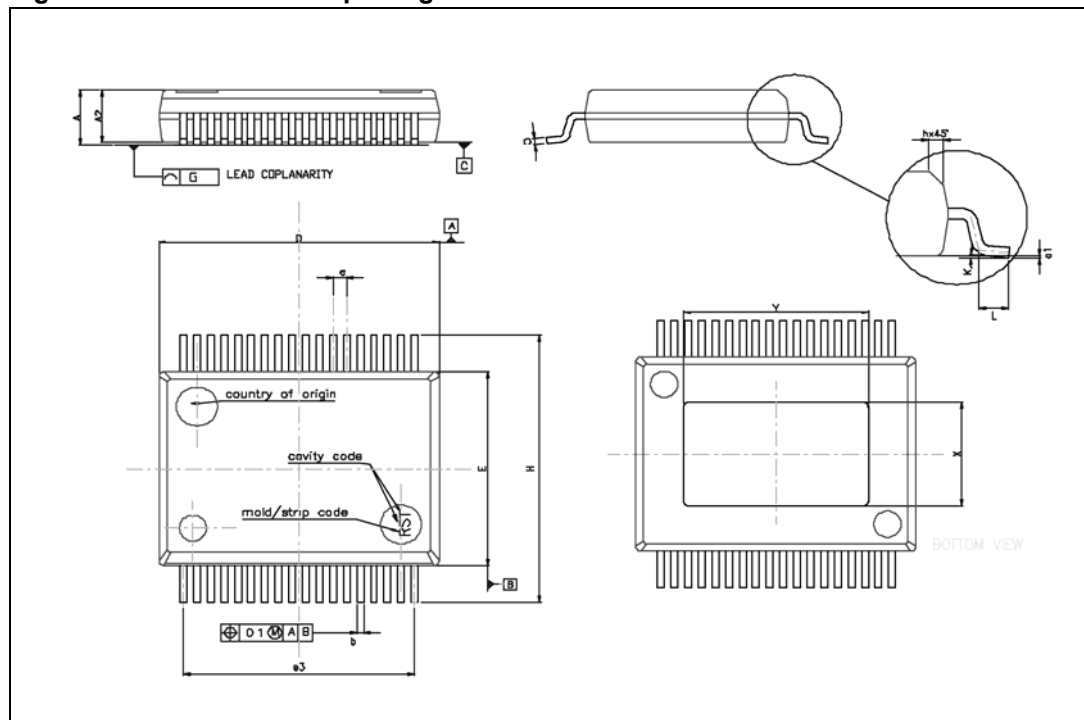


Table 60. PowerSSO-36 mechanical data

| Symbol | Millimeters | | |
|--------|-------------|------|------|
| | Min. | Typ. | Max. |
| A | - | - | 2.45 |
| A2 | 2.15 | - | 2.35 |
| a1 | 0 | - | 0.1 |
| b | 0.18 | - | 0.36 |
| c | 0.23 | - | 0.32 |

Table 60. PowerSSO-36 mechanical data (continued)

| Symbol | Millimeters | | |
|--------|-------------|------|--------|
| | Min. | Typ. | Max. |
| D | 10.10 | - | 10.50 |
| E | 7.4 | - | 7.6 |
| e | - | 0.5 | - |
| e3 | - | 8.5 | - |
| F | - | 2.3 | - |
| G | - | - | 0.1 |
| G1 | - | - | 0.06 |
| H | 10.1 | - | 10.5 |
| h | - | - | 0.4 |
| k | 0° | - | 8° |
| L | 0.55 | - | 0.85 |
| M | - | 4.3 | - |
| N | - | - | 10 deg |
| O | - | 1.2 | - |
| Q | - | 0.8 | - |
| S | - | 2.9 | - |
| T | - | 3.65 | - |
| U | - | 1.0 | - |
| X | 4.1 | - | 4.7 |
| Y | 6.5 | - | 7.1 |

9.3 PowerSSO-36 packing information

Figure 21. PowerSSO-36 tube shipment (no suffix)

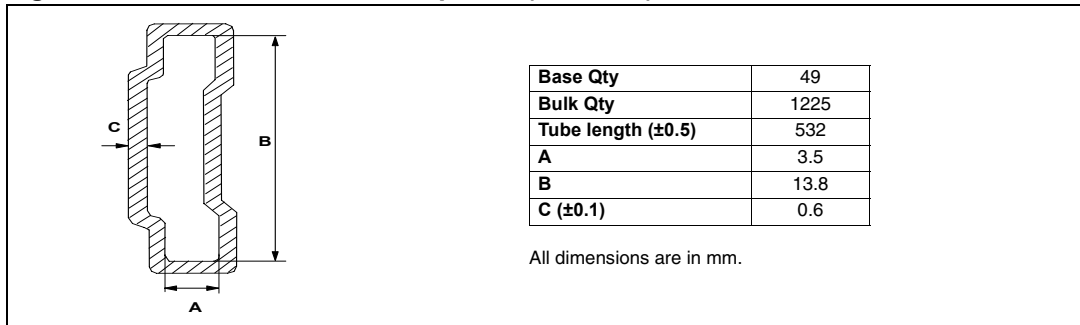
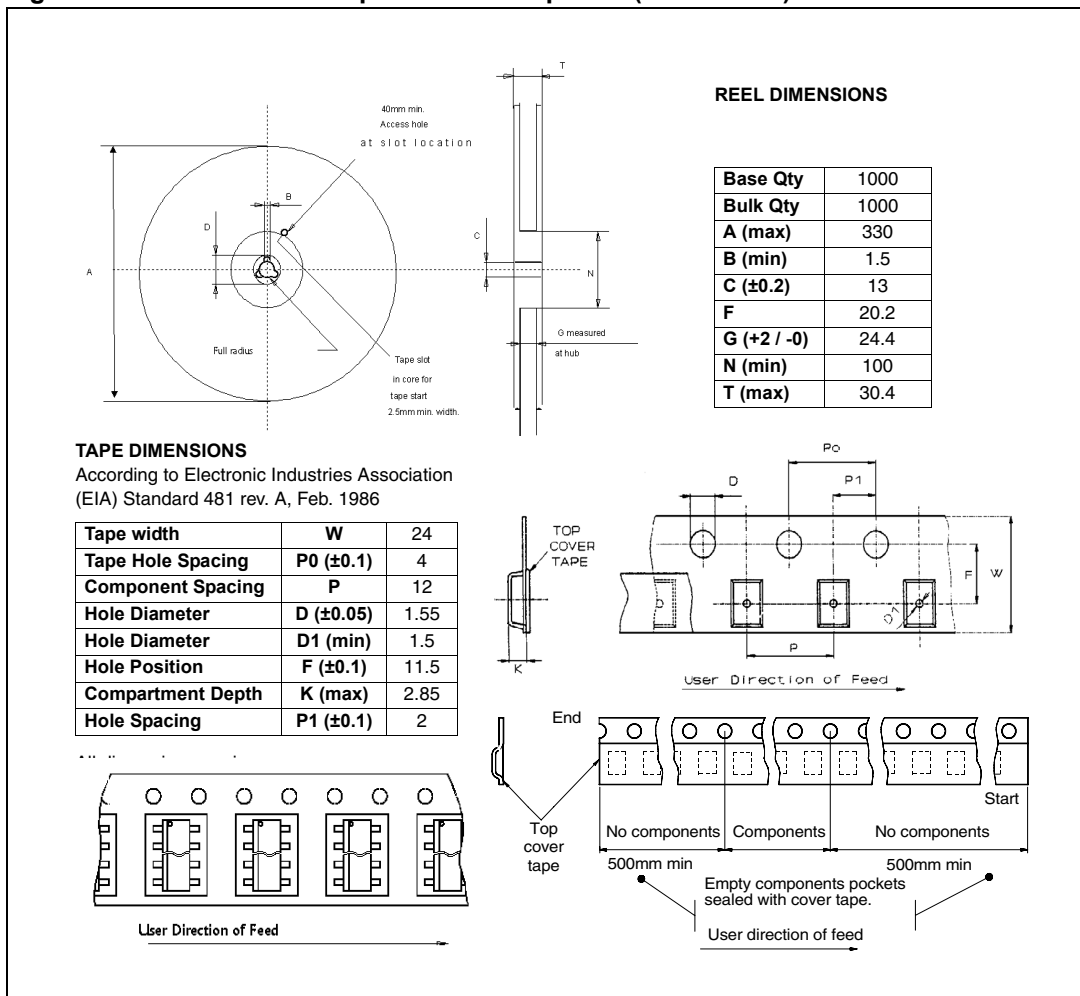


Figure 22. PowerSSO-36 tape and reel shipment (suffix "TR")



10 Revision history

Table 61. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 24-Aug-2007 | 1 | Initial release. |
| 07-Sep-2007 | 2 | <p>Table 18: High side outputs (OUT 1..4): modified openload detection current 1 parameter value (item 7.8.13).</p> <p>Table 20: Wake up inputs(WU1...WU4): modified Input current in standby mode test condition (item 7.10.5).</p> <p>Table 22: LIN receiver: modified symmetry of transmitter propagation delay time parameter value (item 7.12.24).</p> <p>Added Section 9.3: PowerSSO-36 packing information.</p> |
| 21-Sep-2007 | 3 | <p>Section 7.2: Oscillator: changed Vs minimum value from 7 to 6 V.</p> <p>Table 10: Supply and supply monitoring:</p> <ul style="list-style-type: none"> – changed parameter 7.1.10 ($I_{V(BATWU)}$) max value from 300 to 320 μA – changed parameter 7.1.11 ($I_{V(BATWU)}$) max value from 380 to 410 μA. |
| 11-Apr-2008 | 4 | <p>Modified Figure 4.: Watchdog</p> <p>Modified Section 2.13: Low side driver outputs Rel1, Rel2.</p> <p>Added note to Section 2.2.2: Flash mode.</p> <p>Section Table 48.: Control register 2: changed definition to V_S Lock Out parameter.</p> <p>Added Section 6.3: Package and PCB thermal data.</p> <p>Modified Section 7.14.3: Input PWM 2 Vth for flash mode.</p> <p>Table 42: Control register 1: modified "pull down" settings for the wake-up inputs WU1..4 .</p> |
| 08-Jul-2009 | 5 | <p>Table 60: PowerSSO-36 mechanical data:</p> <ul style="list-style-type: none"> – Deleted A (min) value – Changed A (max) value from 2.47 to 2.45 – Changed A2 (max) value from 2.40 to 2.35 – Changed a1 (max) value from 0.075 to 0.1 – Added k row – Changed G (max) value from 0.075 to 0.1 |

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2009 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com