1 Introduction

1.1 General Description

GM8164 is a static synchronously serial-input parallel-output or asynchronously parallel-input serial-output register, which mainly is for I/Os extension and completes the following functions:

- Serial-in/Parallel-out, latch output
- Parallel- in/Serial-out

1.2 Features

- Provides 32 Input Pins and 40 Output Pins
- Provides 8 Open-drain Output Pins
- Fully Synchronous Data Transfers
- Typical Shift Frequency 1MHz
- Very Low Power Consumption, 13 µA at 3.3V ,1MHz
- Very Low Quiescent Current, 3 µA at 3.3V
- 2.7V~ 5.6V Operating Voltage Range
- Expandable for n-Bit I/O Applications
- Serial-in/Parallel-out, Parallel-in/Serial-out Register pin function
- GM8164JN: 40 bit output, 32 bit input
  GM8164QP: 38 bit output, 32 bit input

1.3 APPLICATION

- I/O Expansion
- Serial Input / Parallel Output
- Parallel Input / Serial Output
- Shift Right Register
- Shift Right with parallel loading
- Address Register
- Buffer Register
- Bus System Register With Enable Parallel Lines at Bus Side

1.4 DESCRIPTION

The GM8164 is a CMOS device, a static eight-stage Serial-in, Parallel-out and Parallel-in, Serial-out register, It can be used to:

_ convert serial data to parallel form and direct the parallel data to either of five buses.

_ store parallel data.

_ accept parallel data from either of five buses and convert that data to serial form.

_ I/O Inputs that control the operations include

a single-phase CLOCK (CLK),
DATA LATCH ENABLE (LE),
DATA OUT ENABLE(OC) , and
PARAL LEL/SERIAL (I/O).

_ expand to hundreds I/O ports.

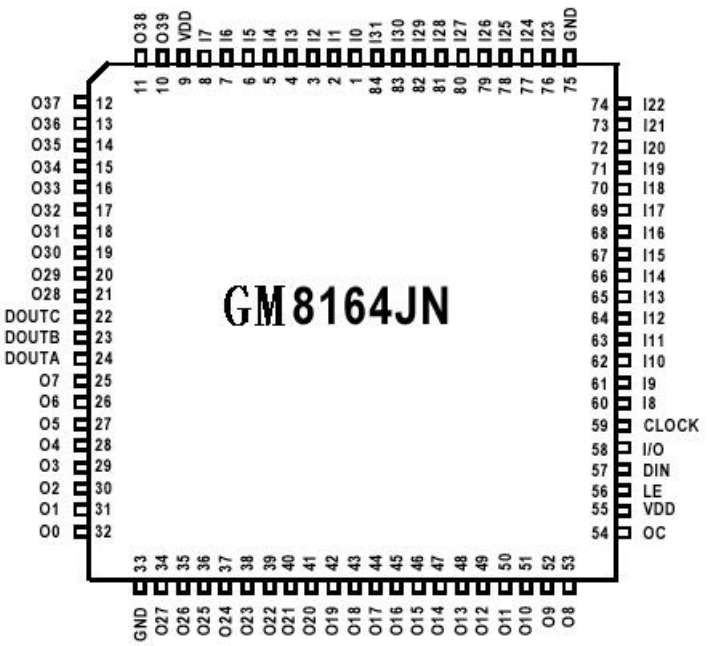
Both the shift and storage clocks are positive-edge triggered. Data inputs include 40 parallel data lines of which the eight O 0-O 7 data lines are inputs (open drain outputs) and O 8-O 39 data lines are inputs (outputs) depending on the signal level on the I/O input. All register stages are D-type master-slave flip-flops allowing synchronous or asynchronous data transfer from master to slave. Isolation from external noise and the effects of loading is provided by output buffering.

2 Specifications

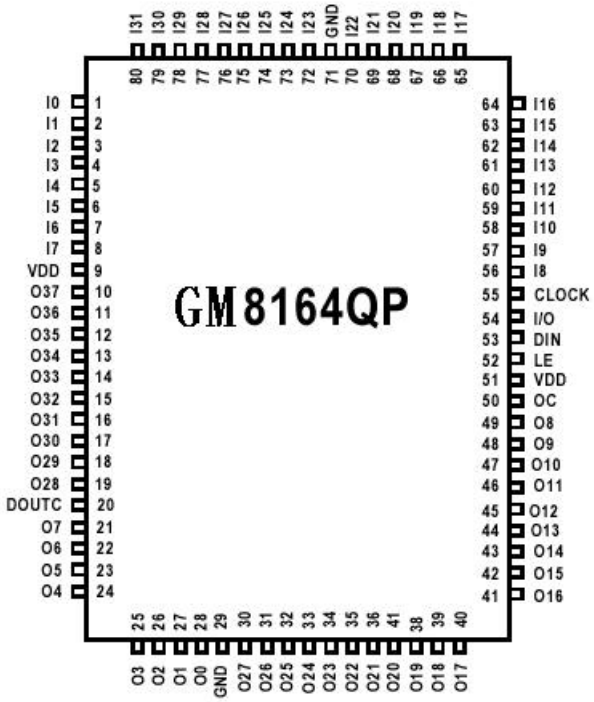
2.1 Pin Configuration

2.1.1 PIN OUT

PLCC-84



QFP-80



2.1.2 Pins Table

GM8164QP	GM8164JN	
$I_0 \sim I_{31}$:	$I_0 \sim I_{31}$:	Input port of asynchronous parallel data (Including Schemitt Trigger)
$O_0 \sim O_{37}$:	$O_0 \sim O_{39}$:	Parallel data output (O_0~O_7 are OC output, Input max high voltage 15V)
DIN :	DIN :	Synchronization serial data input port
	DOUTA(16 bits) :	Synchronization serial data output port
	DOUTB(32 bits) :	Synchronization serial data output port
DOUTC (38 bits)	DOUTC(40 bits) :	Synchronization serial data output port
CLK :	CLK :	Clock input port
I/O :	I/O :	Serial/parallel data input enable port
LE :	LE :	O_0~O_{39} parallel data output latch controller
OC :	OC :	O_0~O_{39} parallel data output enable controller
V_{CC} :	V_{CC} :	Power supply
GND :	GND :	Ground

2.1.3 TRUTH TABLE REGISTER INPUT-LEVELS ANDRESULTING REGISTER OPERATION

OC	LE	I/O	CLK	Function describe
0	0	0	↑	Synchronization serial-in/serial-out, register translocation. Input port is in the state of high- impedance resistor, output data will not change
0	0	0	none	Data from neither internal register nor output port will change, input port is in the state of high-impedance state
0	0	1	↑	Data from input port enter the internal register, output data will not change, internal register translocation is incapable
0	0	1	none	
0	1	0	↑	Synchronization serial-in/serial-out, input port is in the state of high-impedance state, register shifts and exports data to the output port
0	1	0	none	Input port is in the state of high-impedance state, data from neither internal register nor output port will be changed
0	1	1	↑	Data from input port enter the internal register, but can't shift. Data export from output port.
0	1	1	none	
1	0	0	↑	Synchronization serial-in/serial-out, internal register translocation, both input port and output port is in the state of high-impedance state
1	0	0	none	Both input port and output port is in the state of high-impedance state, data in internal register will not change
1	0	1	↑	Data from input port enter the internal register, but can't shift. Output port is in the state of high-impedance state
1	0	1	none	
1	1	0	↑	Synchronization serial-in/serial-out, internal register translocation, both input port and output port is in the state of high-impedance state
1	1	0	none	Both input port and output port is in the state of high-impedance state, data in internal register will not change
1	1	1	↑	Data from input port enter the internal register, but can't shift. Output port is in the state of high-impedance state
1	1	1	None	

2.2 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Units
V_{CC}	Supply voltage	-0.5 to +7	V
V_I	Voltage on input pins	-0.5 to V_{cc} + 0.5	V
V_O	Voltage on output pins	-0.5 to V_{cc} + 0.5	V
I_O	Short Circuit Output Current	25	mA
T_{STG}	Storage temperature	-65 to 150	℃
T_A	Operating temperature	-40 to 85	℃

2.3 RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage	2	6	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
T_A	Operating temperature	-25	+85	℃
t_r t_f	ascending ,descending time (V_{CC}=5 V)	0	500	ns

2.4 DC CHARACTERISTICS

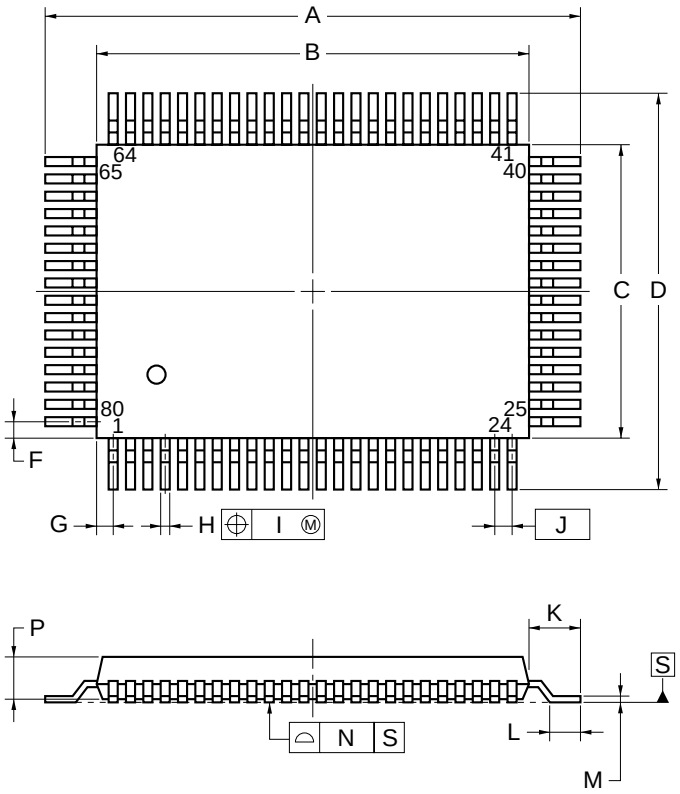
Parameter	Test condition		V_{CC} (V)	-40 ～+85℃		Unit
				min	max	
High-level input voltage V_{IH}			2	1.5		V
			6	4.2		V
Low-level input voltage V_{IL}			2		0.3	V
			6		1.2	V
Output high-level voltage V_{OH}	V_I=V_{IH} or V_{IL}	I_O =-20μA	2	1.9		V
		I_O =-5.2 mA	6	5.9		V
Output low-level voltage V_{OL}	V_I= V_{IH} or V_{IL}	I_O =20μA	2		0.1	V
		I_O =5.2mA	6		0.37	V
Input current I_I	V_I=V_{CC} or ground		6		±1	μA
Static current I_{CC}	V_I=V_{CC} or ground I_O = 0		6		80	μA

3 Application Example

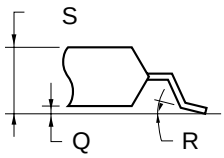
Please see 'AN8164.PDF' for details.

4 PACKAGING INFORMATION

80-PIN PLASTIC QFP (14x20)



detail of lead end



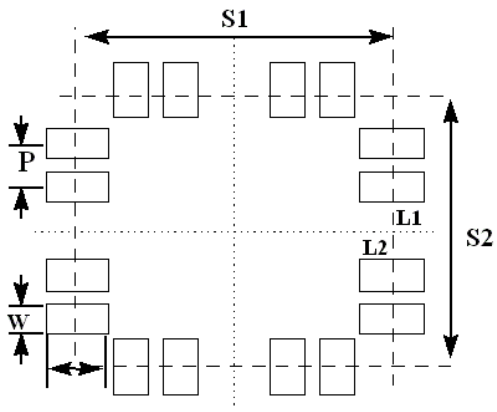
ITEM	MILLIMETERS
A	24.7±0.4
B	20.0±0.2
C	14.0±0.2
D	18.7±0.4
F	1.0
G	0.8
H	0.35±0.10
I	0.15
J	0.8 (T.P.)
K	2.35±0.2
L	1.2±0.2
M	$0.15^{+0.10}_{-0.05}$
N	0.15
P	2.05
Q	0.1±0.1
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	2.45 MAX.

P80G-80-1C-3

NOTE

Each lead centerline is located within 0.15 mm of its true position (T.P.) at maximum material condition.

Plastic Lead Carrier Chip



PIN	PKG CODE	P	S1	S2	W	L	L1	L2
20	FN	1.27	7.90	7.90	0.75	2.0	1.2	0.8
28	FN	1.27	10.45	10.45	0.75	2.0	1.2	0.8
44	FN	1.27	15.50	15.50	0.75	2.0	1.2	0.8
68	FN	1.27	23.15	23.15	0.75	2.0	1.2	0.8
84	FN	1.27	28.20	28.20	0.75	2.0	1.2	0.8

NOTE:

1) All Dimensions In Millimeters (mm)

2) Publication IPC-SM-782 is recommended for alternate designs