

# **AT91SAM9261-EK Evaluation Board**

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## **User Guide**





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# Section 1

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## Overview

- 
- 1.1 Scope** The AT91SAM9261-EK evaluation kit is an effective platform for evaluating chip performance and developing code for applications based on the AT91SAM9261.
- This guide is a description of the hardware included in the AT91SAM9261-EK evaluation kit. Software files are available on the DVD-ROM included in the kit and described in “Deliverables” below.
- 
- 1.2 Deliverables** The AT91SAM9261-EK package contains the following items:
- an AT91SAM9261-EK board
  - one A/B-type USB cable
  - one serial RS232 cable
  - one RJ45 crossed Ethernet cable
  - one DataFlash<sup>®</sup> card
  - universal input AC/DC power supply with US and EU plug adapter
  - one DVD-ROM containing summary and full datasheets, datasheets with electrical and mechanical characteristics, application notes and getting started documents for all development boards and AT91 microcontrollers. An AT91 software package with C and assembly listings is also provided. This allows the user to begin evaluating the AT91 ARM<sup>®</sup> Thumb<sup>®</sup> 32-bit microcontroller quickly.
- 
- 1.3 The AT91SAM9261-EK Evaluation Board** The board is equipped with an AT91SAM9261 (217-ball LFBGA package) together with the following:
- 64 Mbytes of SDRAM memory
  - 256 Mbytes of NAND Flash memory
  - one Atmel 32 Mbit serial DataFlash (AT45DB321C-CNC)
  - one USB device port interface
  - two USB host port interfaces
  - one DBGU serial communication port

## Overview

- JTAG/ICE debug interface
- one Ethernet 100-base TX with three status LEDs
- one Atmel AT73C213 Audio DAC
- one 3.5" 1/4 VGA TFT LCD Module with TouchScreen and backlight
- one Power LED and two general-purpose LEDs
- four user input pushbuttons
- one wakeup input pushbutton
- one reset pushbutton
- one DataFlash SD/MMC card slot
- two expansion footprint connectors (solder side)
- one Lithium Coin Cell Battery Retainer for 12 mm cell size
- dual pitch prototyping area



## Section 2

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# Setting Up the AT91SAM9261-EK Evaluation Board

- 
- 2.1 Electrostatic Warning** The AT91SAM9261-EK evaluation board is shipped in a protective anti-static package. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.
- 
- 2.2 Requirements** In order to set up the AT91SAM9261-EK evaluation board, the following items are required:
- the AT91SAM9261-EK evaluation board itself
  - AC/DC power adapter (5V at 2A), 2.1 mm by 5.5 mm

## 2.3 Layout

Figure 2-1. AT91SAM9261-EK Layout - Top View

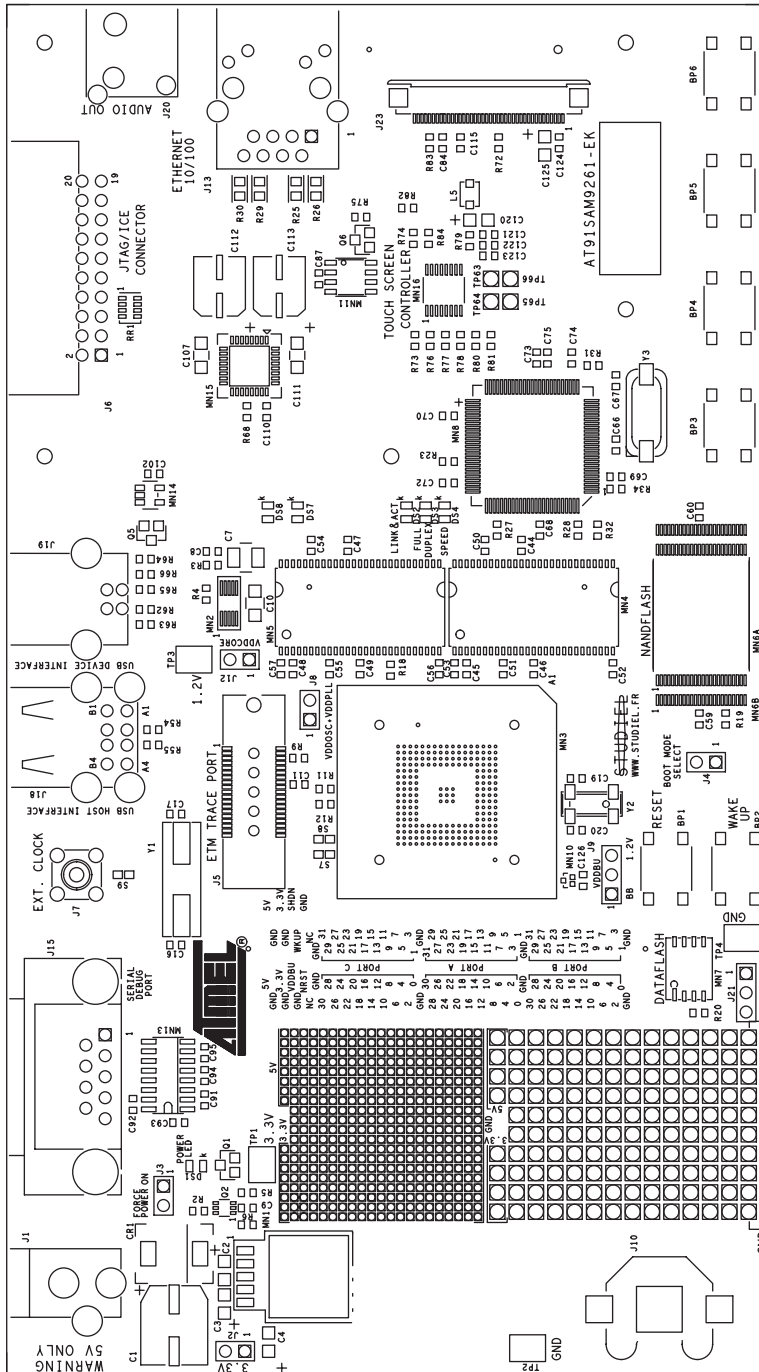
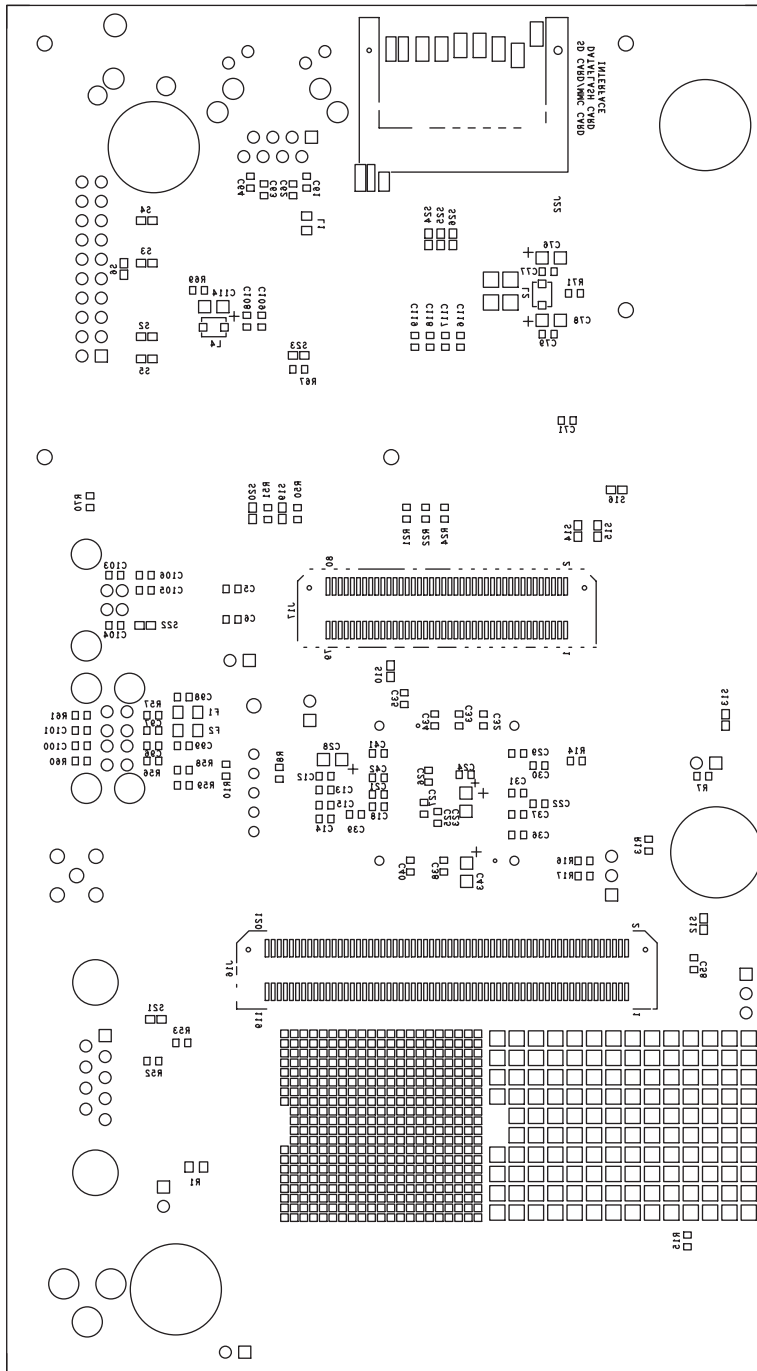




Figure 2-2. AT91SAM9261-EK Layout - Bottom View



**2.4 Powering Up the Board** AT91SAM9261-EK requires 5V DC ( $\pm 5\%$ ). DC power is supplied to the board via the 2.1 mm by 5.5 mm socket (J1). The coaxial power plug center pin is positive polarity .

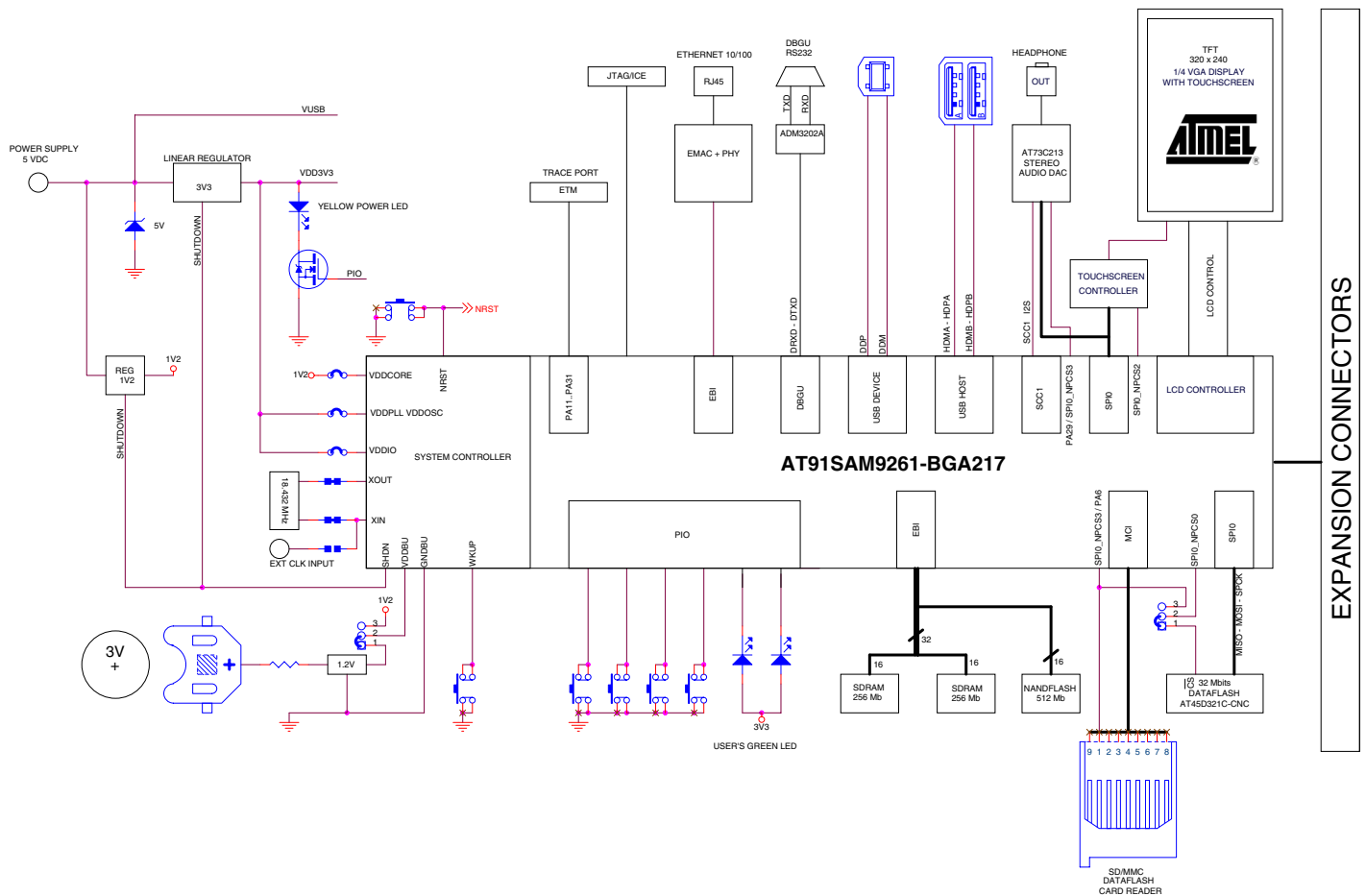
**2.5 Backup Power Supply** The user has the possibility to add a battery (3V Lithium Battery CR1225 or equivalent) in order to permanently power the backup part of the device. In this case, J9 configuration must be set in position 1, 2.

Refer to Table 4-1, "Configuration Jumpers and Straps".

**2.6 Getting Started** The AT91SAM9261-EK evaluation board is delivered with a DVD-ROM containing all necessary information and step-by-step procedures for working with the most common development tool chains. Please refer to this DVD-ROM, or to the AT91 web site, <http://www.atmel.com/products/AT91/>, for the most up-to-date information on getting started with the AT91SAM9261-EK.

**2.7 AT91SAM9261-EK Block Diagram**

Figure 2-3. Block Diagram





## Section 3

# Board Description

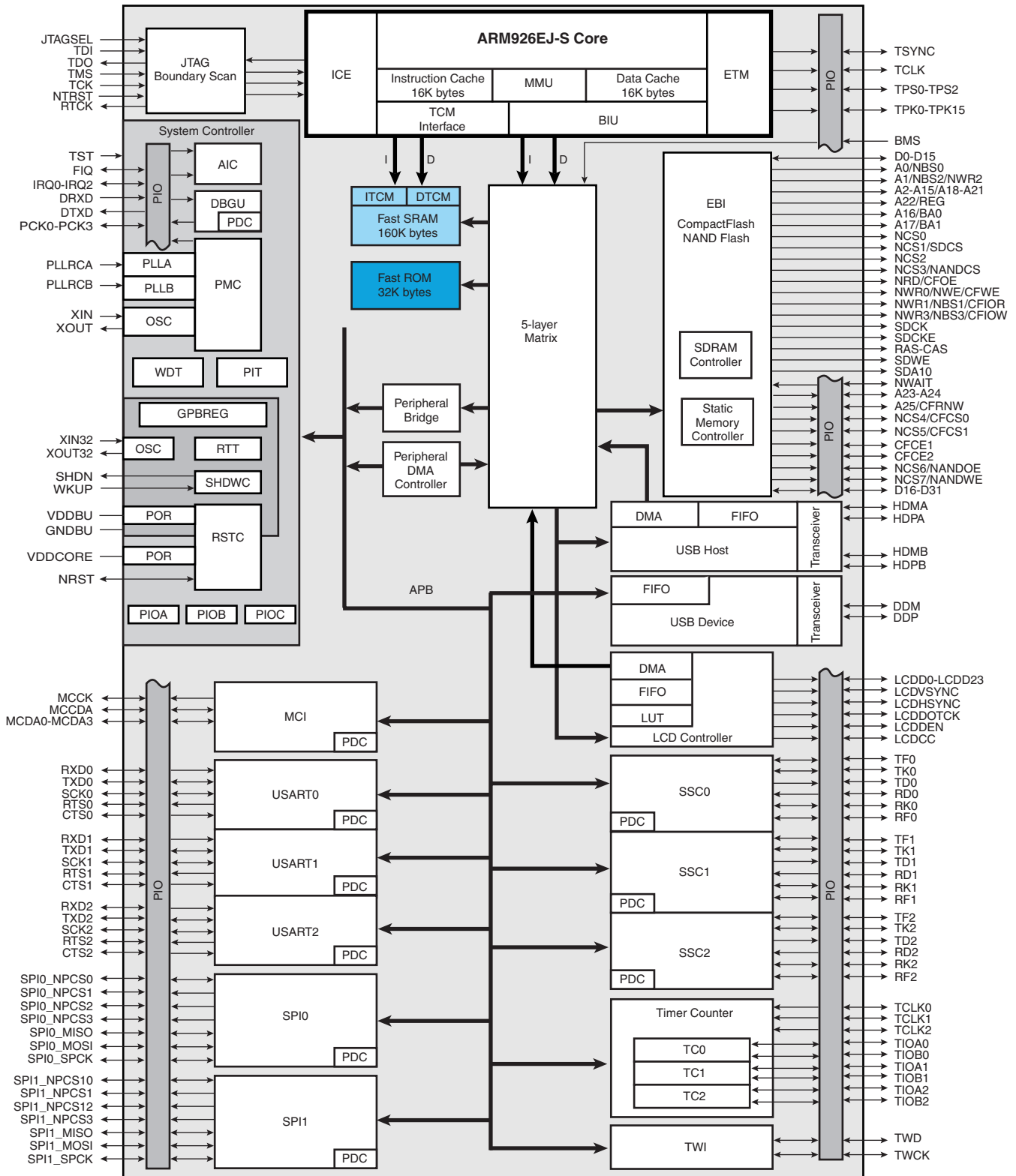
- 3.1 AT91SAM9261 Microcontroller**
- Incorporates the ARM926EJ-S™ ARM® Thumb® Processor
    - DSP Instruction Extensions
    - ARM Jazelle® Technology for Java™ Acceleration
    - 16-KByte Data Cache, 16-KByte Instruction Cache, Write Buffer
    - 200 MIPS at 180 MHz
    - Memory Management Unit
    - EmbeddedICE™ In-circuit Emulation, Debug Communication Channel Support
    - Mid-level implementation Embedded Trace Macrocell™
  - Additional Embedded Memories
    - 32K Bytes of Internal ROM, Single-cycle Access at Maximum Bus Speed
    - 160K Bytes of Internal SRAM, Single-cycle Access at Maximum Processor or Bus Speed
  - External Bus Interface (EBI)
    - Supports SDRAM, Static Memory, NAND Flash and CompactFlash®
  - LCD Controller
    - Supports Passive or Active Displays
    - Up to 16-bits per Pixel in STN Color Mode
    - Up to 16M Colors in TFT Mode (24-bit per Pixel), Resolution up to 2048 x 2048
  - USB
    - USB 2.0 Full Speed (12 Mbits per second) Host Double Port
      - Dual On-chip Transceivers
      - Integrated FIFOs and Dedicated DMA Channels
    - USB 2.0 Full Speed (12 Mbits per second) Device Port
      - On-chip Transceiver, 2-Kbyte Configurable Integrated FIFOs
  - Bus Matrix
    - Handles Five Masters and Five Slaves
    - Boot Mode Select Option

- Remap Command
- Fully Featured System Controller (SYSC) for Efficient System Management, including
  - Reset Controller, Shutdown Controller, Four 32-bit Battery Backup Registers for a Total of 16 Bytes
  - Clock Generator and Power Management Controller
  - Advanced Interrupt Controller and Debug Unit
  - Periodic Interval Timer, Watchdog Timer and Real-time Timer
  - Three 32-bit PIO Controllers
- Reset Controller (RSTC)
  - Based on Power-on Reset Cells, Reset Source Identification and Reset Output Control
- Shutdown Controller (SHDWC)
  - Programmable Shutdown Pin Control and Wake-up Circuitry
- Clock Generator (CKGR)
  - 32.768 kHz Low-power Oscillator on Battery Backup Power Supply, Providing a Permanent Slow Clock
  - 3 to 20 MHz On-chip Oscillator and two PLLs
- Power Management Controller (PMC)
  - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
  - Four Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Three External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - 2-wire USART and Support for Debug Communication Channel, Programmable ICE Access Prevention
- Periodic Interval Timer (PIT)
  - 20-bit Interval Timer plus 12-bit Interval Counter
- Watchdog Timer (WDT)
  - Key Protected, Programmable Only Once, Windowed 12-bit Counter, Running at Slow Clock
- Real-Time Timer (RTT)
  - 32-bit Free-running Backup Counter Running at Slow Clock
- Three 32-bit Parallel Input/Output Controllers (PIO) PIOA, PIOB and PIOC
  - 96 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
- Nineteen Peripheral DMA (PDC) Channels

- Multimedia Card Interface (MCI)
  - Compliant with Multimedia Cards and SDCards
  - Automatic Protocol Control and Fast Automatic Data Transfers with PDC, MMC and SDCard Compliant
- Three Synchronous Serial Controllers (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I<sup>2</sup>S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Three Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA Infrared Modulation/Demodulation
  - Support for ISO7816 T0/T1 Smart Card, Hardware and Software Handshaking, RS485 Support
- Two Master/Slave Serial Peripheral Interface (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- One Three-channel 16-bit Timer/Counters (TC)
  - Three External Clock Inputs, Two multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- Two-wire Interface (TWI)
  - Master Mode Support, All Two-wire Atmel EEPROMs Supported
- IEEE 1149.1 JTAG Boundary Scan on All Digital Pins
- Required Power Supplies:
  - 1.08V to 1.32V for VDDCORE and VDDBU
  - 2.7V to 3.6V for VDDOSC and for VDDPLL
  - 2.7V to 3.6V for VDDIOP (Peripheral I/Os) and for VDDIOM (Memory I/Os)
- Available in a 217-ball LFBGA RoHS-compliant Package

### 3.2 AT91SAM9261 Block Diagram

Figure 3-1. Block Diagram



- 
- 3.3 Memory**
- 32 Kbytes of Internal ROM
  - 160 Kbytes of Internal High-speed SRAM
  - Atmel 32 Mbit serial DataFlash
  - 64 Mbytes of SDRAM memory
  - 256 Mbytes of NAND Flash memory
- 
- 3.4 Clock Circuitry**
- 18.432 MHz standard crystal for the embedded oscillator
  - 32.768 kHz standard crystal for the slow clock oscillator
- 
- 3.5 Reset Circuitry**
- Internal reset controller with a bi-directional reset pin
  - External reset push button
- 
- 3.6 Shutdown Controller**
- Programmable shutdown and Wake-Up
  - Wake-up push button
- 
- 3.7 Power Supply Circuitry**
- For dynamic power consumption, the AT91SAM9261 consumes a maximum of 50 mA on VDDCORE at maximum speed in typical conditions (1.2V, 25°C), processor running full-performance algorithm
  - On-board 1.2V high efficiency step-down charge pump regulator with shutdown control
  - On-board 3.3V linear regulator with shutdown control
- 
- 3.8 Remote Communication**
- One Serial interface (DBGU COM Port) via RS-232 DB9 male socket
  - USB V2.0 Full-speed Compliant, 12 Mbits per second (UDP)
  - Two USB Host port V2.0 Full-speed Compliant, 12 Mbits per second (UHP)
  - One Ethernet 100-base TX with three status LEDs
- 
- 3.9 Audio Stereo Interface**
- One Atmel stereo audio DAC AT73C213
  - One 32 Ohm/20 mW Stereo Headset output (J20) with Master Volume and Mute Controls
- 
- 3.10 User Interface**
- Four user input pushbuttons
  - Two user green LEDs
  - One yellow power LED (can be also software controlled)

- One ¼ VGA display LCD with Touchscreen and white LED backlight

- 
- 3.11 Debug Interface**
- 20-pin JTAG/ICE interface connector
  - DBGU COM Port

- 
- 3.12 Expansion Slot**
- One DataFlash, SD/MMC card slot
  - All I/Os of the AT91SAM9261 are routed to peripheral extension footprint connectors (J16 and J17). This allows the developer to check the integrity of the components and to extend the features of the board by adding external hardware components or boards.





## Section 4

# Configuration Straps

### 4.1 Configuration Straps

Table 4-1 gives details on configuration straps on the AT91SAM9261-EK evaluation board and their default settings.

**Table 4-1.** Configuration Jumpers and Straps

Designation	Default Setting	Feature
J2	Closed	3.3V Jumper <sup>(1)</sup> This jumper footprint is provided for 3.3V power consumption measurement use. By default, it is closed. To use this feature, the user has to open the strap by cutting it before soldering a jumper.
J3	Closed	Forces power on. To use the software shutdown control, J3 must be opened.
J4	Opened	Enables Boot on the internal ROM
	Closed	Enables Boot on the NCS0
J8	Closed	VDDPLL Jumper <sup>(1)</sup>
J9	2-3	VDDBU Jumper select <sup>(1)</sup> 1-2 : Lithium 3V Battery 2-3 : 1.2V from VDDCORE
J12	Closed	VDDCORE Jumper <sup>(1)</sup>
J21	1-2	NPCS0 select 1-2 : AT45DB321C (MN7) 2-3 : Dataflash card interface (J22). <b>Warning: In this case NPCS03 must be configured as input.</b>
S2	Opened	Disables the ICE NTRST input
S3	Closed	Enables the ICE RTCK return. S6 must be opened
S4	Closed	Enables the ICE NRST input
S5	Opened	Selects ICE mode or JTAG mode (Closed)
S6	Opened	Disables TCK <-> RTCK local loop. If S6 is closed, S3 must be opened.

**Table 4-1.** Configuration Jumpers and Straps

Designation	Default Setting	Feature
S7-S8 S9	Closed Opened	Enables the use of 18.432 MHz crystal. If external clock used, S7-S8 must be opened and S9 closed.
S10	Closed	Enables the use of SDRAM (NCS1_SDCS)
S12	Opened	Disables Serial DataFlash write protect.
S13	Closed	Disables NAND FLASH write protect.
S14	Closed	Enables the use of interrupt ETHERNET MAC (PC11_FIQ).
S15	Closed	Enables the use of ETHERNET MAC (NCS2).
S16	Opened	Disables the use of NWAIT ETHERNET MAC signal (PC2_NWAIT)
S19	Closed	Enables the use of the User LED DS7 (PA14)
S20	Closed	Enables the use of the User LED DS8 (PA13)
S21	Closed	Enables the use of the DBGU RXD signal (PA9)
S22	Closed	Enables the use of the USB CNX detection (PB29)
S23	Closed	Enables the use of AUDIO DAC INTERFACE (NPCS03)
S24	Closed	Enables the use of TOUCH SCEEN CONTROLLER (NPCS02)
S25	Closed	Enables the use of TOUCH SCEEN CONTROLLER BUSY signal (PA11)
S26	Closed	Enables the use of TOUCH SCEEN CONTROLLER PENIRQ (PC2_IRQ0)
TP1	N.A	3.3V Test point.
TP2	N.A	GND Test point.
TP3	N.A	1.2V Test point.
TP4	N.A	GND Test point.
TP63	N.A	0 to 3.3V analog user's input
TP64	N.A	0 to 3.3V analog user's input
TP65	N.A	AGND of TP63
TP66	N.A	AGND of TP64

Note: 1. These jumpers are provided for measuring power consumption. By default, they are closed. To use this feature, the user has to open the strap and insert an anmeter.



## Section 5

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# Schematics

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### 5.1 Schematics

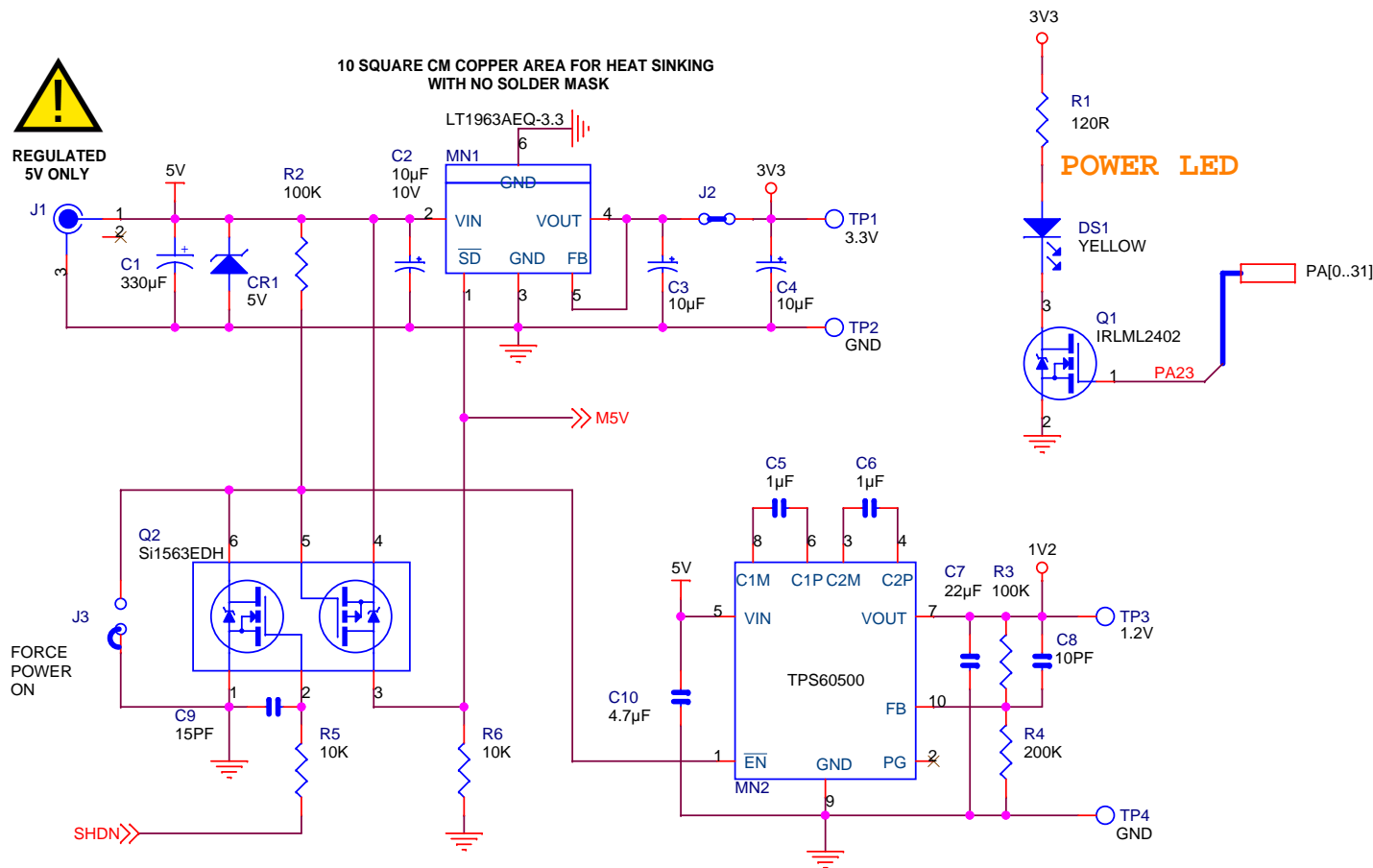
This section contains the following schematics:

- Power Supply and Audio
- AT91SAM9261
- SDRAM and NAND Flash
- Ethernet
- LCD and User Interface
- Serial and I/O Expansion

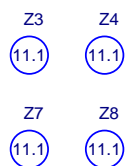


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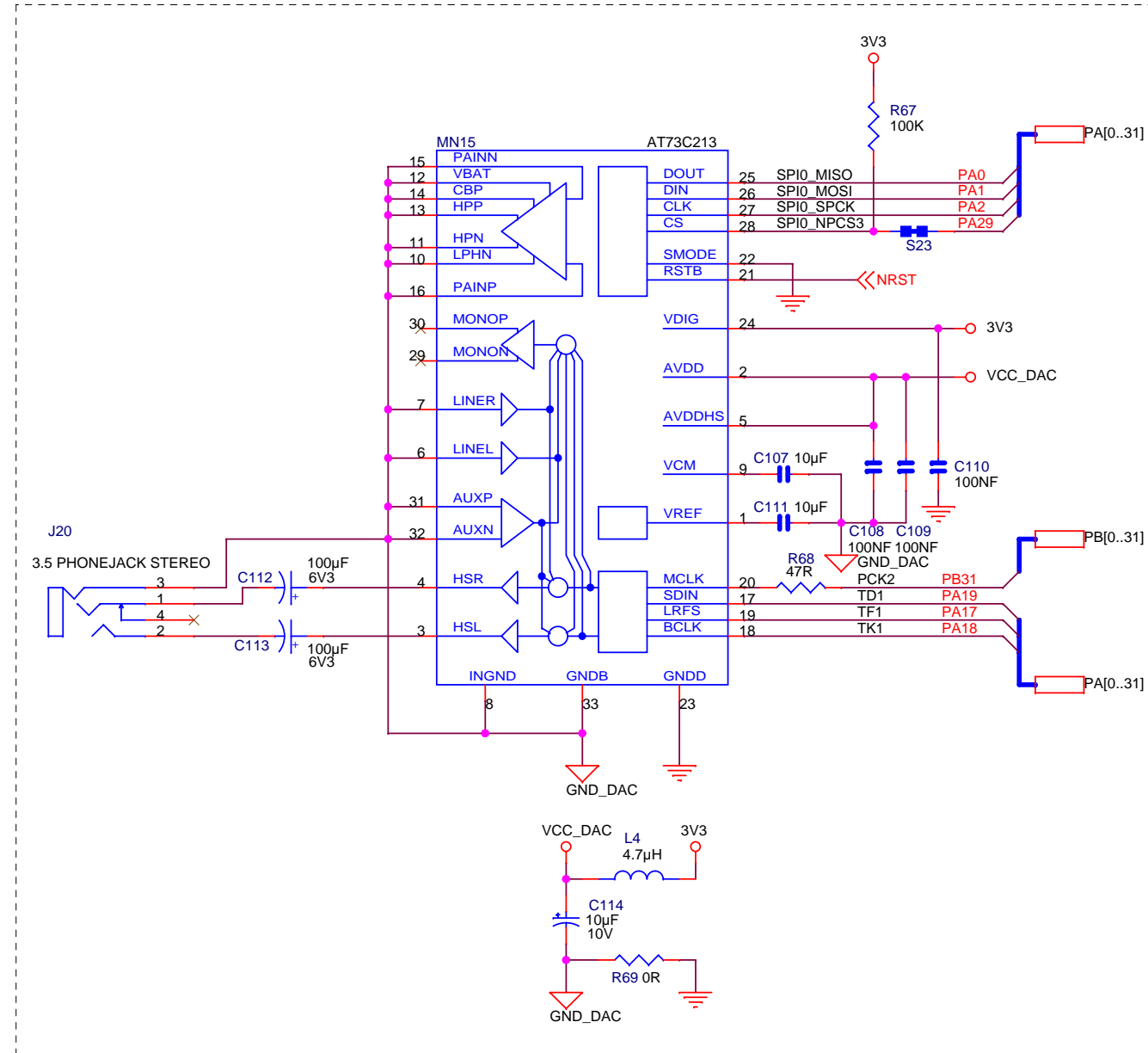
10 SQUARE CM COPPER AREA FOR HEAT SINKING WITH NO SOLDER MASK



ADHESIVE FEET



AUDIO DAC INTERFACE

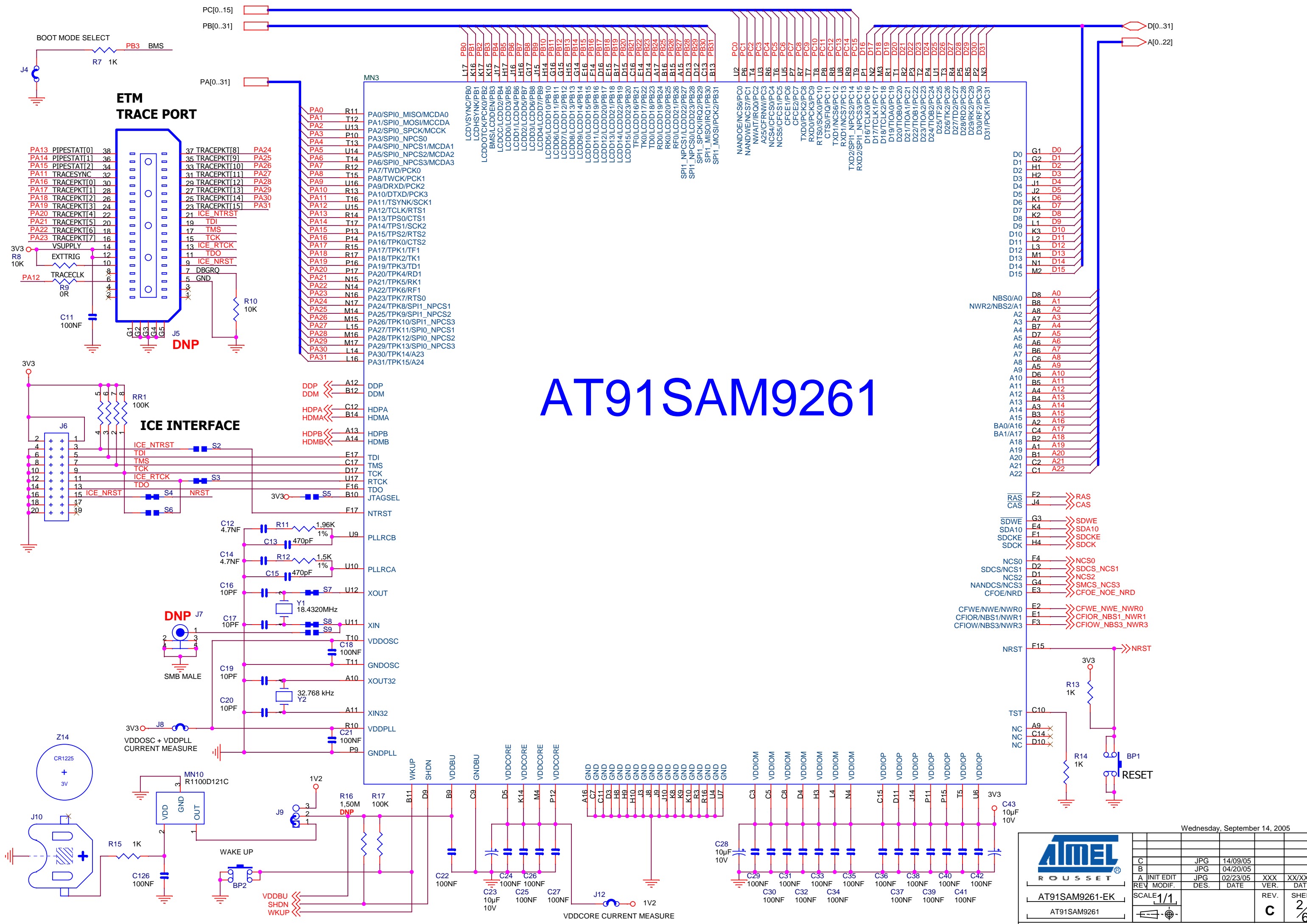


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# AT91SAM9261

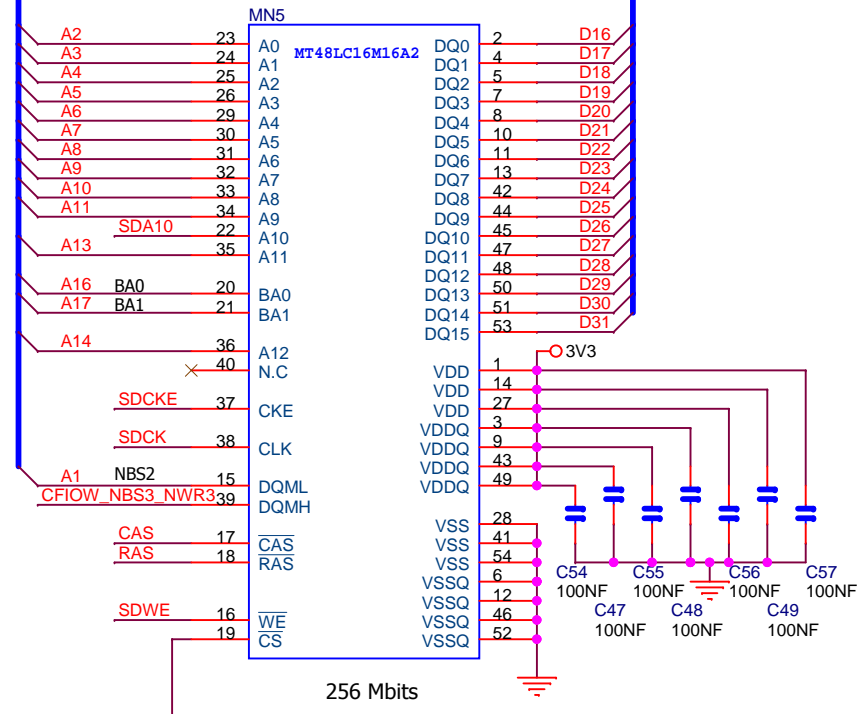
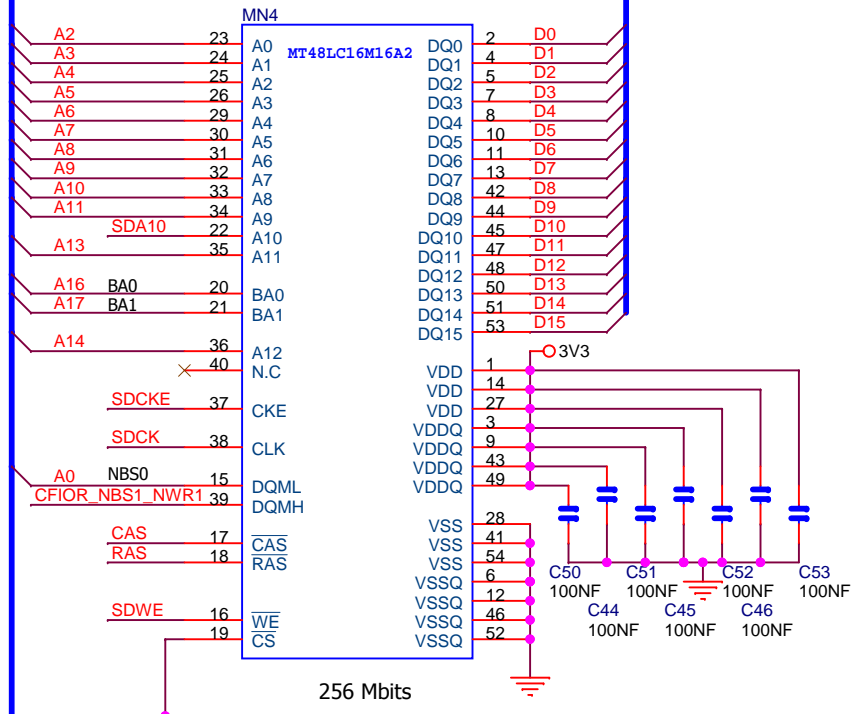
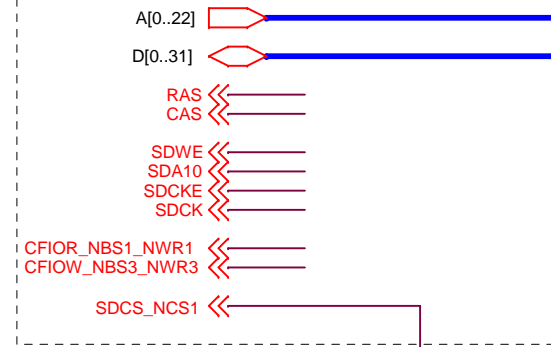


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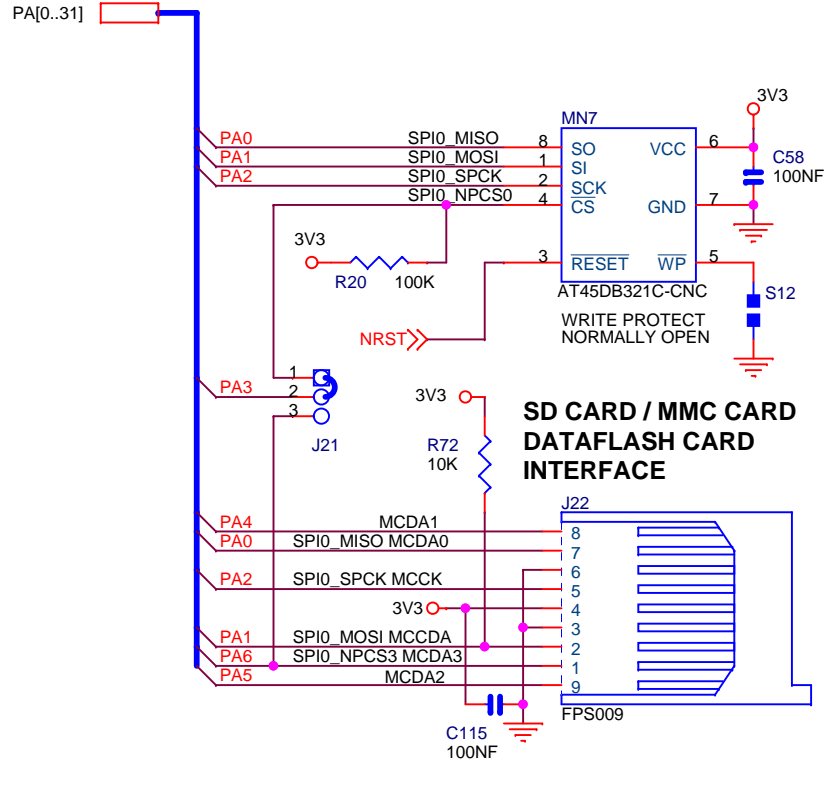
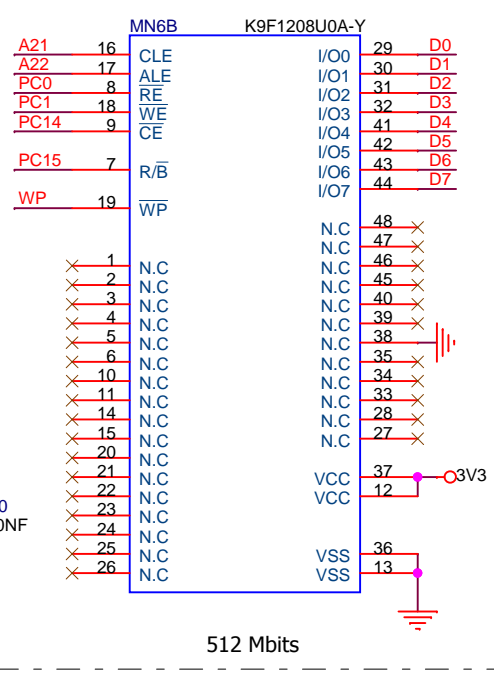
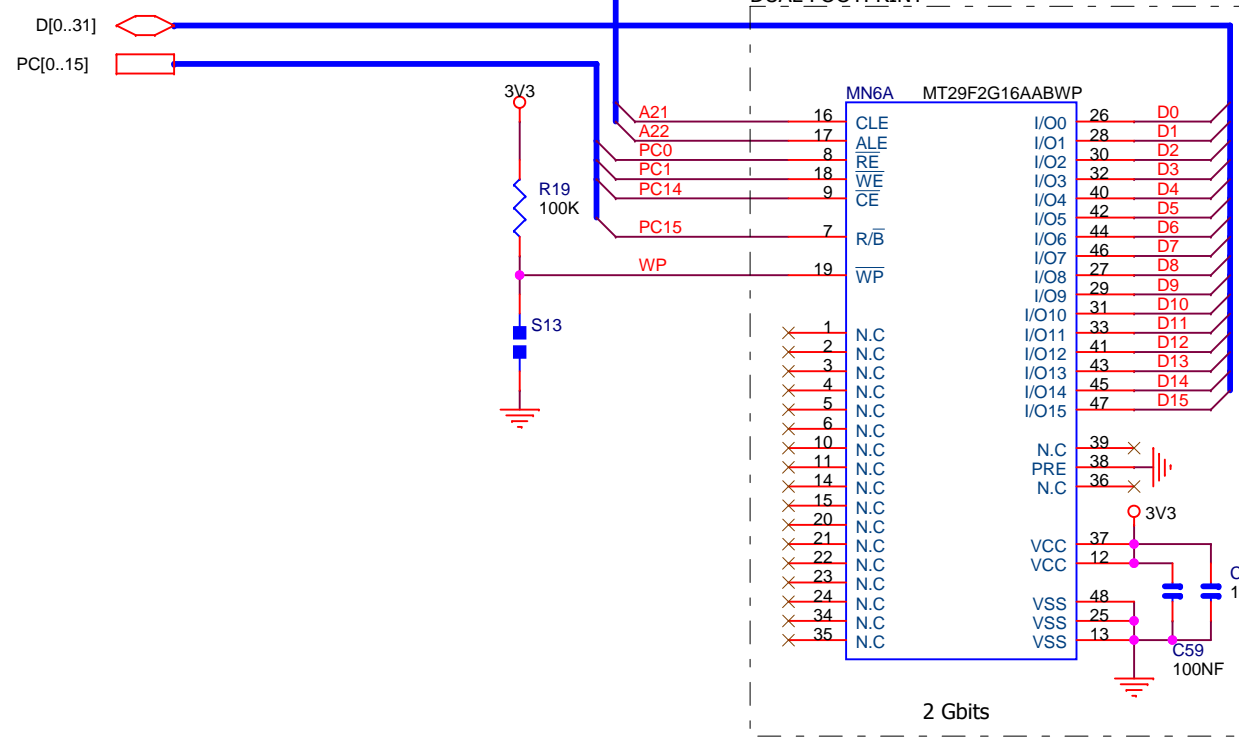
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# EBI SDRAM INTERFACE



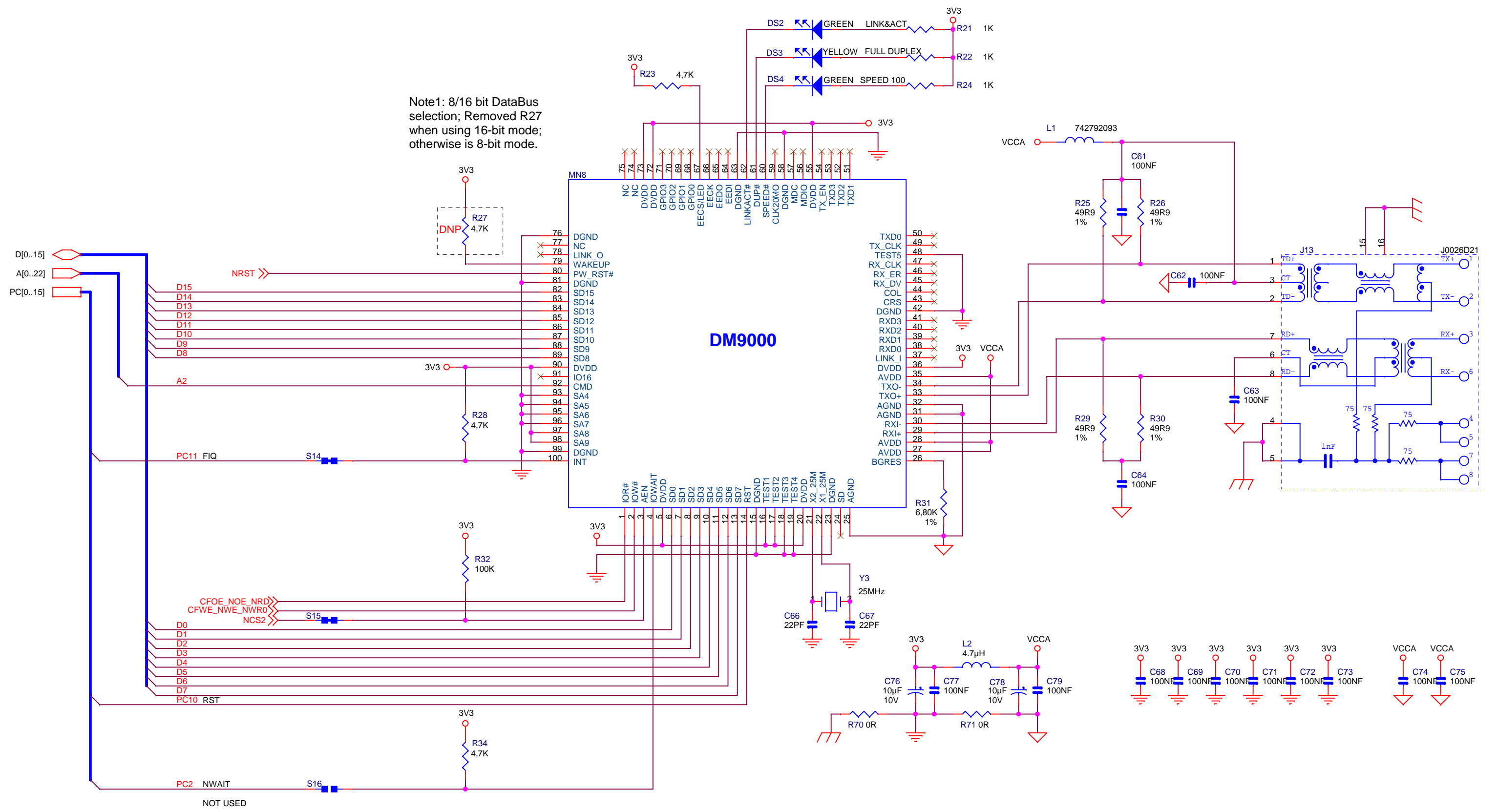
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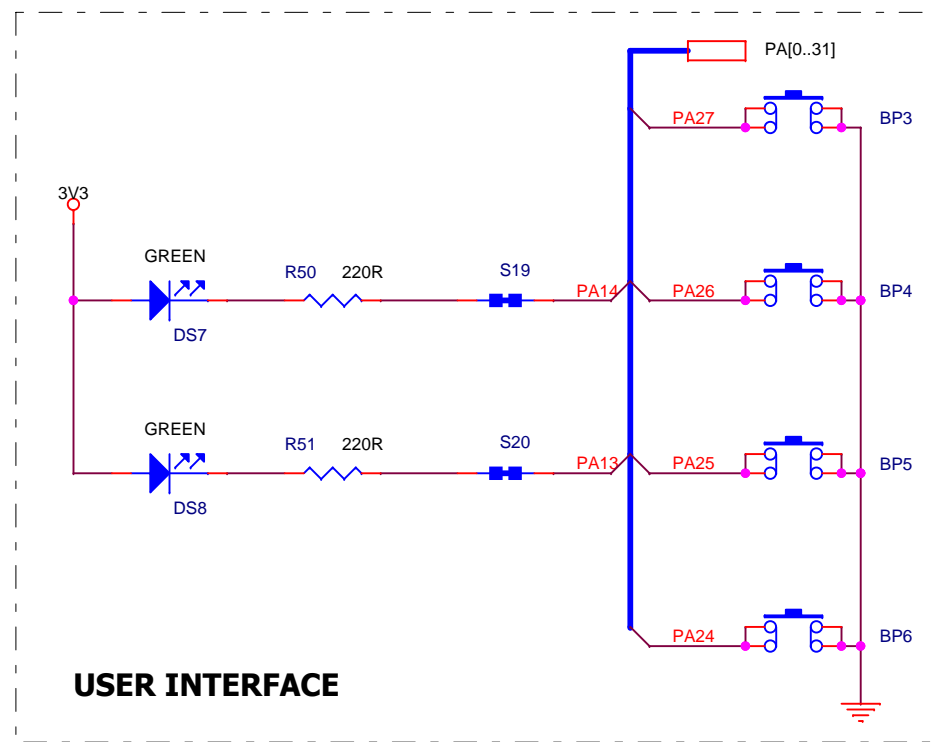
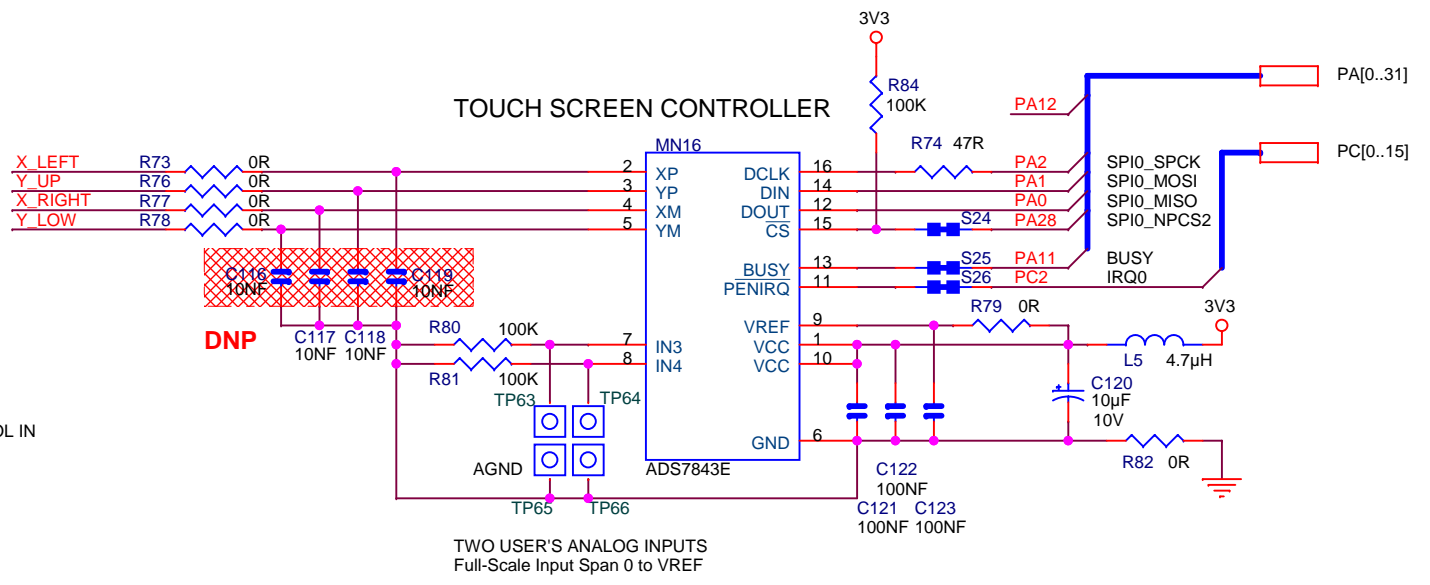
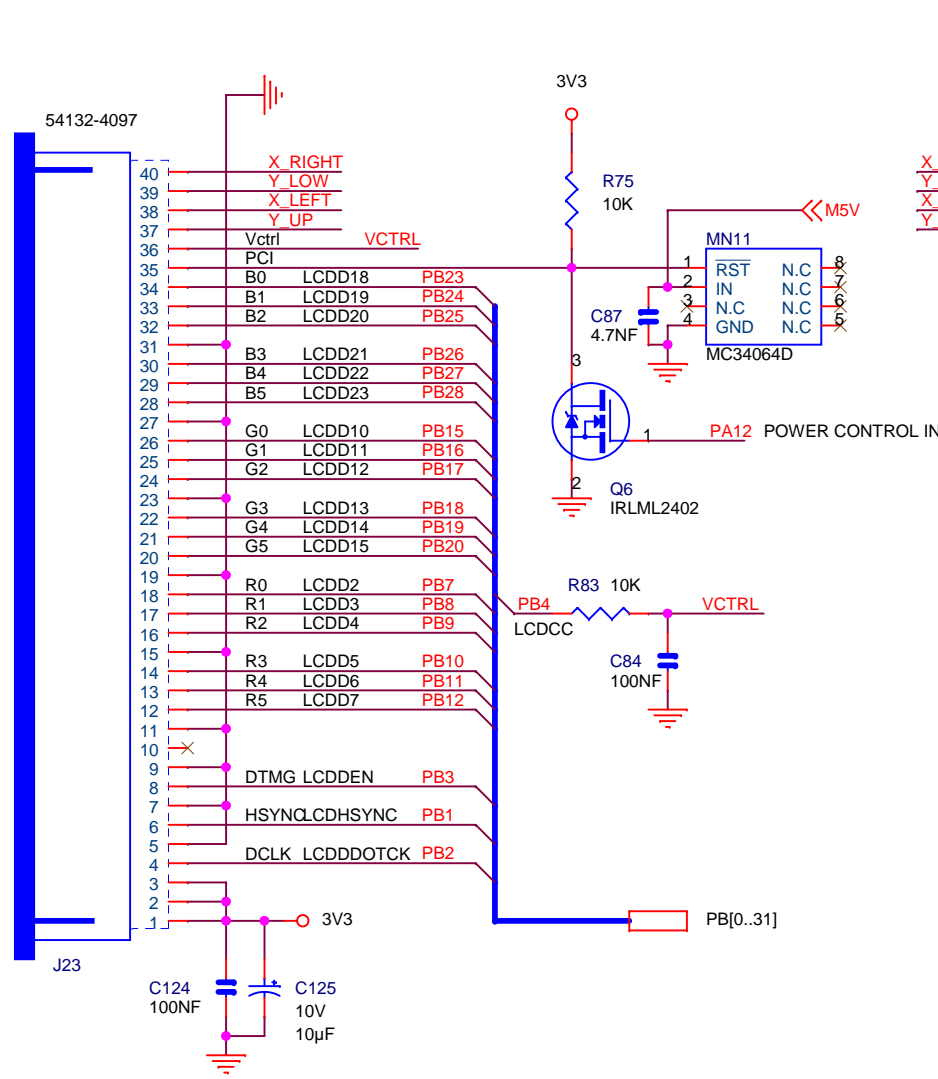
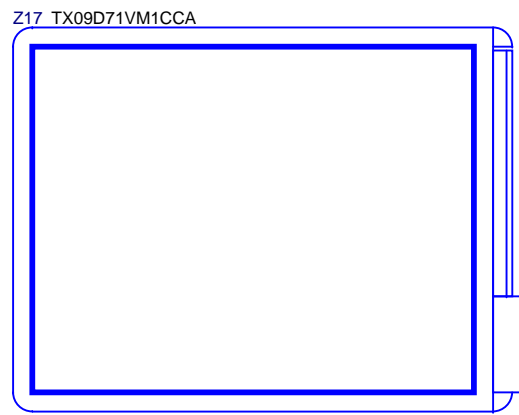
Note1: 8/16 bit DataBus selection; Removed R27 when using 16-bit mode; otherwise is 8-bit mode.

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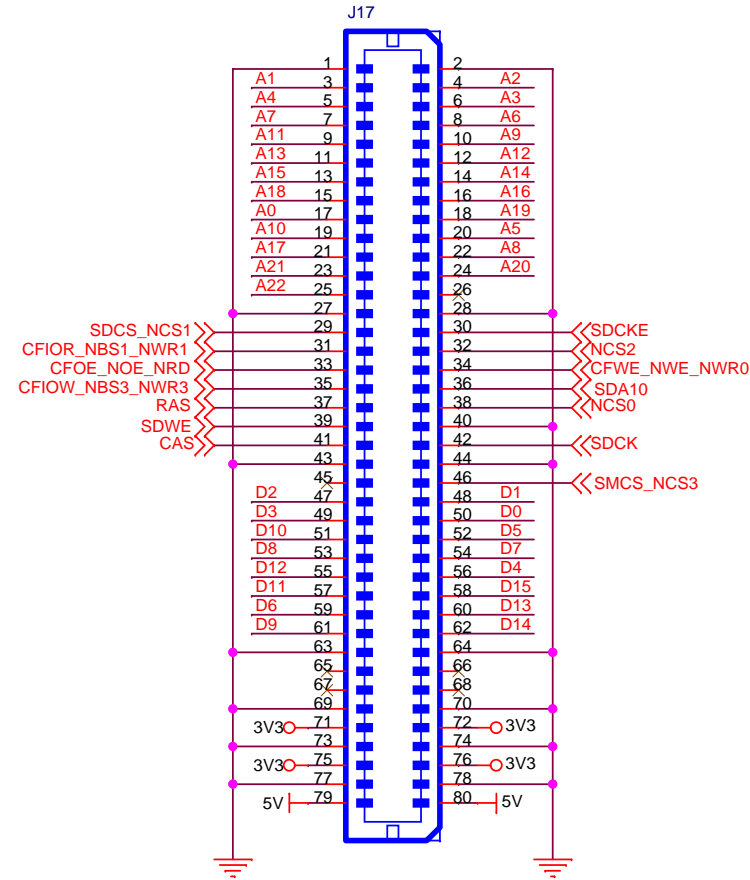
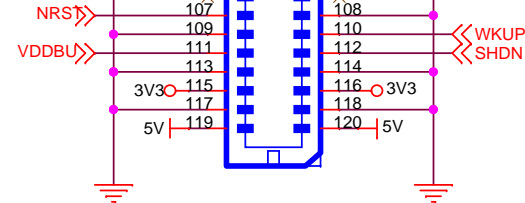
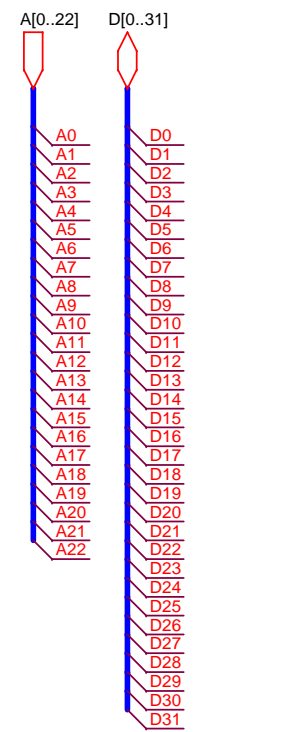
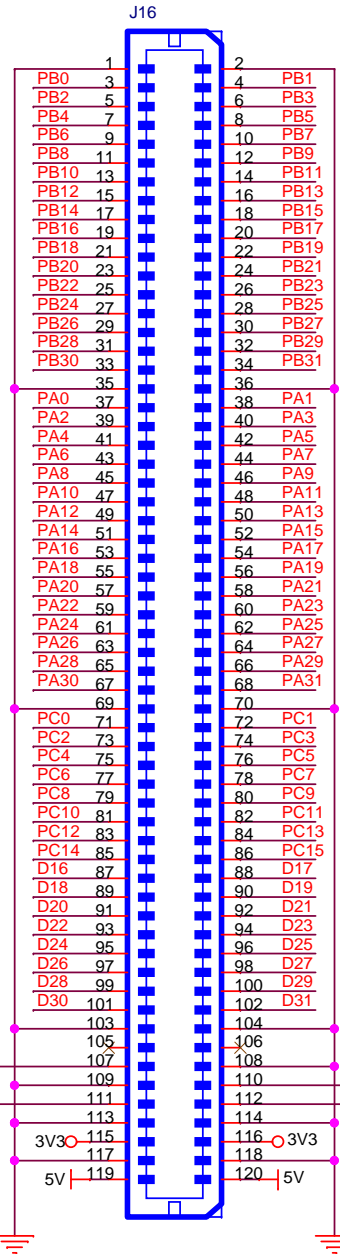
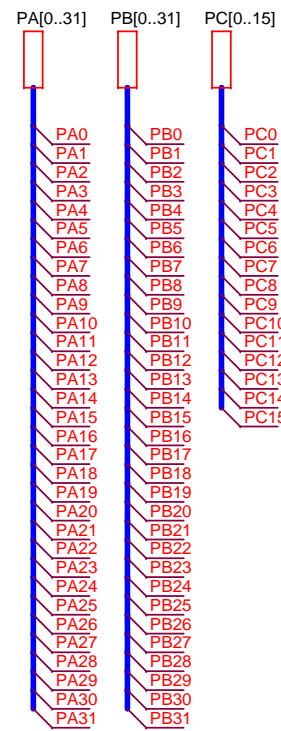
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A	INIT EDIT	JPG	02/23/05	XXX	XX/XX/05
REV	MODIF.	DES.	DATE	VER.	DATE
AT91SAM9261-EK		SCALE 1/1		REV. C	SHEET 5/6
LCD & USER'S INTERFACE					

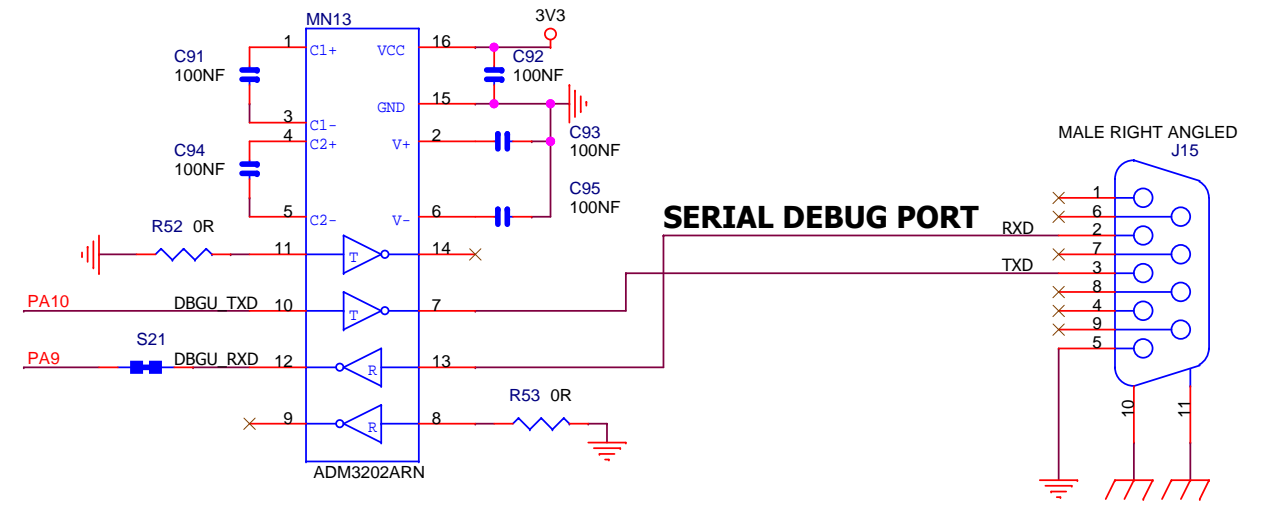
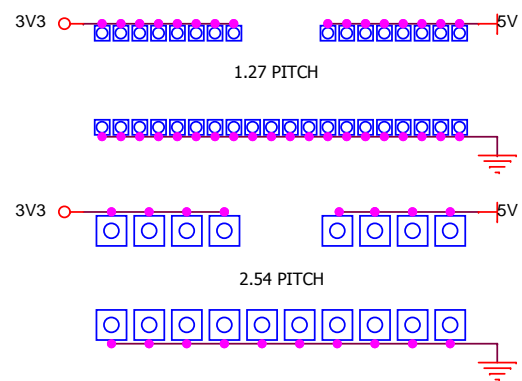
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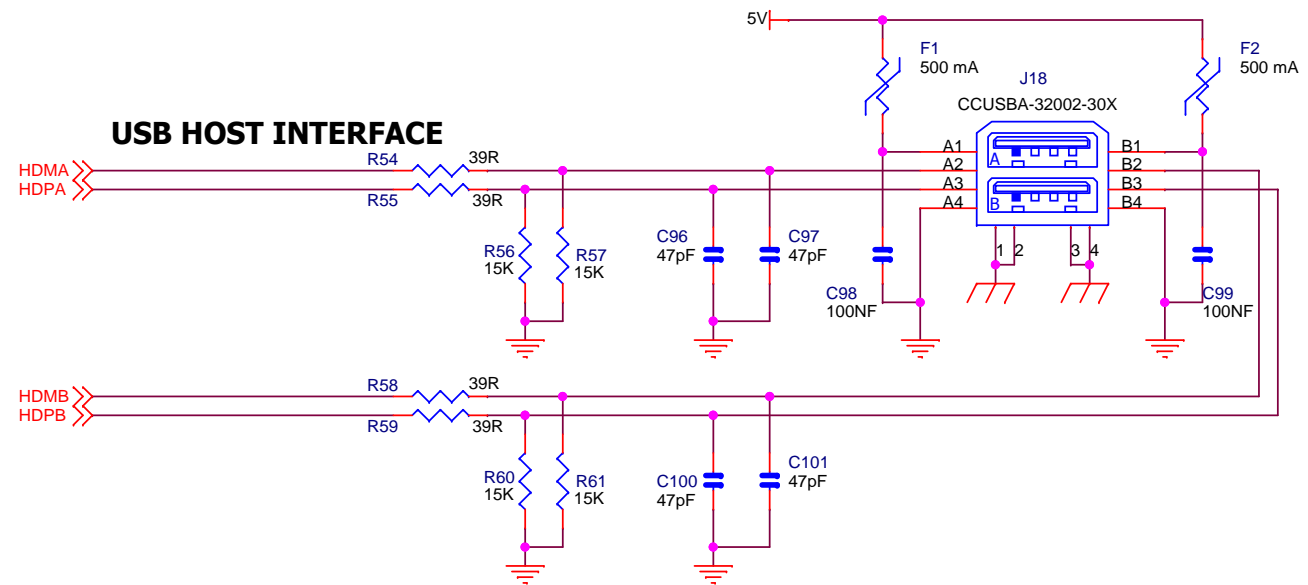
# EXPANSION CONNECTORS



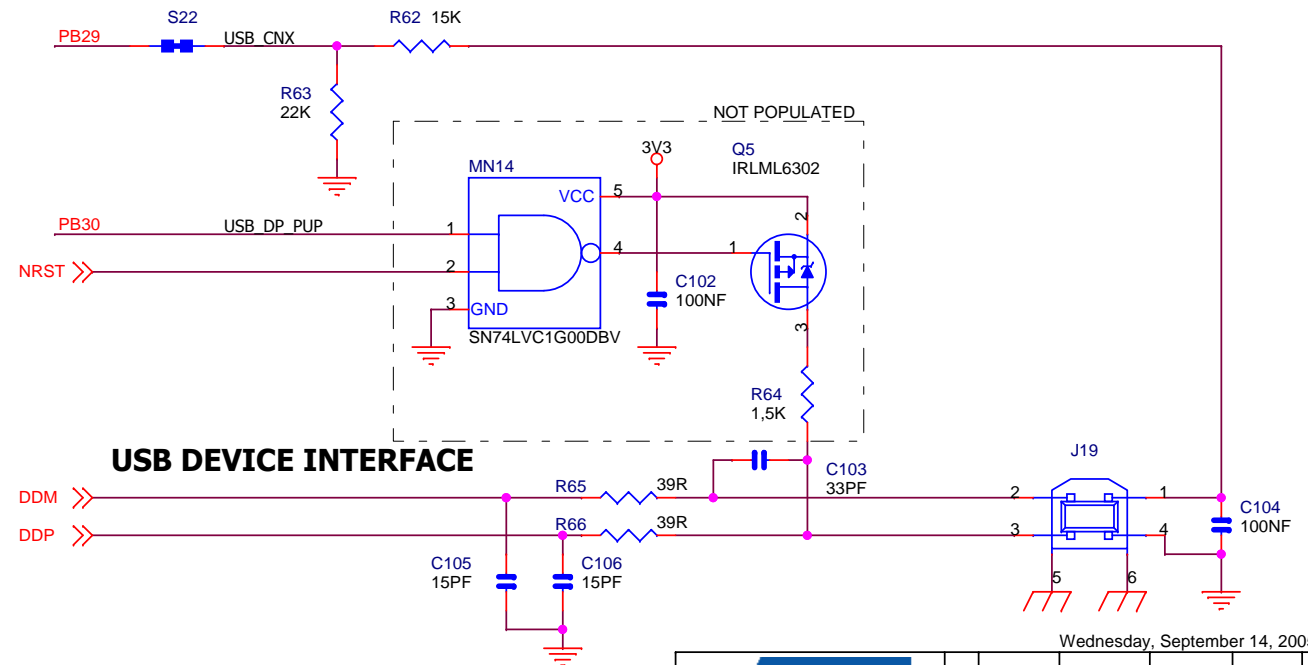
# USER'S GRID AREA



# USB HOST INTERFACE



# USB DEVICE INTERFACE



Wednesday, September 14, 2005

<b>ATMEL</b>					
ROUSSET					
AT91SAM9261-EK					
SERIAL & I/O EXPANSION					
REV	MODIF.	DES.	DATE	VER.	DATE
C		JPG	14/09/05		
B		JPG	04/20/05		
A	INIT EDIT	JPG	02/23/05	XXX	XX/XX/05
SCALE 1/1				REV.	SHEET
				C	6/6



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