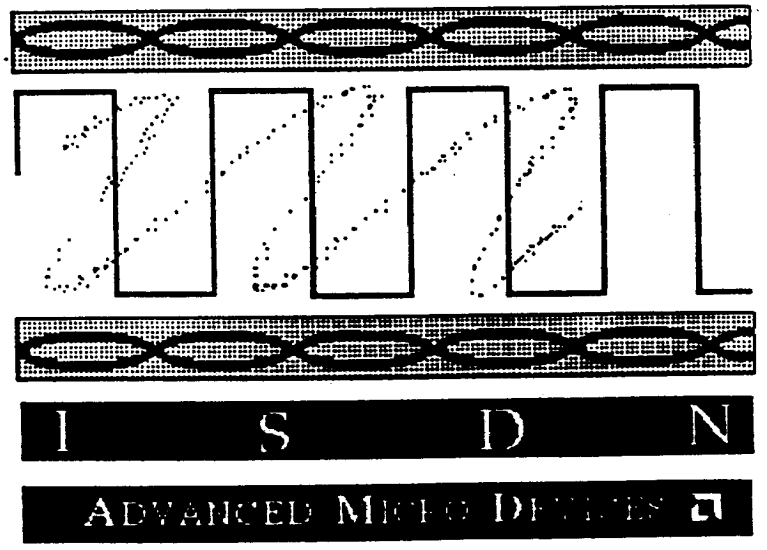
Extended PCM Interface Controller (EPIC™)

Data Sheet

Revision TM 8/89



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Am2055

Advanced Micro Devices

0. GENERAL

Upstream: Direction from the subscriber to the PCM highways in the exchange.

Downstream: Direction from the PCM highways to the subscribers.

Time Slot: Defined period of time in the PCM, IOM or SLD frame consisting of 8 bits. Time slots are allocated to the frames in such away that the time slot boundaries coincide with the frame boundaries. The time slots do not overlap. The lowest time slot number is 0. This time slot is the first in the frame.

Sub Time Slot: A quarter or half a time slot. These are allocated to the time slots in such a way that time slot and subtime slot boundaries match. The subtime slots are non overlapping.

Channel: Sequence of bits which is exchanged between the subsriber, the exchange equipment and/or the microprocessor. It occupies a defined number of bits at a defined position within a frame as long as a connection pervails. Both time slots and subtime slots are channels and hence a channel may offer a bandwidth of 16, 32 or 64 kbps.

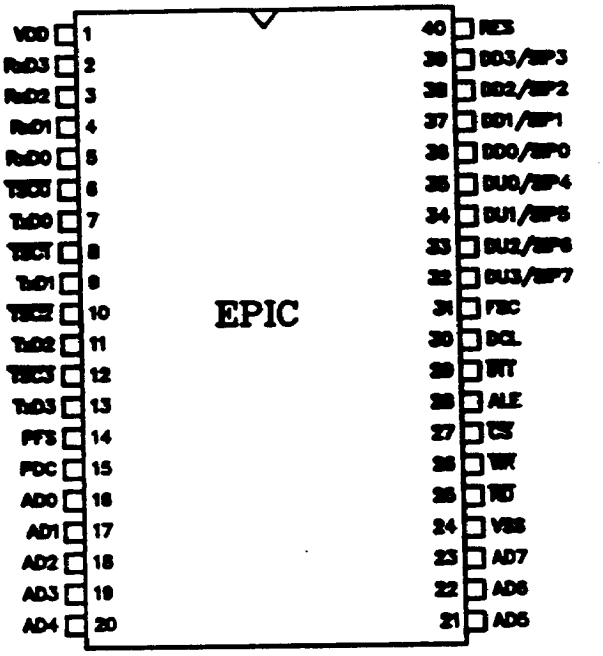
Bit Numbering: The bits in a time slot are numbered 7 (MSB) through 0 (LSB). Bit 7 is the first bit to be transmitted or received, bit 0 the last.

1. Introduction

1.1. Features

- Board Controller for up to 32 ISDN or 64 voice subscribers
- Nonblocking switch for 128 channels (16, 32, or 64 kbps bandwidth)
- Two consecutive 64 kbps channels can be switched as a single 128 kbps channel.
- Timeslot assignment freely programmable for all connected subscribers
- Two serial interfaces (PCM and Configurable)
- Programmable for a wide range of data rates (8 to 8192 kbps)
- Data rates of PCM and configurable interfaces independent from each other (data rate adaption)
- Single and double rate clock selectable
- PCM interface
  - Tristate control signals for external drivers
  - Programmable clock shift
- Configurable interface
  - Configurable for IOM™ compatible devices (4 duplex ports)
  - Configurable for SLD compatible devices (8 bidirectional I/O ports)
  - Configurable for PCM applications
- Standard µP interface with multiplexed address/data bus or seperate address and data buses (PLCC 44)
- Handling of layer 1 functions
  - Change detection and last-look logic for C/I (IOM configuration) or feature control (SLD configuration) channels
  - Buffered monitor (IOM configuration) or signaling channel (SLD configuration)
- Comfortable µP access to two selected channels
- 40 pin Dual In Line or 44 pin PLCC package
- Advanced low power CMOS technology

1.2. Pin Configuration



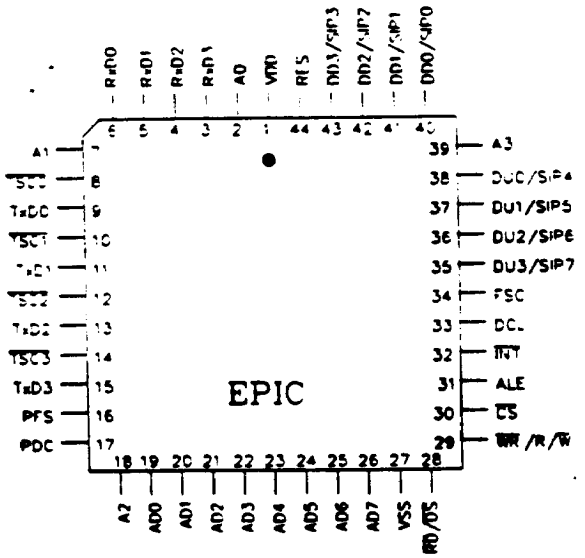


Fig. 1.1: Pin Configurations (top view)

1.3. General Device Overview

The Extended PCM Interface Controller EPIC™ (PEB 2055) is a monolithic switching device for the path control of up to 128 channels of 16, 32 or 64 kbps bandwidth. Two consecutive 64 kbps channels may also be handled as a quasi single 128 kbps channel. For these channels the EPIC performs nonblocking space time switching between two serial interfaces, the system and the configurable interface.

Both interfaces can be programmed to operate at different data rates between 8 and 8192 kbps. The system interface consists of up to four duplex ports with a tristate indication signal for each output line. The configurable interface can be selected to incorporate either four duplex or eight bidirectional I/O ports (SLD).

The EPIC can therefore be programmed to communicate either with SLD or with IOM (ISDN oriented modular) compatible devices. In both cases the device handles the layer 1 functions buffering the C/I and monitor channels for IOM compatible devices and the feature control and signaling channels for SLD compatible devices.

Due to its capability to switch channels of different bandwidths, the EPIC can handle up to 32 ISDN subscribers with their 2B + D channel structure in IOM configuration or up to 16 subscribers in SLD configuration. Since its interfaces can operate at different data rates, the EPIC is an ideal device for data rate adaption.

Moreover, the EPIC is one of the fundamental building blocks for networks with either central, decentral or mixed signaling and packet data handling architectures. The other key devices are the IDEC™ (ISDN D-channel Exchange Controller, PEB 2075) and the HSCX (Enhanced High Level Serial communication Controller, SAB 82525).

Applications of the EPIC include communication multiplexers, concentrators, central switches as well as peripheral ISDN and analog line cards.

The EPIC is available in a DIP/DIC 40 or a PLCC 44 package.

The DIP/DIC 40 version is controlled by a standard 8 bit parallel microprocessor interface with a multiplexed address-data bus. In the PLCC 44 package the device may optionally be controlled by seperate address and data buses.

1.4. Pin Definitions and Functions

Symbol	PIN No. DIP	Pin No. PLCC	Typ	Function
			Input (I) Output (O) In/Output (IO) Open Drain (OD)	
VDD	1	1	I	Supply Voltage 5V ± 5%
A0	-	2	I	Address Bus Bit 0: This input interfaces to the system's address bus to select an internal register for a read or write access. This pin is only provided in the PLCC package and only active if a demultiplexed µP interface mode is selected.
RxD3 RxD2 RxD1 RxD0	2 3 4 5	3 4 5 6	I	Receive PCM interface Data: Serial data is received at these lines at standard TTL or CMOS levels.
A1	-	7	I	Address Bus Bit 1: This input interfaces to the system's address bus to select an internal register for a read or write access. This pin is only provided in the PLCC package and only active if a demultiplexed µP interface mode is selected.
$\overline{TSC0}$ $\overline{TSC1}$ $\overline{TSC2}$ $\overline{TSC3}$	6 8 10 12	8 10 12 14	O	Tristate control for the PCM interface. These lines are low when the corresponding TxD outputs are valid.
TxD0 TxD1 TxD2 TxD3	7 9 11 13	9 11 13 15	O	Transmit PCM interface Data: Serial data is sent by these lines at standard TTL or CMOS levels. These pins can be tristated.
PFS	14	16	I	PCM interface frame synchronization pulse.
PDC	15	17	I	PCM interface data clock, single or double rate.

A2	-	18	I	Address Bus Bit 2: This input interfaces to the system's address bus to select an internal register for a read or write access. This pin is only provided in the PLCC package and only active if a demultiplexed µP interface mode is selected.
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	16 17 18 19 20 21 22 23	19 20 21 22 23 24 25 26	I/O	Address Data Bus. If the multiplexed address/data µP interface bus mode is selected these pins transfer data and commands between the µP and the EPIC. If a demultiplexed mode is used, these bits interface with the system data bus.
VSS	24	27	I	Ground: 0V
$\overline{RD}$	25	28	I	Read: The signal indicates a read operation, active low.
$\overline{WR}$	26	29	I	Write: This signal indicates a write operation, active low.
$\overline{CS}$	27	30	I	Chip select. A low on this line selects the EPIC for a read/write operation.
ALE	28	31	I	Address latch enable. In the Intel type multiplexed µP interface mode a logical high on this line indicates an address of an EPIC internal register on the external address/data bus. In the Intel type demultiplexed µP interface mode this line is hardwired to VSS, in the demultiplexed Motorola type µP interface mode it should be connected to VDD.
$\overline{INT}$	29	32	OD	Interrupt line, active low
DCL	30	33	IO	Data clock input or output in IOM/slave clock in SLD configuration.
FSC	31	34	IO	Frame synchronization input or output in IOM configuration / Direction indication signal in SLD configuration.
DU3/SIP7 DU2/SIP6 DU1/SIP5 DU0/SIP4	32 33 34 35	35 36 37 38	I/IO	Data Upstream Input in IOM configuration. Serial interface port 4, 5, 6 and 7 in bidirectional configuration.

A3	-	39	I	Address Bus Bit 3: This input interfaces to the system's address bus to select an internal register for a read or write access. This pin is only provides in the PLCC package and only active if a demultiplexed µP interface mode is selected.
DD0/SIP0 DD1/SIP1 DD2/SIP2 DD3/SIP3	36 37 38 39	40 41 42 43	O/IO	Data Downstream outputs in IOM configuration. Serial interface ports 0, 1, 2 and 3 in bidirectional configuration.
RES	40	44	I	Reset. A logical high on this input forces the EPIC into the reset state.

Tab. 1.1: Pin Listing

1.5. Logic Symbol

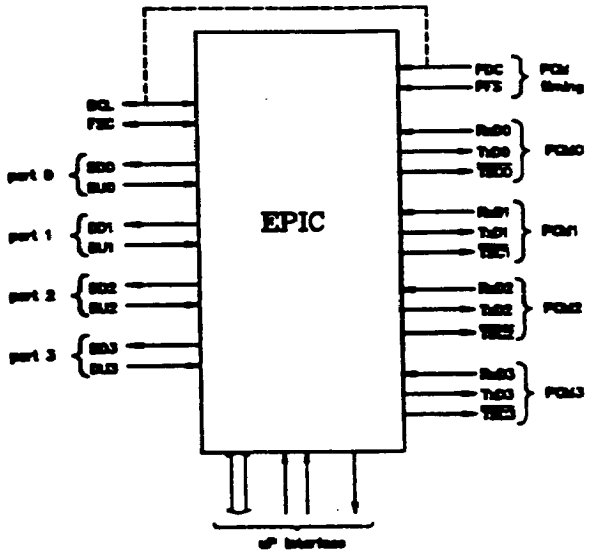


Fig. 1.2: Functional Symbol for the Duplex Configuration

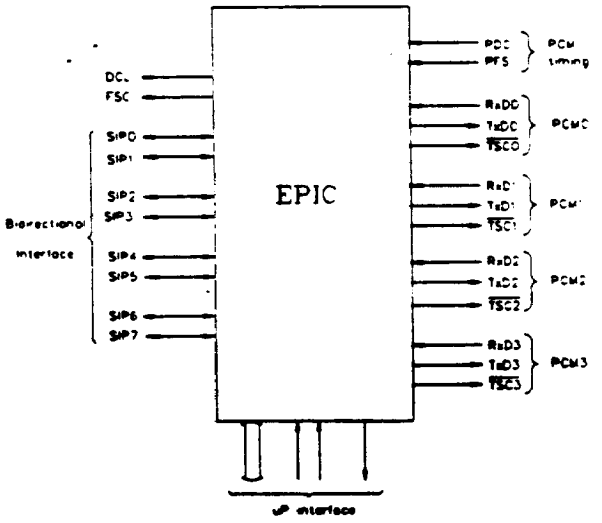


Fig. 1.3: Functional Symbol for the Bidirectional Configuration

1.6. System Integration

1.6.1. Communication Multiplexers

The nonblocking switching capability for various bandwidths implemented in the EPIC makes the circuit suitable for use in communication multiplexers. Due to the data rate programmability of the configurable and PCM interfaces data rate adaption (e.g. between 1544 and 2048 kbps systems) can be accomplished.

1.6.2. Concentrators

Due to the high data rates of up to 8192 kbps the EPIC can be used in concentrator applications.

1.6.3. Central Switches

The EPIC is a nonblocking switch for up to 128 channels per direction. The channel bandwidth can be programmed to 16, 32 or 64 kbps. The PCM and configurable interfaces are programmable for a wide variety of data rates from 8 to 8192 kbps. PCM and configurable interfaces can be operated with different clock frequences. Thus, the EPIC can be used in central switches and for data rate adaption.

1.6.4. Line Cards

The EPIC is designed to operate in 3 different digital or analog line card architectures. For a schematic summary of these possible line card configurations refer to figure 1.4

With its configurable interface being programmed as a SLD interface, it can communicate with SLD compatible devices (e.g. Siemens Codec Filter, SICOFI™, PEB 2060 or ISDN Subscriber Access Controller ISAC™-S, PEB 2085). Connected to up to 16 SICOFIs, the EPIC can serve up to 16 analog lines. Used together with ISAC-Ss, the EPIC provides the signals for up to 16 ISAC-S, to support up to 16 S-interfaces.

Alternatively, the configurable interface may be selected as IOM interface, which is compatible to both the multiplexed IOM1 and the IOM2interface.

If the multiplexed IOM1 interface is chosen, the EPIC supports up to 32 ISDN subscribers on the digital line card. The interface lines are then connected to the EPIC, an IOM1 compatible layer 1 device e.g. the S-bus controller (SBC, PEB 2080), the ISDN Burst Transceiver Circuit (IBC, PEB 2095) or the ISDN Echo Cancellation Circuit (IEC, PEB 2090) and, optionally, an IOM1 compatible layer 2 device e.g. the ISDN D Channel Exchange Controller (IDEC, PEB 2075).

In the case of an IOM2 interface the EPIC supports up to 32 ISDN or 64 voice subscribers. They are connected via the SBCX (PEB 2081), IBC-B (PEB 2096) or IEC (PEB 20901 and PEB 20902) and a digital loop. In both cases either the ICC-B (PEB 2070) or the IDEC (PEB 2075) may perform the D channel handling.

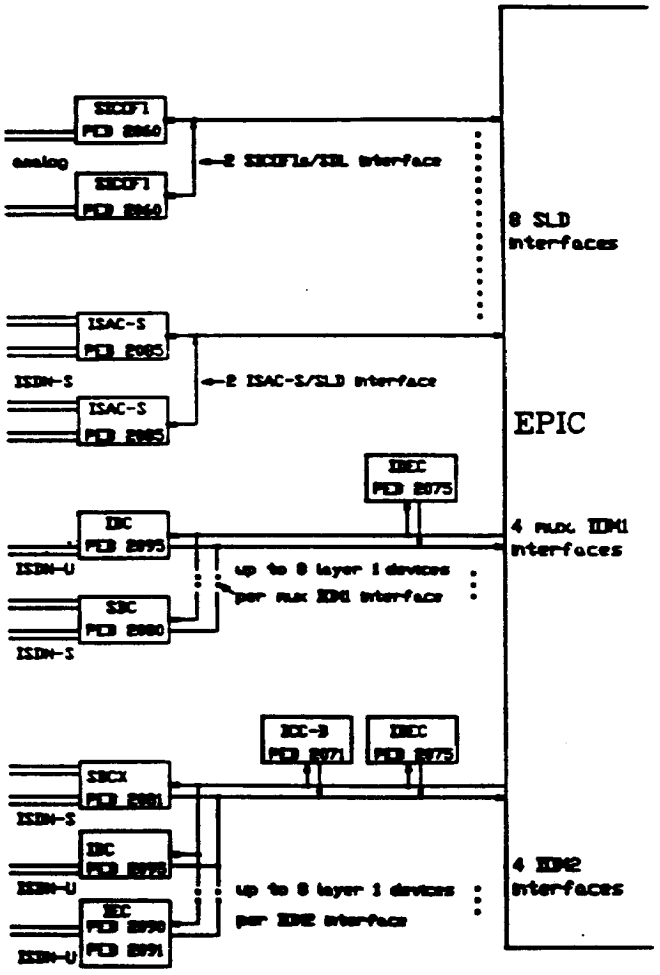


Fig. 1.4: Schematic Summary of the Line Card

1.6.5. Analog Line Card

In analog line cards the EPIC controls the signaling, voice and data paths of 64 kbps channels.

In combination with SLD compatible devices e.g. the highly flexible Siemens Codec Filter (PEB 2060), it forms an optimized analog subscriber line board architecture as shown in figure 1.5. The HSCX (High Level Serial Communication Controller, SAB 82525) handles the signaling information contained in a time slot of programmable bandwidth at the PCM interface or on a dedicated signaling highway.

Moreover, the EPIC controls the feature control and signaling channels and buffers these channels to the µC.

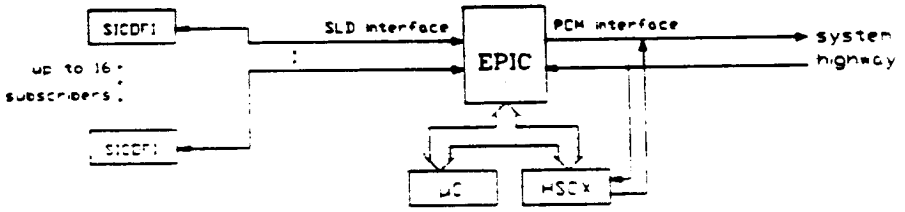


Fig. 1.5: Example of an Analog Line Card Architecture

1.6.6. Digital Line Cards

On digital line cards, the EPIC performs the switching function for up to 32 ISDN subscribers between the PCM system highways and the IOM interfaces. Moreover, it has the layer 1 controlling capability of buffering the C/I and monitor channels of the IOM interface.

The EPIC can be operated in tandem, i.e. one device is active, another one is a backup device. The backup device can instantaneously take over from the active device when the active device fails. Due to this tandem operation capability and the high number of ISDN subscribers which can be connected to one EPIC, the use of single line cards is feasable.

Several architectures are possible.

In completely decentral D channel processing architectures (Fig. 1.6), the processing capacity of a line card is usually dimensioned to avoid blocking situations even under maximum conceivable D channel traffic conditions. In such an architecture the EPIC switches the B channels and performs C/I and monitor channel control. The IDECs handle the layer 2 functions for signaling and data packets in the D channel and transfer the extracted data via the µP and an HDLC controller, e.g. the HSCX (Enhanced High Level Serial Communication Controller SAB

82525) to the system. One of the channels of the HSCX may be used for example for the signaling information, the other for data packets. The HSCX may access either a time slot of programmable bandwidth on one of the system highways (Fig. 1.6) or a separate signaling highway (Fig. 1.7). In both cases the highway capacity used for packet traffic can be shared among several line cards due to the statistical multiplexing capabilities of the HSCX.

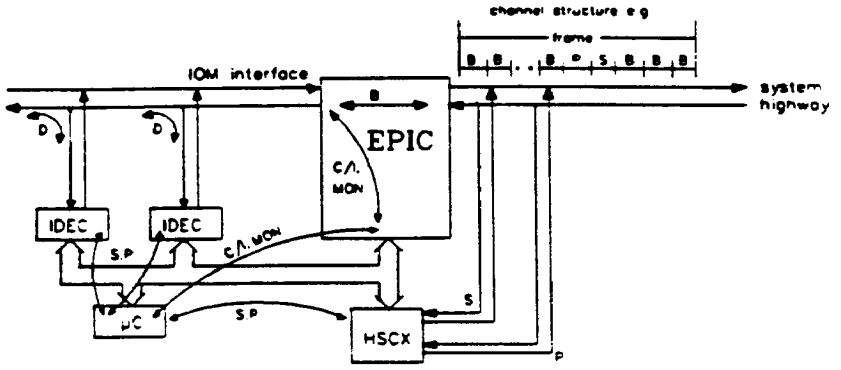


Fig. 1.6: Completely Decentral Packet Switching Digital Line Card Architecture

In an architecture with completely central D channel handling (Fig. 1.7), the EPIC switches the B and D channels and performs the C/I and monitor channel control functions.

The line card microcontroller programs the EPIC and is connected to the group control via a signaling highway and an HSCX. Moreover the EPIC controls the layer 1 protocol on the IOM interface, buffering the C/I and monitor channels to the microprocessor.

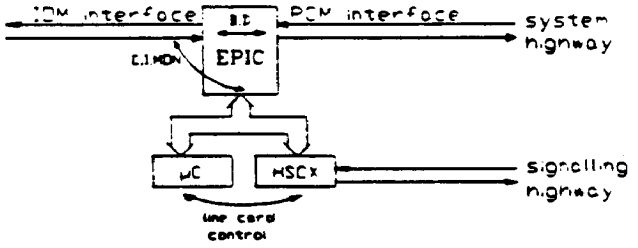


Fig. 1.7: Digital Line Card Architecture with a Completely Central D Channel Handling

A third possibility is a mixed architecture with central packet data and decentral signal handling. This is a very flexible architecture which reduces the dynamic load of central processing units by evaluating the signaling information on the line card. For this case, any increase of packet data traffic does not necessitate any changes in the architecture since the line cards do not have to be modified. The central packet handling unit can simply be expanded.

For such an architecture, the EPIC performs B and D channel switching in addition to C/I and monitor channel control. The IDECs handle the signaling data of the D channel. These messages are transferred to the group controller via the microprocessor and an HDLC controller. The packet data of the D channel are switched to the system highways and processed by the central packet unit.

In this architecture, the EPIC switches the B channels from IOM port A (Fig. 1.8) to the PCM interface. The IDEC works in a master/slave configuration. Therefore, an additional collision resolution line is needed. The IDEC separates signaling from data packets. The signaling messages are transferred to the μC, which in turn hands them over to the group controller using the HSCX.

The packet data are processed differently. Together with the collision resolution line they are handled by the IDEC at another IOM port (port B). The EPIC switches the channels of these ports to the PCM interface as shown in figure 1.8.

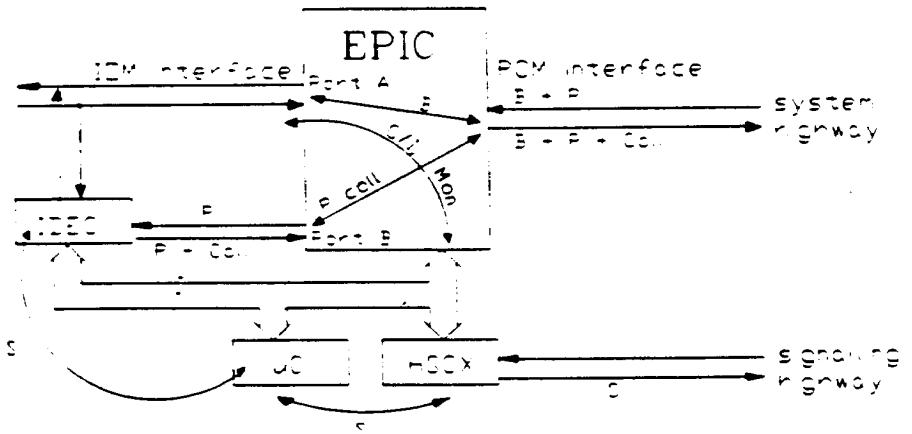


Fig. 1.8: Line Card Architecture for Mixed Packet Handling two IOM Ports of the EPIC

In such a configuration, the p packets and the collision resolution signal occupy one of the IOM ports available at the configurable interface. This reduces the total switching capability of the EPIC to 24 ISDN subscribers.

Alternately, the packet data and the collision line can be directly exchanged between the IDEC and the PCM highway. The EPIC then simply switches the B channels (see figure 1.9). The

packet data are separated by the IDEC and placed on the PCM highway. Thus, the full 32 subscriber switching capability of the EPIC is retained.

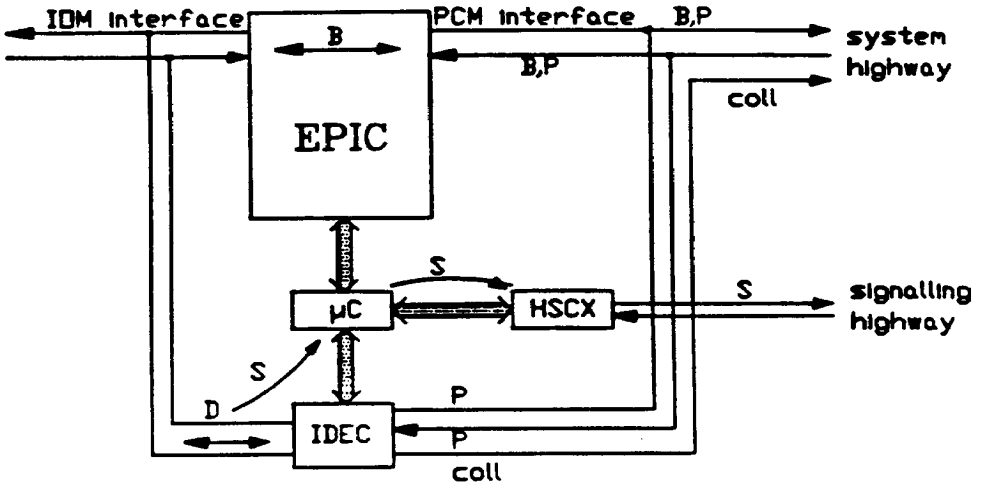


Fig. 1.9: Digital Line Card Architecture for Mixed Packet Handling Using a Collision Highway

1.7. Packet Handlers

The EPIC is an important building block for networks based on either central, decentral or mixed signaling and packet data handling architectures. Its flexibility allows for the modification of the packet handling architecture according to the changing needs.

Thus, it may be useful to add central packet handling groups to a network originally based on decentral signaling packet handling. This may be the case if growing data packet traffic exceeds the initial capacity of the network. The result is a mixed architecture .

On the other hand, increasing packet handling demand on a few dedicated subscriber lines calls for solutions which back up the capacity at these few decentral line cards.

In both of these cases and several other applications, the EPIC is a powerful device for solving the problem of packet handling. In most applications it is used together with the IDEC (ISDN D Channel Exchange Controller).

Decentralized and mixed packet handling has already been covered in the line card chapter. In the following, the centralized signaling/data packet handlers built up with the EPIC will be described.

Central packet handling is used if many subscribers with a generally low demand for packet switching are to be connected to a system. Concentrating the packet servers for multiple users eliminates the need to provide a packet server channel for every user. The overall number of packet server channels can thus be reduced.

In such a central packet handling group, the EPIC performs the switching and concentrator function. It connects a variable number of PCM highways to the packet handler internal highway. HDLC controllers are also connected to this internal highway as illustrated in figure 1.10.

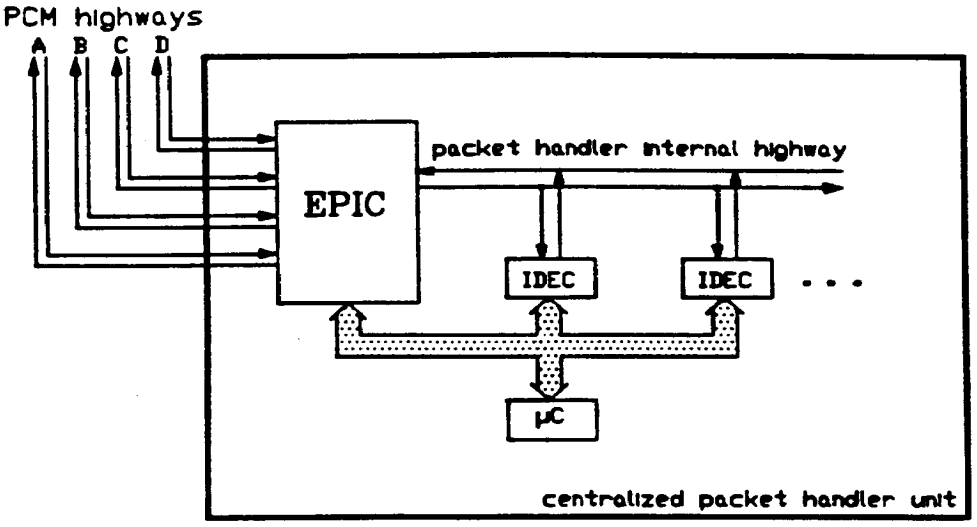


Fig. 1.10: Centralized Packet Handler with a single Internal Highway Connected to 4 PCM Highways

This figure shows one EPIC connecting four PCM highways to one packet handler internal highway. These highways are accessed by the IDECs (ISDN D channel Exchange Controller) which are 4 channel HDLC controllers and handle the packets. If more than four PCM highways shall be connected to the centralized packet handler, further EPICs are necessary. Such a situation is shown in figure 1.11, where 8 highways are switched to one packet handler internal highway. In this case the two EPICs are connected in parallel at the packet handler internal side.

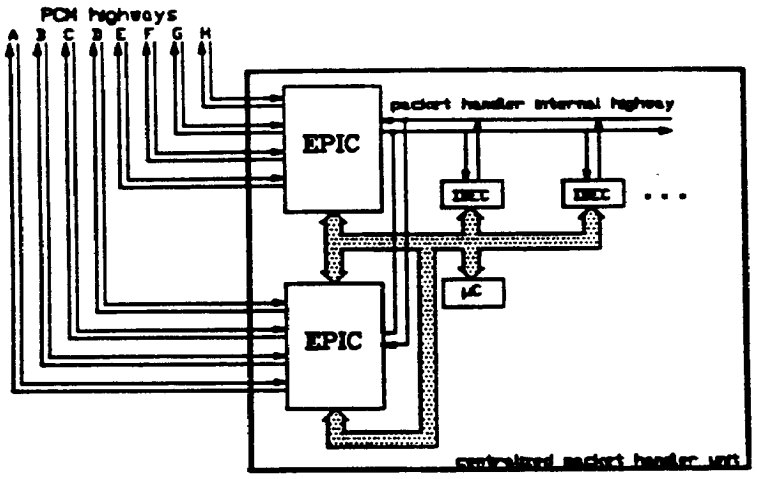


Fig. 1.11: Centralized Packet Handler with One Internal Highway Connected to 8 PCM Highways

The data rate of the packet handler internal highway can be up to 4096 kbps. If this capacity is not sufficient, other packet handler internal highways may be added as shown in figure 1.12.

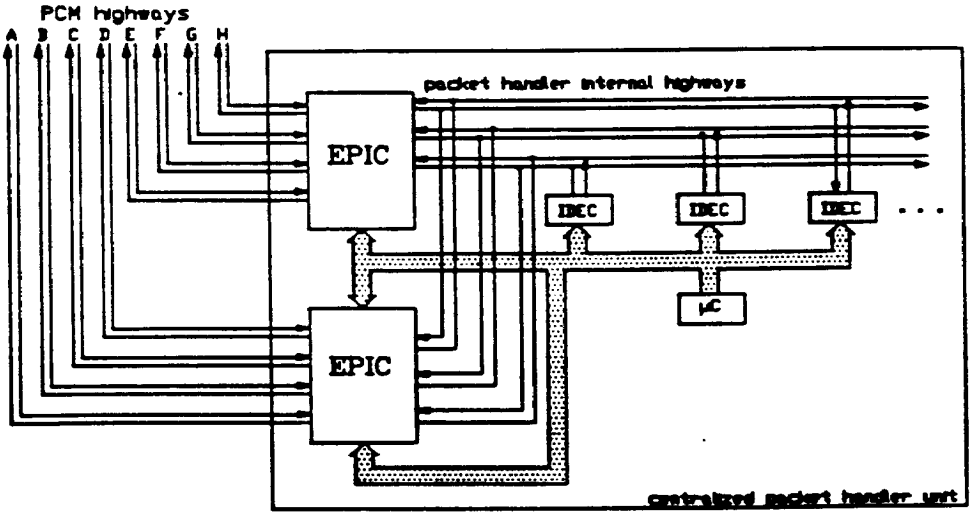


Fig. 1.12: Centralized Packet Handler with 3 Internal Highways

In some applications an additional collision resolution signal is required for the HDLC controllers. This information can be demultiplexed from the PCM highways to a third line for each packet handler internal highway (see figure 1.13).

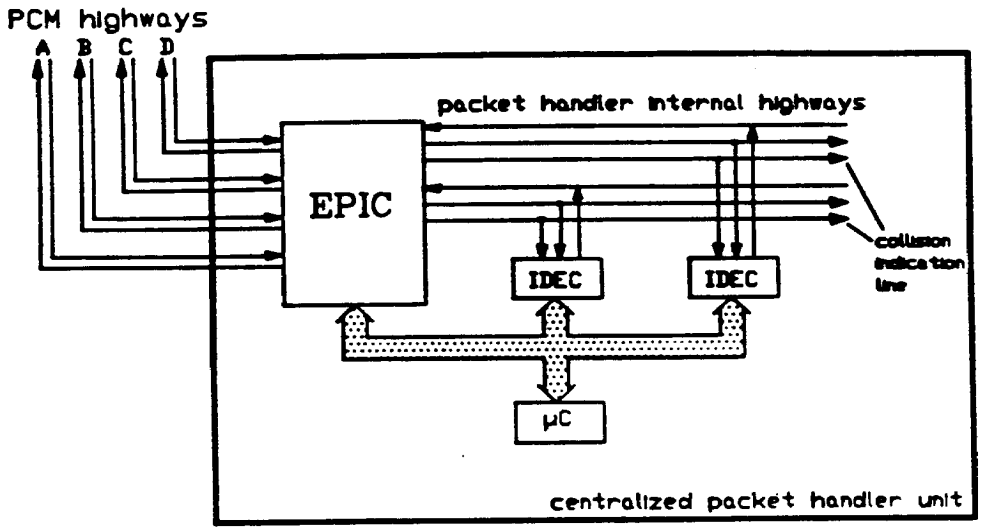


Fig. 1.13: Centralized Packet Handler with Internal Collision line

The applications illustrated apply equally to centralized signaling as well as to data packet handlers.

2. Functional Description

In the following chapters the functions of the PEB 2055 will be covered in more detail.

2.1. PCM Interface

The PCM Interface formats the data transmitted or received at the PCM highways. Via PMOD: PMD1, PMD2 it can be configured to one, two or four PCM ports consisting each of a data receive (RxD#), a data transmit (TxD#) and an output tristate indication line (TSC#).

As stated in table 4.2 the *maximum* data rate with four PCM ports is 2048 kbps (PCM mode 0), with two PCM ports 4096 kbps (PCM mode 1), for one PCM port it is 8192 kbps (PCM mode 2). However, the *actual* data rate may be varied in a wide range. It is programmed to PBNR. In PCM mode 0 this register contains the number of bits per frame minus 1 bit, in PCM mode 1 half the number of bits minus 2 bits and in CM mode 2 the fourth of the number of bits per frame minus 4 bits. Hence the data rate can be stepped in 8, 16 or 32 kbps increments in PCM mode 0, 1 and 2, respectively.

E.g., selecting the T1 data rate (1544 kbps) at the system interface PBNR = 11000000 has to be programmed (PCM mode 0). To initialize the EPIC for a 8192 kbps data rate in PCM mode 2 PBNR has to be written with FF_H.

To properly clock the PCM interface a PDC signal with a frequency equal to or twice the data rate has to be applied to the EPIC as selected in PMOD: PCR.

For the synchronization of the time slot structure a framing signal needs to be connected to the EPIC's PFS pin. The rising edge of this signal is evaluated by the device.

Under the control of PMOD: PSM this occurs either with the rising or the falling PDC slope as shown in figure 4.1. The PFS pulse is of arbitrary length. However, it must be ensured that the framing signal is low for at least the last PDC clock period before the next framing pulse.

The PFS period is internally checked against the duration expected from the PBNR and PMOD: PCR entries. E.g. programming PBNR = 11000000 (1544 kbps) and PMOD:PCR = 1 a PFS period equal to 386 PCL clock periods is anticipated.

After reset, the EPIC reaches synchronism having received two consecutive correct PFS pulses. Synchronization is considered lost by the device if the PFS signal is not repeated with the correct repetition rate. The PCM synchronization status can be seen in STAR: PSS. For any change in the synchronization status a maskable interrupt (ISTA: PFI, MASK: PFI) is generated.

A logical 1 indicates the synchronous state, a logical 0 shows, that synchronism has been lost.

Without programming the bit shift function of the EPIC'S PCM interface, the rising edge of the PFS signal marks the following bits:

upstream	PCM mode 0:	bit7, time slot	29
	PCM mode 1:	bit7, time slot	58
	PCM mode 2:	bit7, time slot	116
downstream	PCM mode 0:	bit7, time slot	2
	PCM mode 1:	bit7, time slot	4
	PCM mode 2:	bit7, time slot	8

In upstream direction the maximum number of bits in the relevant PCM mode is assumed. In the case of a lower bit count per frame the PFS signal marks an according bit in the frame. E.g., in a 1536 kbps system (24 time slots numbered 0 through 23/frame in PCM mode 0), it marks bit 7 of the time slot 21.

The time slot structure may be shifted using the POFD, POFU and PCSR registers.

The correlation between the framing signal PFS and the bit stream is controlled by the content of these registers as shown in table 2.1.

Register Bits	Direction	PCM Mode
POFD: OFD9..2, PCSR: OFD1..0	downstream	2
POFD: OFD9..2, PCSR: OFD1	downstream	1
POFD: OFD9..2	downstream	0
POFU: OFU9..2, PCSR: OFU1..0	upstream	2
POFU: OFU9..2, PCSR: OFU1	upstream	1
POFU: OFU9..2	upstream	0

Table 2.1: Register Bits Correlating PFS Signal and PCM Bit Stream

These register contents denote the number of bit periods, the PCM frame is shifted. A few examples are given in figure 2.1.

After reset, with single rate clocking, the downstream data is input and upstream data is output with the falling edge of the PDC signal. However, programming the PCSR: DRE and URE bits with a logical 0, these instants may be changed to the rising edge. Thus the frame structure can be shifted by a half bit period. For a picture of this behaviour - also with double rate clocking, please refer to figure 4.1.

Another feature of the EPIC's PCM interface is its' alternative input function. In PCM mode 1 and 2, the unused input ports can be used for redundancy purposes. In these modes, for every active input port there exists a second input port, which can be connected to a redundant PCM input line. The EPIC checks the input from the two lines for mismatches. PMOD: AIC0, AIC1 control this comparison function of the EPIC. With AIC0 active (logical 1) the EPIC compares RxD 1 and RxD0 in PCM mode 1 and stores the timeslot, where a mis-

match occures in the PICM register. Similarily, an active PMOD: AIC1 enables the comparison function between RxD2 and RxD3 (in PCM modes 1 and 2). PMOD: AIS1, AIS0 associate the lines to the logical ports. For the active output lines the $\overline{TSC\#}$ pins indicate the output driver impedance. $\overline{TSC1}$ and $\overline{TSC3}$ output the value programmed to AIS0 and AIS1, respectively.

For a tabularic summary of the PCM interface line functions please refer to table 4.3.

Finally all PCM outputs may be switched to high impedance. (OMDR: PSB). Thus redundand systems with one of two devices working in standby mode are feasible.

2.2. Configurable Interface

The CFI formats the data transmitted or received at the DD#, DU# or SIP# lines. Via CMD1: CMD1, 0 it can be configured to one, two or four duplex ports consisting each of a data downstream (DD#) and a data upstream line (DU#), or to eight bidirectional lines (SIP#).

As stated in table 4.6 the *maximum* data rate with four duplex ports is 2048 kbps (CFI mode 0), with two duplex ports it is 4096 kbps (CFI mode 1), with one duplex port 8192 kbps (CF0 mode 2) and with eight bidirectional ports 1024 kbps (CFI mode 3). The *actual* data rate, however, is subject to the CMD2: CBN9, 8 and CBNR entries and may be varied in a wide range. In each CFI frame there are (CBN9..CBN0)8 bits plus one bit. Hence, the data rate can be stepped in 8 kbps increments in all CFI modes.

To properly clock the CFI a reference clock (RCL) of a specific frequency is required, as also stated in table 4.6.!

In CFI modes 1 and 2 this frequency is equal to the actual data rate, in CFI mode 0 it is twice the actual data rate and in CFI mode 3 four times the actual data rate. Thus, a 2048 kHz reference clock is needed for a bidirectional setup with a 512 kbps data rate or for a duplex setup with 2 ports and a 2048 kbps data rate. This reference clock may be obtained from the DCL pin (CMD1:CSS = 1) or the PDC pin (CMD1:CSS = 0) subject to the prescalor divisor selection (see figure 2.1).

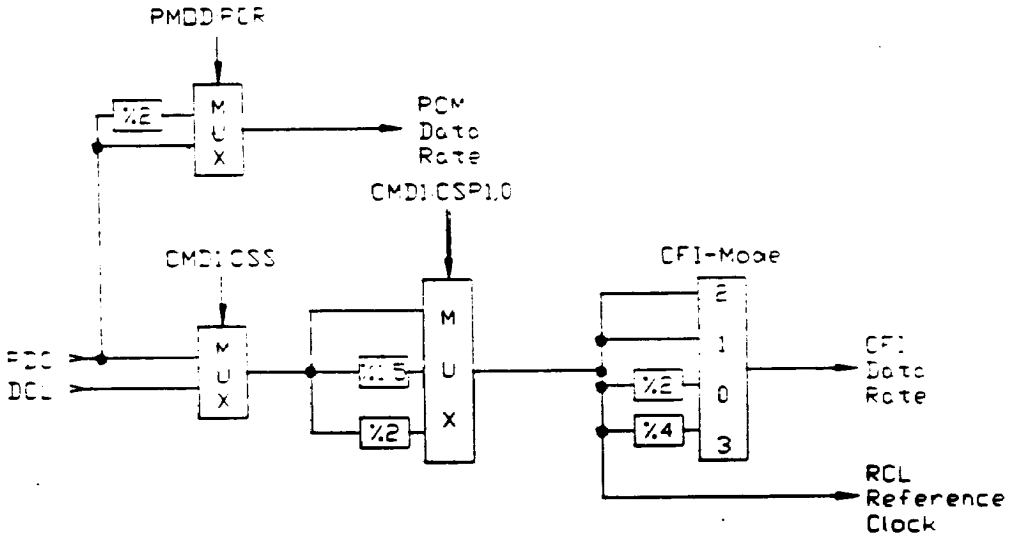


Figure 2.1: EPIC Clock Sources for the CFI and PCM Interface

Depending on the values CMD1: CSP1..CSP0 the external clock is divided by 2, 1.5 or 1. As a result, the reference clock is generated.

Thus, using the PDC as the source for the reference clock, the following data rate ratios between PCM interface and CFI may be obtained.

PCM/CFI data rate ratio	PCM clocking	Prescalor divisor	CFI mode
1	single rate	1	1,2
1.5	single rate	1.5	1,2
2	single rate	2	1,2
2	single rate	1	0
3	single rate	1.5	0
4	single rate	2	0
4	single rate	1	3
6	single rate	1.5	3
8	single rate	2	3
0.5	double rate	1	1,2
0.75	double rate	1.5	1,2
1	double rate	2	1,2
1	double rate	1	0
1.5	double rate	1.5	0
2	double rate	2	0
2	double rate	1	3
3	double rate	1.5	3
4	double rate	2	3

For other data rate ratios DCL has to be used as clock source.

CMD1: CSS also selects the synchronization source. With CMD1: CSS = 0 the synchronization signal is taken from PFS whereas with CMD1: CSS = 1 it is derived from FSC.

Again, the rising edge of the synchronization signal is evaluated by the device. Under the control of CMD1: CSM the signal is evaluated at every positive or negative source clock slope. The framing pulse is of arbitrary length. However, it must be ensured that the framing signal is low for at least the last clock period before the next framing pulse. This behaviour and the pulse shape of the generated reference clock is shown in figure 4.5.

If PDC and PFS are selected as clock and framing sources the EPIC outputs clock signals derived from these at DCL and FSC. As stated in table 4.6 a single rate clock signal with a frequency equal to the CFI data rate or a double rate clock signal (CFI modes 0 and 3) may be generated at DCL (CMD2: COC). Figure 4.5 shows the wave form and phase correlation of the generated output clocks.

The generated output framing signal is controlled by CMD2: FC2..FC0. The different pulse forms are shown in the figures 4.3 and 4.4. Except in FC mode 7 (see table 4.8) they have a period of one frame.

In the framing mode 7 the generation of the framing signal includes the use of two other registers, the timer register and the command register. The timer register defines a period in multiples of 250 µsec (TIMR: TVAL6..TVAL0 = 0: 250 µsec). E.g., setting TIMR: TVAL6..TVAL0 = 01_H defines a period of 500 µsec equalling 4 frames. Programming CMDR: ST = 1 starts the timer. At every but the last frame begin in the predefined period the EPIC then outputs the framing signal of FC mode 6, i.e. a logical 1 during the time slots 0, 1, 2 and 3. At the last frame begin the framing signal of FC mode 3 is sent, i.e. a logical 1 during the first bit period of the frame.

This function is repeated until the timer is stopped (see 2.6.1). For a repetition period of 500 µs the frame signal is shown in figure 4.4.

The bit shift function of the EPIC's CFI is illustrated in figure 4.6. The time slot adjustment register (CTAR) and bit shift register (CBSR) control it. CTAR and CBSR: CDS2..CDS0 shift both upstream and downstream frame in exactly the same way. The CTAR content shifts the frame structure by whole time slots, CBSR: CDS2..CDS0 by single bits. CBSR: CUSR..CUS0 shift the upstream frame relative to the downstream frame by up to 15 bit periods covering the range of two time slots. Finally, the upstream and downstream frame may be shifted by half bit periods independently from each other programming the CMD2: CXF and CMD2: CRR bits accordingly.

Similar to the PCM Interface for CFI mode 1 and 2 the input of a logical port may be chosen from one of two physical lines. This feature is controlled by CMD1:CIS1 and CIS0. A complete list of the physical line allocation is shown in table 4.7. A line comparison and mismatch monitoring is not provided for the CFI.

For unassigned output channels the output driver may be selected to be open drain or tristate (OMDR: COS). OMDR: CSB switches all CFI outputs to high impedance, over ruling the output driver impedance selecting and thus allowing for standby operation in redundand systems.

Different from the PCM interface (see 2.4) the subchannel assignement of the CFI occurs on a per port basis. Two bits per port are provided in the CSCR for this function. Thus, a time slot on a CFI port can contain only one channel having a bandwith of 16, 32 or 64 kbps, and all subchannels on the port have the same position (e.g. bits 5 and 4 of a time slot for a 16 kbps channel).

2.3. Memory Structure and Switching

The EPIC contains two memories, the control memory (CM) and data memory (DM). Their structure and connection is shown in figure 2.2.

The data memory consists of two blocks. The downstream block buffers the data input from the PCM interface, the upstream block the data input from the CFI. The downstream block has a capacity of 128 timeslots to buffer a whole PCM frame. It is written from the PCM interface periodically once every frame controlled by the downstream input counter and read at random to perform the switching function.

The upstream block consists of the data and tristate fields. Similar to the downstream block the upstream data field has a capacity of 128 time slots and is capable to buffer a whole PCM frame to the PCM interface. This field is written at random and read cyclically for PCM interface output, under the control of the upstream output counter.

The upstream tristate field contents control the PCM output impedance. This field is written via the µP interface and read synchronously with the data field. Thus, the impedance information is read together with the data for output at the PCM interface. The tristate field contains 512 bits, structured as 128 x 4, so that one bit of the tristate field is attributed to each of the possible 2 bit/frame sub time slot positions.

The upstream and downstream data field are randomly accessed by either the CFI (for switching) or the µP interface (for information monitoring or idle code implementation).

The control memory is also composed of an upstream and a downstream block. Each block contains 128 locations of 8 bits of control memory data and 4 bits of control memory code. Both blocks are written at random via the µP interface and read cyclically under the control of a seperate counter for each block/upstream input counter, downstream output counter). These counters are synchronous with the CFI upstream and downstream frames.

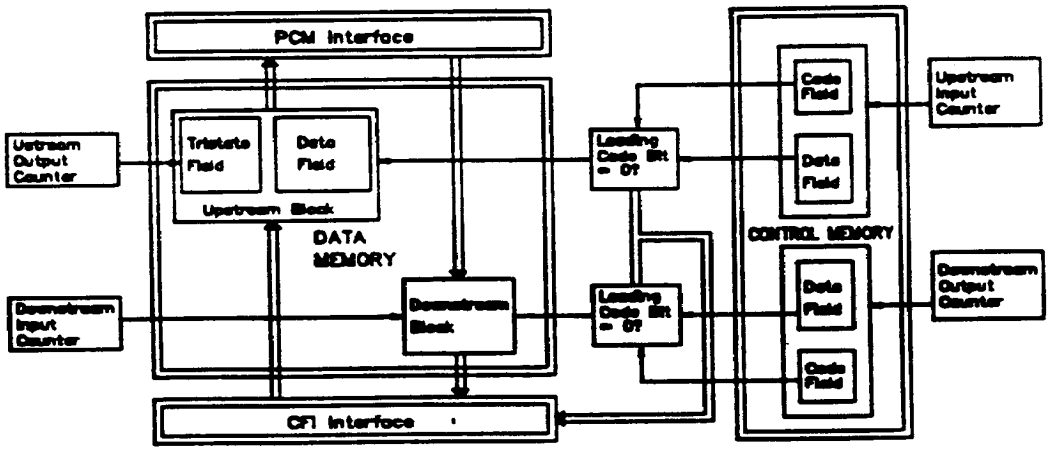


Figure 2.2: EPIC Memory Structure

The code field entries determine, in which way the data field entries are handled. The codes are entered via MACR: CMC3..CMC0 setting MACR: MOC3..MOC1 to 111 (see chapter 4.3). A leading 0 in the code field entry identifies the data field entry as a pointer to a data memory position.

For downstream switching, the downstream block of the CM is read in sequence. If the leading bit of the code field is a logical 0 the corresponding data field entry points to a location in the data memory downstream block. The byte in this data memory location is read into the current downstream CFI frame.

For upstream switching the corresponding upstream blocks are involved.

For proper switching, the CM needs to be programmed for the desired connection. The control memory address corresponds to one particular CFI time slot and port number. The contents of this CM address point to a particular PCM time slot and line number correlated to a fixed location in the data memory.

The lower significant code field bits control the PCM subchannel bandwith and location, i.e. the number of bits and their position within the time slot (see 4.3.1). Thus up to four 16 kbps subchannels may be combined into one byte at the PCM interface. However, in switching operation only one channel or subchannel may be assigned to one CFI time slot, the position and bandwith of which is defined by CSCR.

A leading 1 in the control memory code field entry indicates a CFI data interaction. Thus either a CFI idle code may be programmed or a control channel (IOM applications)/signaling channel (SLD applications) is marked. The function of these channels will be covered in the Control/Signaling section.

2.4. Microprocessor Interface

The EPIC provides interface signals for both, Motorola type and Intel type microprocessors. In the Intel type µP interface mode either a multiplexed or a demultiplexed bus structure may be chosen.

For a demultiplexed bus structure including the Motorola type µP interface the PLCC 44 package of the EPIC needs to be used, since only this package provides the additional lines of a separate 4 line address bus.

The ALE line of the PEB 2055 is used to control the bus structure and interface type. ALE is fixed to + 5V for the Motorola type µP interface and it is switching to signal an address or data transfer in the multiplexed Intel type µP interface mode. Pins 28 and 29 of the PLCC package are interpreted as RD and WR for a Intel type interface or DS and R/W for a Motorola type interface. Tab. 2.2 summarizes these functions.

ALE	Type of µP Interface	Bus Structure	PLCC pin 28	PLCC pin 29	package
fixed to VDD fixed to ground switching	Motorola Intel Intel	demultiplexed demultiplexed multiplexed	DS RD RD	R/W WR WR	PLCC PLCC DIP or PLCC

Table 2.2: µP Interface Functions

In the multiplexed µP interface mode the addresses as outlined in the detailed register description are used, AD0 is always fixed to logical 0. This simplifies the use of a 16 bit Intel type processors.

For a demultiplexed µP interface, in addition to the A3 to A0 lines the OMDR: RBS bit is needed for addressing a register. With OMDR: RBS (register bank selection) one of two register banks is selected. RBS = 1 selects a set of registers used in the device initialization phase (e.g. CFI interface and CM initialization), RBS = 0 switches to a group of registers necessary during operation (e.g. connection programming, special channel programming).

The OMDR register containing the RBS bit can be accessed with either value of RBS.

For memory accesses the memory access registers are provided. Fig. 2.3 visualizes the functions of these registers. The memory access adddress register contains the address of a specific location of the data or control memory, the memory access data registers the content to be read or written. The memory access control register content controls the memory access.

There are control codes to access the

- data memory upstream tristate field
- data memory data fields
- control memory data fields
- control memory data and code fields simultaneously.

A memory access using the actual MADR and MAAR contents is performed upon every MACR write access.

During the processing of the memory access, which takes at most 9.5 RCL periods, STAR: MAR is set.

For a detailed descriptions of the codes please refer to chapter 4.3.

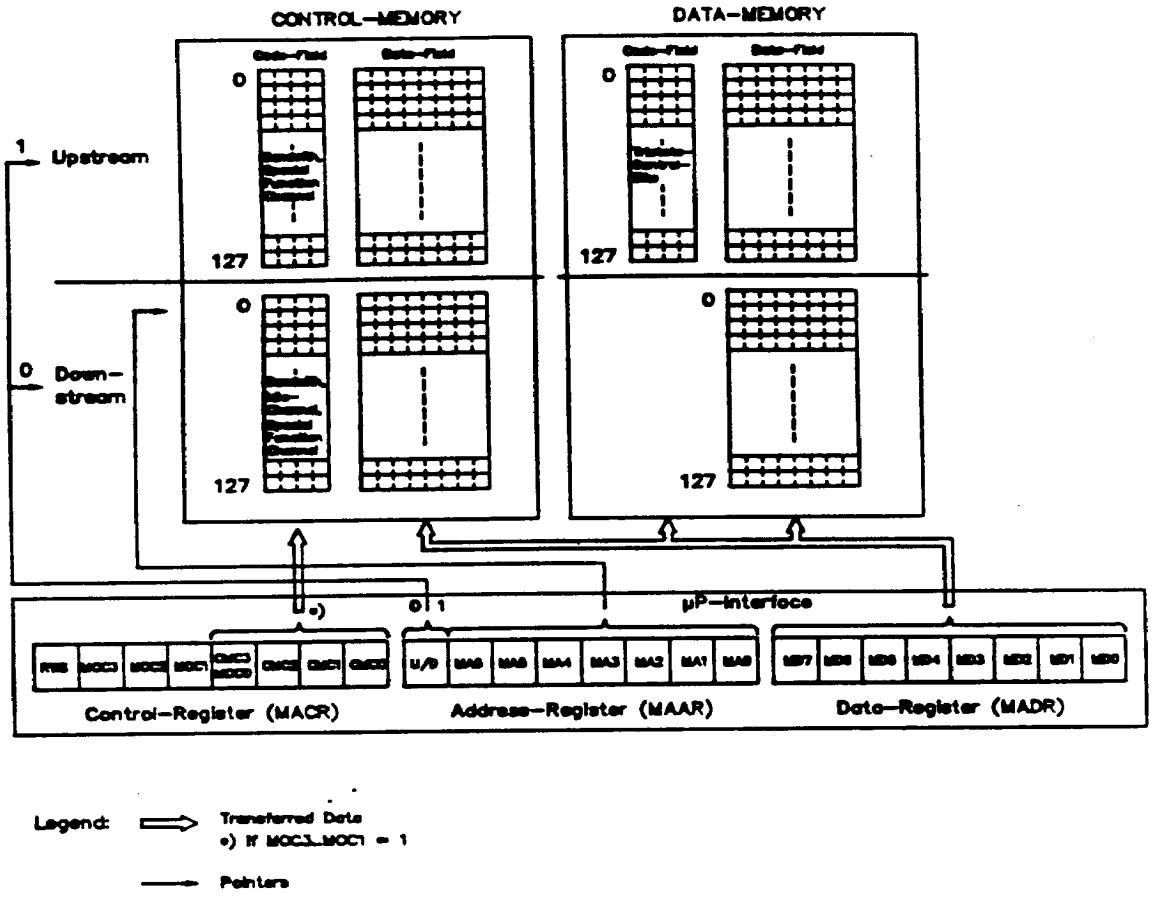


Figure 2.3: Data Transfer between µP-Interface and the Memories

The following few examples illustrate the behaviour of the EPIC.

In PCM mode 0 the instruction sequence

```
MADR   01011000
MAAR   11000110
MACR   00001000
```

instructs the EPIC to output the idle code 58_H in time slot 16 at the PCM port 3.

Then programming

```
MADR   00001111
MAAR   11000110
MACR   01100000
```

will switch the output drivers at the PCM port 3 to low impedance in the selected time slot 16.

Now programming

```
MADR   11000110
MAAR   10100010
MACR   01110001
```

will establish a connection from CFI time slot 8 port 1 (CFI mode 0) to PCM port 3 time slot 16 erasing the idle code.

whereas the instruction sequence

```
MAAR   01000110
MADR   00100010
MACR   01110111
```

would set up a connection between bits 7..6 of time slot 18 of PCM port 0 (input) and the CFI time slot 70 (output). PCM mode 1 and CFI mode 2 are assumed, the CFI subchannel position is determined by the CSCR content.

The code

```
MADR   10101001
MAAR   10101011
MACR   01110010
MAAR   00110111
MADR   10101001
MACR   01110010
MADR   00000000
MAAR   10101001
MACR   01100000
```

loops back the bit 3..0 sub time slot of time slot 11 at the CFI port 1 to time slot 13 of CFI port 3. CSCR, = xxxx11xx, CFI mode 0 and PCM mode 1 are assumed. The output of PCM time slot 21 port 0 is hold at high impedance. By selecting the bits 7 of MAAR and MADR the switching mode is elected for MACR:MOC3..MOC1 = 111 according to table 2.3.

bit 7 MAAR	bit 7 MADR	Switching Mode
0	0	Connection PCM → CFI
1	1	Connection CFI → PCM
0	1	CFI → PCM → CFI
1	0	PCM → CFI → PCM

Table 2.3: Switching Modes

2.5. Preprocessed Channels

The EPIC supports the

- Monitor/Feature Control (MF) and
- Control/Signaling (CS)

channels at the CFI.

The monitor handler takes care of the monitor/feature control channels, the signaling handler of the control/signaling channels. These channels are established by programming an appropriate code (as shown in figures 4.14 and 4.15) for two consecutive CFI time slots (starting with the even time slot number) to the control memory. The even address maps to the monitor/feature control channel, the consecutive odd to the control/signaling channel.

The possible code combinations for the different applications are listed in table 2.4.

Application	Upstream Codes		Downstream Codes	
Decentral ISDN-D Channel Handling	1000	0000	1000	1011
Central ISDN-D Channel Handling	1000	16kbps channel code	1000	16 kbps channel code
6 Bit Signaling (e.g. analog IOM)	1010	1010	1010	1011
8 Bit Signaling (e.g. SLD)	1011	1011	1010	1011
CM-Address	even	odd	even	odd

Table 2.4: Possible Preprocessed Channel Codes

2.5.1. Signaling Handler

In downstream direction the relevant content of the control memory data field location with the even address is transmitted in the odd time slot (signaling channel). In the central D channel handling scheme the two bits of the current control memory data field location, which are selected by the code residing in the code field, are added.

This is shown in figure 4.15.

In upstream direction the signaling handler monitors the received control/signaling channels. Upon a change

- an interrupt is generated (ISTA, MASK:SFI)
- the address of the specific channel is written into the C/I FIFO and
- the actual value is stored in the even control memory data field locations.

In the central D channel handling scheme the two D channel bits are written to the odd data field location at a position identified by the code residing in the code field of the same location (table 4.16).

In the 6 bit and 8 bit signaling schemes the odd data field location contains the stable value the even data field location the actual value. The actual value is subject to the double last look procedure (LL procedure). As shown in figure 2.7 the actual value is sampled when the last look period runs out the next time and again a double last look period later. The actual value is copied to the stable value, if it is identical to the two samples. This period is controlled by the timer register (TIMR). If TIMR: SSR is selected to logical 1, the double last look period is fixed to 125 µsec, otherwise it is a multiple of 250 µsec. Depending on TIMR: TVAL6..TVAL0 it may thus be varied from 250 µsec (TIMR = 00_H) to 32 ms (TIMR = $7F_H$).

The signaling FIFO is 9 bytes deep and can thus hold 9 channels, where the signaling information changed. Each entry in this FIFO includes the SBV bit indicating the validity of the entry. The polarity of SBV (SBV = 1: valid entry) has been chosen such that a valid C/I FIFO entry can instantaneously be used for control memory accesses without manipulations: A valid pointer selects the upstream block of the CM. Moreover SAD0 is set to logical 1 (odd address) if the 6 or 8 bit signaling scheme is used pointing to the stable value. In the ISDN D-channel handling schemes it is fixed to logical 0 for an access of the C/I information at the even address location.

The complete signaling FIFO is reset, i.e. all SBV bits are set to logical 0 by selecting OMDR: OMS0 = 0 or by instructing the EPIC to reset the C/I FIFO with CMDR: MFFR = 1.

2.5.2. Monitor Handler

The monitor handler communicates with the subscriber circuits subject to the IOM or SLD protocols. It works either with active (only in IOM applications) or with not active handshake protocol as selected in OMDR: MFPS. With the handshake protocol active each byte exchanged between the EPIC and the subscriber in the monitor channel is internally autonomously acknowledged for a safe communication. When the handshake protocol is not active the bytes constituing the message are sent one per frame.

The monitor handler only works upon it has been instructed with a proper selection in the command register.

The time slot and port/line numbers coded in MFSAR/MFAIR: SAD5..SAD0 may be identified using table 4.17. In this case an additional least significant logical 0 and a most significant bit depending on the transmission direction has to be assumed.

HANDSHAKE PROTOCOL ACTIVE

With the handshake protocol active the following commands are provided by the EPIC.

- By setting CMDR: MFSO to logical 1 the EPIC starts to look for active monitor channels. As soon as an active channel is found the ISTA, MASK: MAC interrupt is generated and the address of this channel is stored in MFAIR: SAD5..SAD0.

  The search for an active monitor channel is stopped, when one such channel has been found or when a logical 0 is written to CMDR: MFSO.

  The address of a found channel may be copied to MFSAR: SAD5..SAD0 for further processing.

- By setting CMDR: MFT1, MFT0 to 01 the EPIC starts transmitting the content of MFFIFO. When the message has been completely transferred, the ISTA, MASK: MFFI interrupt is generated. The group of recipient subscribers is defined by MFSAR: MFTC1, MFTC0. Programming these bits with

- 00 the message is sent to the subscriber with the address specified in MFSAR: SAD5..SAD0.

- 01 the message is broadcast in all monitor channels. The MF bytes are transmitted at maximum speed, i.e. one byte per three frames. The arriving acknowledgments are ignored.

- 10 the MFFIFO content is not transmitted and may instantaneously be read again (test operation). The ISTA, MASK: MFFI interrupt is also generated instantaneously.

- For the transmission of messages longer than 16 bytes the selection CMDR: MFT1, MFT0 = 11 is provided. This choice transmits a block of 16 bytes and interrupts the microprocessor for the next bytes to be written to MFFIFO. (ISTA, MASK: MFFI; STAR:MFAE = 1, MFRW = 0). The last block of such a long message in transmitted programming CMDR: MFT1, MFT0 to 10.

  Such a long message can only be transmitted to a single subscriber (MFSAR: MFTC1, MFTC0 = 00).

- Setting CMDR: MFT1,0 to 10 an answer to the sent message is expected from the same subscriber (same port, same time slot). The MFTC1, MFTC0 bits need to be fixed to 00. The message is stored in MFFIFO and as soon as it is complete the ISTA, MASK: MFFI interrupt is generated.

In all cases the transmitted message consists of the MFFIFO content prior to the command.

If a message shall be received without transmission (e.g. an active monitor channel has been found) the receive and transmission command is issued with an empty MFFIFO.

The STAR: MFAB bit is set, if the remote partner aborts the reception of an arriving message.

HANDSHAKE PROTOCOL INACTIVE

With the handshake protocol not active a search for an active monitor channel is not possible. The EPIC always outputs transmitted messages at full speed, i.e. one byte per frame. Keeping that in mind the transmit (CMDR: MFT1, MFT0 = 01) and transmit + receive same timeslot (CMDR: MFT1, MFT0 = 10) commands are similar to the active handshake protocol case. Executing the CMDR: MFT1, MFT0 = 11 command, however (transmit + receiver same line), the EPIC expects the arriving bytes at the same line, but four time slots later than those it sent the transmitted bytes to. (SLD application)

In both transmit + receive cases the number of expected bytes is programmed to MFSAR: MFTC1,0 bits. Setting these bits to

00	1	byte
01	2	bytes
10	8	bytes
11	16	bytes

of answer are expected.

Before every command and after each MFFI interrupt STAR should be read. The bits MFT0, MFAB, MFAE, MFRW and MFFE show the state of the monitor handler.

To reset the MFFIFO CMDR: MFFR has to be set.

2.5.3. Synchron Transfer

The synchron transfer utility allows the synchronous exchange of information between the PCM interface, the configurable interface and the µP interface for two independent channels (A and B).

The information is buffered in the µP transfer data register. It is copied to there from a data memory location ponted to by the content of the µP transfer receive register and copied from the data register to a data memory location programmed to the µP transfer transmit register.

The transmit and receive register contents identify the interface as well as the time slot and port numbers of the involved channels according to tables 4.16 and 4.17. Further bits in µP transfer control register allow to restrict the synchron transfer to one of he possible sub time slots and are enabling or disabling the facility.

Thus it is possible to read information from the PCM interface input to the Synchron Data Transfer Register (STD#) via the downstream data memory and to transmit it from STD# back to the PCM output via the upstream data register, routing a loop from the PCM interface to the PCM interface. Similarily the synchron transfer facility may be used to loop configurable interface channels or to establish connections. While the information is stored in the data register it may be read and or manipulated by the µP.

The data flow paths for the EPIC as a whole are shown in figure 2.4, for the synchron transfer facility they can be seen in figure 2.5.

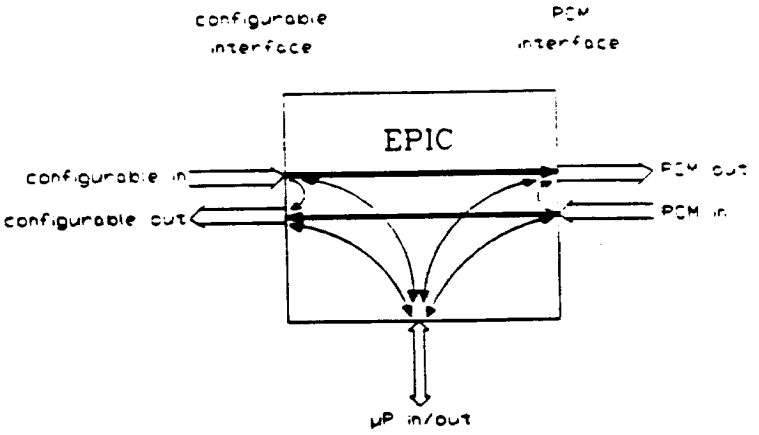


Figure 2.4: Transmission and Access Possibilities of the EPIC

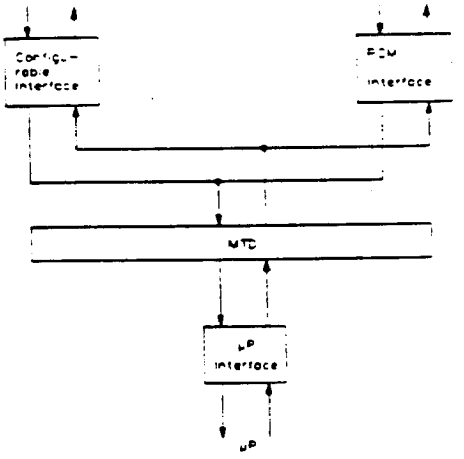


Figure 2.5: Synchron Transfer Paths between the µP, PCM and Configurable Interfaces

In upstream transmit direction ist is necessary to ensure that no other data memory access writes to the same location in the upstream block. Hence an upstream connection involving the same PCM port and timeslot as the synchron transfer may not be programmed.

An idle code entered to the data or connection memory for the upstream or downstream directions is overwritten.

The EPIC generates interrupts guiding through the synchronous transfer. Upon the ISTA, MASK: SIN interrupt the data registers may be accessed for some time. If the data register of an active synchron transfer channel has not been accessed at the end of this time interval the ISTA, MASK: SOV interrupt is genrated, before the EPIC performs the transfer to the memory locations. After that it again issues the ISTA, MASK: SIN interrupt and the access window opens again. The repetition cycle of the synchronous transfer is identical to a frame length. The access window is closed for at most 16 RCL periods per active channel + 1 RCL period, leaving a very long data register access time. This behaviour is also shown in figure 2.6.

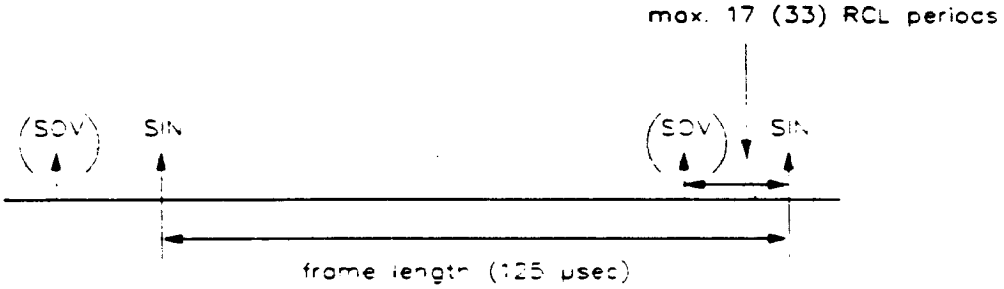


Figure 2.6: Synchron Transfer Flow Diagram

2.6. Special Functions

2.6.1. Hardware Timer

The EPIC provides an hardware timer continuously interrupting the µP after programmable time periods. The timer period is selected by programming TIMR: TVAL6..TVAL0. It's value is given there in multiples of 250 µs. Programming e.g. TVAL6..TVAL0 with 07_H gives a timer period of 2 ms. The timer is started by setting CMDR: ST to logical 1. Then STAR: TAC is set indicating the active timer. To activate the interrupt (MASK, ISTA: TIN) generation, CMDR: TIG must also be set. Now the EPIC generates a periodic interrupt whenever the timer runs out.

Besides this interrupt generation the timer is used for determining the double last look period or generating a proper CFI multiframe synchronization signal. For all three application the period is equal. The timer is stopped by accessing TIMR.

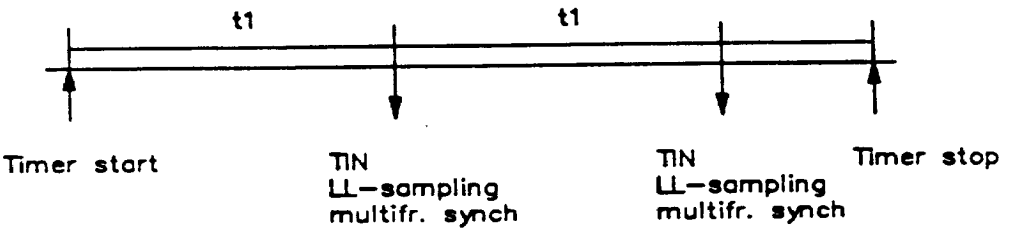


Fig. 2.7: Example of the Timer Function

3. Operational Description

3.1. Principles

Every time slot at the configurable interface is controlled by one control memory entry. Thus, the functionality of every time slot may be chosen from the choices of table 3.1.

Functionality			Application
Transparent	64 kbps 32 kbps 16 kbps	to/from PCM interface	Switching
Transparent	64 kbps	from µP interface	Idle Code
Signaling Channel bits 5..2			IOM C/I channel
Signaling Channel bits 7..2			e.g. analog IOM channel
Signaling Channel bits 7..0			e.g. SLD signaling channel
MFFIFO Channel			Monitor Channel in IOM Feature Control Channel in SLD

Tab. 3.1: CFI Time Slot Functionality Choices

Every channel may be selected in either upstream or downstream direction. The selections for the time slots are nearly independant of each other.

The only restriction is that MFFIFO and signaling channels must be programmed to adjacent time slots, starting with the MFFIFO channel at the even time slot.

The choices of table 3.1 may be programmed independantly of the selected mode.

By programming the time slots the configurable interface may be configured e.g. as a

- transparent PCM Interface (plain switching function)
- IOM interface
- SLD interface.

3.2. Initialization Procedure

For a proper initialization of the EPIC the following procedure is recommended.

3.2.1. Reset

First a reset pulse of at least 4 PDC clock periods has to be applied.

3.2.2. Register Initialization

After reset the register contents are their reset values. In the multiplexed µP access mode, the OMDR is left unchanged (PCM interface and CFI are in standby mode). In the demultiplexed µP access modes OMDR: RBS is switched to logical 1. Now the PCM interface and CFI registers can be initialized to the values necessary in the later application.

3.2.3. CM Initialization

Having thus selected a proper RCL frequency, in the next step the CM is initialized. OMDR: OMS1, OMS0 are still at their reset value 00. Now programming

$$MACR = 70_H$$

initalizes the complete control memory with 256 RCL periods.

It is recommended to select

$$MADR = FF_H$$

for this operation.

After the control memory initialization all CFI channels are unassigned.

3.2.4. CFI Configuration

As a next step CFI is configured. Using the configurable interface without preprocessed channels (as a plain PCM interface) nothing needs to be done at this step. For configuring CFI as

- SLD interface or
- IOM2 interface

the preprocessed channels need to be programmed. Selecting OMDR: OMS1, OMS0 = 10 this procedure is speeded up, since the memory access time is reduced to max. 2.5 RCL cycles from the standard max. 9.5 RCL cycles in normal operation mode (OMDR: OMS1, OMS0 = 11).

The tables 3.2 and 3.3 show the values to be programmed to MADR, MAAR and MACR for these applications.

Function				MACR	MAAR	MADR
Transmit	time slot	2	port 0	$7A_H$	10_H	XVAL
Transmit	time slot	3	port 0	$7B_H$	11_H	FF_H
Transmit	time slot	2	port 1	$7A_H$	12_H	XVAL
Transmit	time slot	3	port 1	$7B_H$	13_H	FF_H
Transmit	time slot	2	port 2	$7A_H$	14_H	XVAL
Transmit	time slot	3	port 2	$7B_H$	15_H	FF_H
Transmit	time slot	2	port 3	$7A_H$	16_H	XVAL
Transmit	time slot	3	port 3	$7B_H$	17_H	FF_H
Transmit	time slot	2	port 4	$7A_H$	18_H	XVAL
Transmit	time slot	3	port 4	$7B_H$	19_H	FF_H
Transmit	time slot	2	port 5	$7A_H$	$1A_H$	XVAL
Transmit	time slot	3	port 5	$7B_H$	$1B_H$	FF_H
Transmit	time slot	2	port 6	$7A_H$	$1C_H$	XVAL
Transmit	time slot	3	port 6	$7B_H$	$1D_H$	FF_H
Transmit	time slot	2	port 7	$7A_H$	$1E_H$	XVAL
Transmit	time slot	3	port 7	$7B_H$	$1F_H$	FF_H
Receive	time slot	6	port 0	$7B_H$	$B0_H$	RVAL
Receive	time slot	7	port 0	$7B_H$	$B1_H$	FF_H
Receive	time slot	6	port 1	$7B_H$	$B2_H$	RVAL
Receive	time slot	7	port 1	$7B_H$	$B3_H$	FF_H
Receive	time slot	6	port 2	$7B_H$	$B4_H$	RVAL
Receive	time slot	7	port 2	$7B_H$	$B5_H$	FF_H
Receive	time slot	6	port 3	$7B_H$	$B6_H$	RVAL
Receive	time slot	7	port 3	$7B_H$	$B7_H$	FF_H
Receive	time slot	6	port 4	$7B_H$	$B8_H$	RVAL
Receive	time slot	7	port 4	$7B_H$	$B9_H$	FF_H
Receive	time slot	6	port 5	$7B_H$	BA_H	RVAL
Receive	time slot	7	port 5	$7B_H$	BB_H	FF_H
Receive	time slot	6	port 6	$7B_H$	BC_H	RVAL
Receive	time slot	7	port 6	$7B_H$	BD_H	FF_H
Receive	time slot	6	port 7	$7B_H$	BE_H	RVAL
Receive	time slot	7	port 7	$7B_H$	BF_H	FF_H

Tab. 3.2: Initialization of the Preprocessed Channels in the CM in a 8 channel SLD Configuration

Function				MACR	MAAR	MADR
Transmit	time slot	2	port 0	78/7AH	08H	XVal
Transmit	time slot	3	port 0	7BH	09H	FFH
Transmit	time slot	2	port 1	78/7AH	0AH	XVal
Transmit	time slot	3	port 1	7BH	0BH	FFH
Transmit	time slot	2	port 2	78/7AH	0CH	XVal
Transmit	time slot	3	port 2	7BH	0DH	FFH
Transmit	time slot	2	port 3	78/7AH	0EH	XVal
Transmit	time slot	3	port 3	7BH	0FH	FFH
Transmit	time slot	6	port 0	78/7AH	18H	XVal
Transmit	time slot	7	port 0	7BH	19H	FFH
Transmit	time slot	6	port 1	78/7AH	1AH	XVal
Transmit	time slot	7	port 1	7BH	1BH	FFH
Transmit	time slot	6	port 2	78/7AH	1CH	XVal
Transmit	time slot	7	port 2	7BH	1DH	FFH
Transmit	time slot	6	port 3	78H/7AH	1EH	XVal
Transmit	time slot	7	port 3	7BH	1FH	FFH
Transmit	time slot	10	port 0	78/7AH	28H	XVal
Transmit	time slot	11	port 0	7BH	29H	FFH
Transmit	time slot	10	port 1	78/7AH	2AH	XVal
Transmit	time slot	11	port 1	7BH	2BH	FFH
Transmit	time slot	10	port 2	78H/7AH	2CH	XVal
Transmit	time slot	11	port 2	7BH	2DH	FFH
Transmit	time slot	10	port 3	78/7AH	2EH	XVal
Transmit	time slot	11	port 3	7BH	2FH	FFH
Transmit	time slot	14	port 0	78/7AH	38H	XVal
Transmit	time slot	15	port 0	7BH	39H	FFH
Transmit	time slot	14	port 1	78H/7AH	3AH	XVal
Transmit	time slot	15	port 1	7BH	3BH	FFH
Transmit	time slot	14	port 2	78/7AH	3CH	XVal
Transmit	time slot	15	port 2	7BH	3DH	FFH
Transmit	time slot	14	port 3	78/7AH	3EH	XVal
Transmit	time slot	15	port 3	7BH	3FH	FFH
Transmit	time slot	18	port 0	78/7AH	48H	XVal
Transmit	time slot	19	port 0	7BH	49H	FFH
Transmit	time slot	18	port 1	78/7AH	4AH	XVal
Transmit	time slot	19	port 1	7BH	4BH	FFH
Transmit	time slot	18	port 2	78/7AH	4CH	XVal
Transmit	time slot	19	port 2	7BH	4DH	FFH
Transmit	time slot	18	port 3	78/7AH	4EH	XVal
Transmit	time slot	19	port 3	7BH	4FH	FFH
Transmit	time slot	22	port 0	78/7AH	58H	XVal
Transmit	time slot	23	port 0	7BH	59H	FFH
Transmit	time slot	22	port 1	78/7AH	5AH	XVal
Transmit	time slot	23	port 1	7BH	5BH	FFH
Transmit	time slot	22	port 2	78/7AH	5CH	XVal
Transmit	time slot	23	port 2	7BH	5DH	FFH
Transmit	time slot	22	port 3	78H/7AH	5EH	XVal
Transmit	time slot	23	port 3	7BH	5FH	FFH

Function				MACR	MAAR	MADR
Transmit	time slot	26	port 0	78/7A$_H$	68$_H$	XVal
Transmit	time slot	27	port 0	7B$_H$	69$_H$	FF$_H$
Transmit	time slot	26	port 1	78/7A$_H$	6A$_H$	XVal
Transmit	time slot	27	port 1	7B$_H$	6B$_H$	FF$_H$
Transmit	time slot	26	port 2	78/7A$_H$	6C$_H$	XVal
Transmit	time slot	27	port 2	7B$_H$	6D$_H$	FF$_H$
Transmit	time slot	26	port 3	78/7A$_H$	6E$_H$	XVal
Transmit	time slot	27	port 3	7B$_H$	6F$_H$	FF$_H$
Transmit	time slot	30	port 0	78/7A$_H$	78$_H$	XVal
Transmit	time slot	31	port 0	7B$_H$	79$_H$	FF$_H$
Transmit	time slot	30	port 1	78/7A$_H$	7A$_H$	XVal
Transmit	time slot	31	port 1	7B$_H$	7B$_H$	FF$_H$
Transmit	time slot	30	port 2	78/7A$_H$	7C$_H$	XVal
Transmit	time slot	31	port 2	7B$_H$	7D$_H$	FF$_H$
Transmit	time slot	30	port 3	78/7A$_H$	7E$_H$	XVal
Transmit	time slot	31	port 3	7B$_H$	7F$_H$	FF$_H$
Receive	time slot	2	port 0	78$_H$/7A$_H$	88$_H$	FF$_H$
Receive	time slot	3	port 0	70$_H$/7A$_H$	89$_H$	FF$_H$
Receive	time slot	2	port 1	78$_H$/7A$_H$	8A$_H$	FF$_H$
Receive	time slot	3	port 1	70$_H$/7A$_H$	8B$_H$	FF$_H$
Receive	time slot	2	port 2	78$_H$/7A$_H$	8C$_H$	FF$_H$
Receive	time slot	3	port 2	70$_H$/7A$_H$	8D$_H$	FF$_H$
Receive	time slot	2	port 3	78$_H$/7A$_H$	8E$_H$	FF$_H$
Receive	time slot	3	port 3	70$_H$/7A$_H$	8F$_H$	FF$_H$
Receive	time slot	6	port 0	78$_H$/7A$_H$	98$_H$	FF$_H$
Receive	time slot	7	port 0	70$_H$/7A$_H$	99$_H$	FF$_H$
Receive	time slot	6	port 1	78$_H$/7A$_H$	9A$_H$	FF$_H$
Receive	time slot	7	port 1	70$_H$/7A$_H$	9B$_H$	FF$_H$
Receive	time slot	6	port 2	78$_H$/7A$_H$	9C$_H$	FF$_H$
Receive	time slot	7	port 2	70$_H$/7A$_H$	9D$_H$	FF$_H$
Receive	time slot	6	port 3	78$_H$/7A$_H$	9E$_H$	FF$_H$
Receive	time slot	7	port 3	70$_H$/7A$_H$	9F$_H$	FF$_H$
Receive	time slot	10	port 0	78$_H$/7A$_H$	A8$_H$	FF$_H$
Receive	time slot	11	port 0	70$_H$/7A$_H$	A9$_H$	FF$_H$
Receive	time slot	10	port 1	78$_H$/7A$_H$	AA$_H$	FF$_H$
Receive	time slot	11	port 1	70$_H$/7A$_H$	AB$_H$	FF$_H$
Receive	time slot	10	port 2	78$_H$/7A$_H$	AC$_H$	FF$_H$
Receive	time slot	11	port 2	70$_H$/7A$_H$	AD$_H$	FF$_H$
Receive	time slot	10	port 3	78$_H$/7A$_H$	AE$_H$	FF$_H$
Receive	time slot	11	port 3	70$_H$/7A$_H$	AF$_H$	FF$_H$

Function				MACR	MAAR	MADR
Receive	time slot	14	port 0	78H/7AH	B8H	FFH
Receive	time slot	15	port 0	70H/7AH	B9H	FFH
Receive	time slot	14	port 1	78H/7AH	BAH	FFH
Receive	time slot	15	port 1	70H/7AH	BBH	FFH
Receive	time slot	14	port 2	78H/7AH	BCH	FFH
Receive	time slot	15	port 2	70H/7AH	BDH	FFH
Receive	time slot	14	port 3	78H/7AH	BEH	FFH
Receive	time slot	15	port 3	70H/7AH	BFH	FFH
Receive	time slot	18	port 0	78H/7AH	C8H	FFH
Receive	time slot	19	port 0	70H/7AH	C9H	FFH
Receive	time slot	18	port 1	78H/7AH	CAH	FFH
Receive	time slot	19	port 1	70H/7AH	CBH	FFH
Receive	time slot	18	port 2	78H/7AH	CCH	FFH
Receive	time slot	19	port 2	78H/7AH	CDH	FFH
Receive	time slot	18	port 3	70H/7AH	CEH	FFH
Receive	time slot	19	port 3	78H/7AH	CFH	FFH
Receive	time slot	22	port 0	78H/7AH	D8H	FFH
Receive	time slot	23	port 0	70H/7AH	D9H	FFH
Receive	time slot	22	port 1	78H/7AH	DAH	FFH
Receive	time slot	23	port 1	70H/7AH	DBH	FFH
Receive	time slot	22	port 2	78H/7AH	DCH	FFH
Receive	time slot	23	port 2	70H/7AH	DDH	FFH
Receive	time slot	22	port 3	78H/7AH	DEH	FFH
Receive	time slot	23	port 3	70H/7AH	DFH	FFH
Receive	time slot	26	port 0	78H/7AH	E8H	FFH
Receive	time slot	27	port 0	70H/7AH	E9H	FFH
Receive	time slot	26	port 1	78H/7AH	EAH	FFH
Receive	time slot	27	port 1	70H/7AH	EBH	FFH
Receive	time slot	26	port 2	78H/7AH	ECH	FFH
Receive	time slot	27	port 2	78H/7AH	EDH	FFH
Receive	time slot	26	port 3	70H/7AH	EEH	FFH
Receive	time slot	27	port 3	78H/7AH	EFH	FFH
Receive	time slot	30	port 0	70H/7AH	F8H	FFH
Receive	time slot	31	port 0	78H/7AH	F9H	FFH
Receive	time slot	30	port 1	70H/7AH	FAH	FFH
Receive	time slot	31	port 1	78H/7AH	FBH	FFH
Receive	time slot	30	port 2	70H/7AH	FCH	FFH
Receive	time slot	31	port 2	78H/7AH	FDH	FFH
Receive	time slot	30	port 3	70H/7AH	FEH	FFH
Receive	time slot	31	port 3	78H/7AH	FFH	FFH

Tab. 3.3: **Initialization of the Preprocessed Channels in the CM for a 32 channel IOM2 Configuration**

3.2.5. Initialization of the Tristate Field

Now the data memory tristate field should be initialized so that all PCM output channels are tristated. To do this it is necessary to change to the normal operation mode by programming OMO0: OMS1, OMS0 = 11. Then

MADR = 00_H

MACR = 68_H

is programmed resulting in the reset of the complete tristate field within 1035 RCL periods.

3.2.6. Activating the EPIC

Finally the EPIC is brought into operation by switching the PCM interface and CFI from standby to low impedance (OMDR: PSB = 1, OMDR: CSB = 1).

4. DETAILED REGISTER DESCRIPTION

The following symbols are used throughout chapter 4

x... don't care

u... used to ensure the intended function

n... not used. It has to be set to logical 0 in write accesses but may be switched by the EPIC to either logical level in read accesses.

Group	Register Name	Access Write(WR) Read(RD)	µP Interface Mode mux. AD7..AD0	demux. A3..A0/RBS	Reset Value	Register Content
PCM	PMOD	RD/WR	20H	0H/1	00	PCM Mode Register
	PBNR	RD/WR	22H	1H/1	FF	PCM Bit Number Register
	POFD	RD/WR	24H	2H/1	00	PCM Offset Downstream Register
	POFU	RD/WR	26H	3H/1	00	PCM Offset Upstream Register
	PCSR	RD/WR	28H	4H/1	00	PCM Clock Shift Register
	PICM	RD/WR	2AH	5H/1	-	PCM Input Comparison Mismatch Register
CFI	CMD1	RD/WR	2CH	6H/1	00	CFI Mode Register 1
	CMD2	RD/WR	2EH	7H/1	00	CFI Mode Register 2
	CBNR	RD/WR	30H	8H/1	FF	CFI Bit Number Register
	CTAR	RD/WR	32H	9H/1	00	CFI Time Slot Adjustment Register
	CBSR	RD/WR	34H	AH/1	00	CFI Bit Shift Register
	CSCR	RD/WR	36H	BH/1	00	CFI Subchannel Register
MAR	MACR	RD/WR	00H	0H/0	-	Memory Access Control Register
	MAAR	RD/WR	02H	1H/0	-	Memory Access Address Register
	MADR	RD/WR	04H	2H/0	-	Memory Access Data Register

Group	Register Name	Access Write(WR) Read(RD)	µP Interface Mode mux. AD7..AD0	µP Interface Mode demux. A3..A0/RBS	Reset Value	Register Content
STR	STDA	RD/WR	06H	3H/0	–	Synchron Transfer Data Register A
	STDB	RD/WR	08H	4H/0	–	Synchron Transfer Data Register B
	SARA	RD/WR	0AH	5H/0	–	Synchron Transfer Receive Address Register A
	SARB	RD/WR	0CH	6H/0	–	Synchron Transfer Receive Address Register B
	SAXA	RD/WR	0EH	7H/0	–	Synchron Transfer Transmit Address Register A
	SAXB	RD/WR	10H	8H/0	–	Synchron Transfer Transmit Address Register B
	STCR	RD/WR	12H	9H/0	00	Synchron Transfer Control Register
MFCH	MFAIR	RD	14H	AH/0	Undef.	MF Channel Active Indication Register
	MFSAR	WR	14H	AH/0	Undef.	MF Channel Subscriber Address Register
	MFFIFO	RD/WR	16H	BH/0	Empty	MF Channel FIFO
SCR	C/I FIFO	RD	18H	CH/0	Validity 0	Signalling Channel FIFO
	TIMR	WR	18H	CH/0	00	Timer Register
	STAR	RD	1AH	DH/0	05	Status Register
	CMDR	WR	1AH	DH/0	00	Command Register
	ISTA	RD	1CH	EH/0	00	Interrupt Status Register
	MASK	WR	1CH	EH/0	00	Mask Register
	OMDR	RD/WR	1EH/3EH	FH/X	00	Operation Mode Register
	VNSR	RD	3AH	DH/1		Version Number Register

Tab. 4.1: Register Set

Note: In the multiplexed µP interface mode AD0 is not used for address coding.

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4.1. PCM Interface (PCM) Registers

4.1.1. PCM Mode Register (PMOD)

Access in the multiplexed µP interface mode: Read or write, address: 20H
Access in a demultiplexed µP interface mode: Read or write, address 0H, OMDR:RBS = 1
Reset value: 00H

bit 7							bit0
PMD1	PMD0	PCR	PSM	AIS1	AIS0	AIC1	AIC0

PMD1...PMD0 ... PCM Mode 1 and 0; these bits define the PCM mode according to table 4.2. The ports used in the selected PCM mode are stated in table 4.3.

PMD1	PMD0	PCM Mode	Port Count	Data Rate [kbps] min	Data Rate [kbps] max	Data Rate Stepping [kbps]
0	0	0	4	256	2048	8
0	1	1	2	512	4096	16
1	0	2	1	1024	8192	32

Tab. 4.2: Modes at the PCM Interface

PCR... PCM Clock Rate; a logical 0 selects the PCM interface for single clock rate operation, a logical 1 for double clock rate operation. In single clock rate operation, the PCM interface of the EPIC is supplied with clock and data of the same frequency; in double clock rate operation the clock frequency is twice the data frequency. In PCM mode 2,only single clock rate operation is feasable.

PSM ... PCM Synchronization Mode; the rising edge of the PFS signal synchronizes the PCM frame. The PFS signal is evaluated with the rising clock edge (logical 1) or with the falling clock edge (logical 0). Also refer to figure 4.1.

AIS1..AIS0 ... Alternative Input Selection 1 and 0; these bits determine the relationship between the physical pins and the logical port numbers used to program the switching function of the EPIC, as shown in table 4.3.

	Port 0			Port 1			Port 2			Port 3		
Mode	PxD0	TxD0	$\overline{TSC0}$	PxD1	TxD1	$\overline{TSC1}$	PxD2	TxD2	$\overline{TSC2}$	PxD3	TxD3	$\overline{TSC3}$
0	IN0	OUT 0	Val0	IN1	Out1	Val1	IN2	OUT2	Val2	IN3	OUT3	Val3
1	IN0(AIS0 = 1)	OUT0	Val0	IN0(AIS0 = 0)	tristate	AIS0	IN1(AIS1 = 1)	OUT1	Val1	IN1(AIS1 = 0)	tristate	AIS1
2	tristate	OUT	Val	tristate	tristate	AIS0	IN(AIS1 = 1)	undef.	undef.	IN(AIS1 = 0)	tristate	AIS1

Tab. 4.3: PCM Pin Configuration

Note: The $\overline{TSC}$ pins output either information about the validity of the relevant TxD output (VAL, active low) or the content of the respective AIS bit.

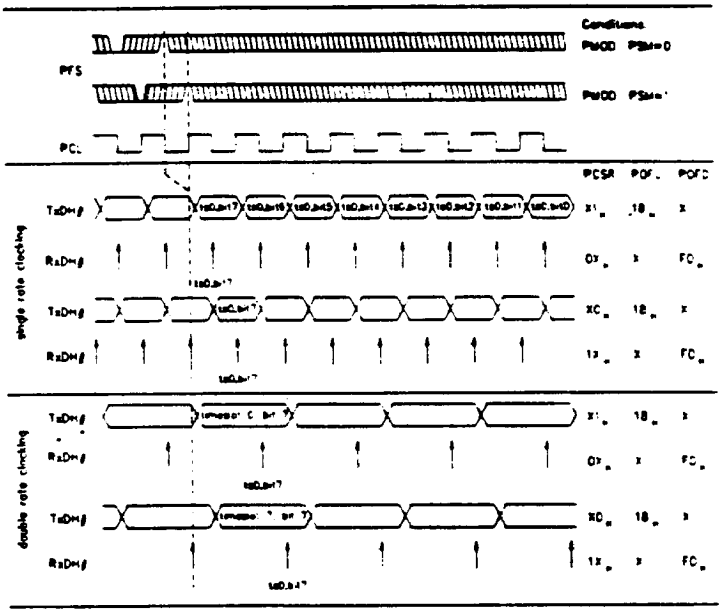

Fig. 4.1: Upstream and Downstream Timing at the PCM Interface for Single and Double Rate Clocking.

Setting AIS0 or AIS1 in PCM mode 0 may result in an undefined operational behaviour and should therefore be avoided.

AIC1..AIC0 ... Alternative Input Comparison 1 and 0; these bits control the input comparison function of the EPIC. If AIC1 is programmed to logical 1, the inputs of port 2 and 3 are compared in PCM mode 1 and 2. If AIC0 is programmed to logical 1, the inputs of port 0 and 1 are compared in PCM mode 1. A logical 0 dis-ables the respective comparison function.

4.1.2. Bit Number per PCM Frame (PBNR)

Access in the multiplexed µP interface mode: Read or write, address: 22_H
Access in a demultiplexed µP interface mode: Read or write, address 1_H, OMDR:RBS = 1
Reset value: FF_H

bit 7							bit0
BNF7	BNF6	BNF5	BNF4	BNF3	BNF2	BNF1	BNF0

BNF7...BNF0 ... Bit Number per PCM Frame: these bits denote the number of bits constituing a PCM frame -1. BNF0 is the least significant bit, BNF7 the most significant bit. In PCM mode 0 the EPIC expects the number of bits as programmed to BNF7...BNF0, in PCM mode 1 twice and in PCM mode 2 four times this number to be contained in one frame.

4.1.3. PCM Offset Downstream Register (POFD)

Access in the multiplexed µP interface mode: Read or write, address: 24_H
Access in a demultiplexed µP interface mode: Read or write, address 2_H, OMDR:RBS = 1
Reset value: 00_H

bit 7							bit0
OFD9	OFD8	OFD7	OFD6	OFD5	OFD4	OFD3	OFD2

OFD9...OFD2 ... Offset Downstream bit 9...2; these bits together with PCSR:OFD1...0 determine the offset of the PCM downstream frame. The positive edge of PFS marks the bit number in the downstream frame (BND) according to the following formulas: (BND = 1: 1st bit in the frame).

PCM mode 0: $BND = MOD_{256}\ (17_D + (OFD9...OFD2)_B)$
PCM mode 1: $BND = MOD_{512}\ (33_D + (OFD9...OFD1)_B)$
PCM mode 2: $BND = MOD_{1024}\ (65_D + (OFD9...OFD0)_B)$

This behaviour is also shown in figure 4.2

The stated formulas are valid for a bit number count of 256, 512 or 1024 in PCM mode 0,1 or 2, resepectively. For a lower bit number count the decimal summands have to increased by the number of bits missing. E.g., for a frame consisting of 24 time slots (PCM mode 0) OFD has to be programmed 10110000. Then the positive PFS edge mark bit 7 of time slot 0.

4.1.4. PCM Offset Upstream Register (POFU)

Access in the multiplexed µP interface mode: Read or write, address: 26_H
Access in a demultiplexed µP interface mode: Read or write, address 3_H, OMDR:RBS = 1
Reset value: 00_H

bit 7							bit 0
OFU9	OFU8	OFU7	OFU6	OFU5	OFU4	OFU3	OFU2

OFU7...OFU0 ... Offset upstream bits 9...2; these bits together with PCSR:OFU1...OFU0 determine the offset of the PCM upstream frame. The positive PFS edge marks the bit number in the upstream frame (BNU) according to the following formulas (BNU = 1: 1st bit in frame)

PCM mode 0: $MOD_{256}\ (BNU_D + 23) = (OFU9...OFU2)_B$
PCM mode 1: $MOD_{512}\ (BNU_D + 47) = (OFU9...OFU1)_B$
PCM mode 2: $MOD_{1024}\ (BNU_D + 95) = (OFU9...OFU0)_B$

This behaviour is also shown in figure 4.2

4.1.5. PCM Clock Shift Register (PCSR)

Access in the multiplexed µP interface mode: Read or write, address: 28_H
Access in a demultiplexed µP interface mode: Read or write, address 4_H, OMDR:RBS = 1
Reset value: 00_H

bit 7							bit0
0	OFD1	OFD0	DRE	0	OFU1	OFU0	URE

OFD1...OFD0 ... Offset downstream bits 1...0; see POFD register. In PCM mode 0, both bits and in PCM mode 1, OFD0 need to be fixed to logical 0.

DRE ... Downstream rising edge; the PCM data is sampled with the rising edge (DRE = 1) or the falling edge (DRE = 0) of PCL, as shown in figure 4.1.

OFU1...OFU0... Offset upstream bits 1...0; see POFU register. In PCM mode 0, both bits and in PCM mode 1, OFU0 need to be fixed to logical 0

URE ... Upstream rising edge; the PCM data is transmitted with the rising edge (URE = 1) or the falling edge (URE = 0) of PCL, as shown in figure 4.1.

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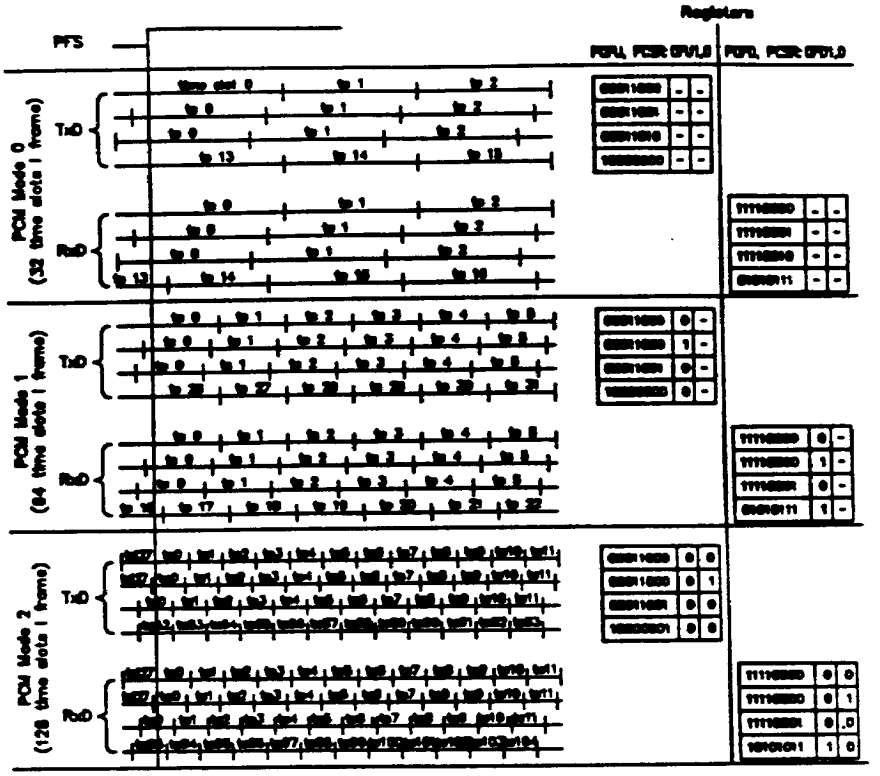

Fig. 4.2: PCM Interface Framing Offset

4.1.6. PCM Input Comparison Mismatch (PICM)

Access in the multiplexed µP interface mode: Read, address: $2A_H$

Access in a demultiplexed µP interface mode: Read or write, address 5_H, OMDR:RBS = 1

bit 7							bit 0
IPN	TSN6	TSN5	TSN4	TSN3	TSN2	TSN1	TSN0

IPN ... Input Pair Number; this bit denotes the pair of ports, where a bit mismatch of the inputs occured. A logical 0 indicates a mismatch between ports 0 and 1, a logical 1 between ports 2 and 3.

TSN6...TSN0 ... These bits contain information, when a mismatch occured as can be seen from table 4.4.

PCM Mode	Time Slot Identification	Bit Identification
2	TSN6..TSN0 + 8	-
1	TSN6...TSN1 + 4	TSN0 = 1 : bits 0...3 TSN0 = 0 : bits 4...7
0	TSN6...TSN2 + 2	TSN1..TSN0 = 11: bits 0...1 TSN1..TSN0 = 10 : bits 2...3 TSN1..TSN0 = 01: bits 4...5 TSN1..TSN0 = 00 : bits 6...7

Tab. 4.4: Identification of the Differing PCM Data

4.2. Configurable Interface Registers (CFI)

4.2.1. Configurable Interface Mode Register 1 (CMD1)

Access in the multiplexed µP interface mode: Read or write, address: 2C$_H$
Access in a demultiplexed µP interface mode: Read or write, address 6$_H$, OMDR:RBS = 1
Reset value: 00$_H$

bit 7							bit 0
CSS	CSM	CSP1	CSP0	CMD1	CMD0	CIS1	CIS0

CSS ... Clock Source Selection: A logical 0 selects PCL as clock and PFS as framing source for the configurable interface. Clock and framing signals derived from these sources are output at the DCL and FSC pins (OMDR:CSB = 1). A logical 1 selects DCL as clock and FSC as framing signal source for the configurable interface.

CSM ... Configurable Interface Synchronization Mode; the positive FSC transition synchronizes the CFI frame. The FSC signal is evaluated at every positive clock slope (logical 1) or at every negative clock slope (logical 0). If CSS = 0 is selected CSM should be programmed identical to PMOD:PSM. Also refer to figure 4.5.

CSP1..CSP0 ... Clock Source Prescaler 1,0; the clock source frequency is divided by the values listed in the table below to obtain the device reference clock.

CSP1	CSP0	Prescalor Divisor
0	0	2
0	1	1.5
1	0	1
1	1	Not Allowed

Tab. 4.5: Prescalor Divisors

CMD1,0 ... CFI Mode 1,0; these bits define the CFI mode according to table 4.6.

CMD1	CMD0	CFI Mode	Port Count/ device setup	Data Rate (DR) [kbps] min	max	Necessary Reference Clock (RCL) DR = actual data rate	Possible DCL Output Frequencies
1	1	3	8 bidir	128	1024	4*DR	DR, 2*DR
0	0	0	4 duplex	128	2048	2*DR	DR, 2*DR
0	1	1	2 duplex	128	4096	DR	DR
1	0	2	1 duplex	128	8192	DR	DR

Tab. 4.6: Configurable Interface Modes

CIS1,0 ... CFI alternative input selection; these bits determine the relationship between the physical pins and the logical port numbers used to program the switching function of the EPIC, as shown in table 4.7.

CFI Mode	DD0	DU0	DD1	DU1	DD2	DU2	DD3	DU3
0	OUT0	IN0	OUT1	IN1	OUT2	IN2	OUT3	IN3
1	OUT0	IN0(CIS0 = 0)	OUT1	IN1(CIS1 = 0)	tristate	IN0(CIS0 = 1)	tristate	IN1(CIS1 = 1)
2	OUT	IN(CIS0 = 0)	tristate	not active	tristate	IN(CIS0 = 1)	tristate	not active
3	I/O0	I/O4	I/O1	I/O5	I/O2	I/O6	I/O3	I/O7

Tab. 4.7: CFI Pin Configuration

4.2.2. Configurable Interface Mode Register 2 (CMD2)

Access in the multiplexed µP interface mode: Read or write, address: $2E_H$

Access in a demultiplexed µP interface mode: Read or write, address 7_H, OMDR:RBS = 1

Reset value: 00_H

bit 7							bit 0
FC2	FC1	FC0	COC	CXF	CRR	CBN9	CBN8

FC2...FC0 ... Framing Output Control; for CMD1:CSS = 0 and OMDR:CSB = 0, these bits determine the type of generated CFI framing signal according to figure 4.3.

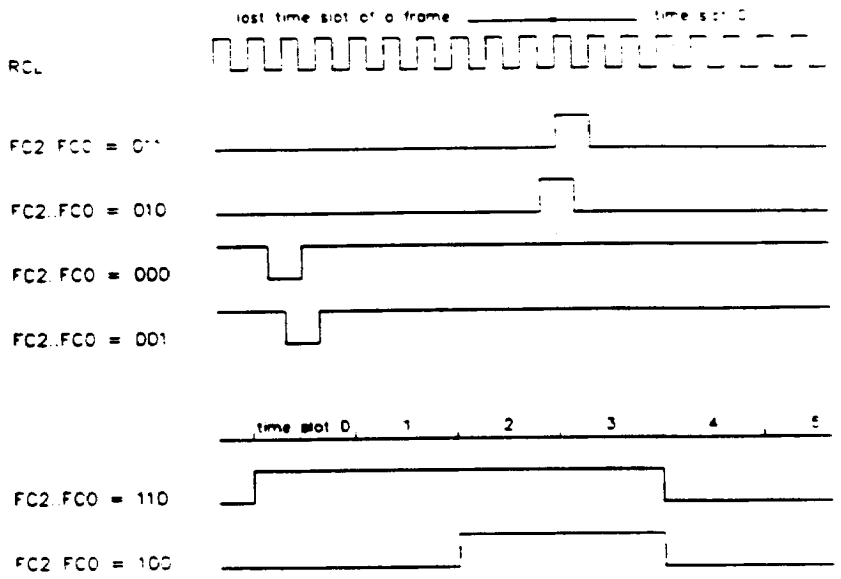

Fig. 4.3: FSC Framing Signal Generation

Table 4.8 states the main applications, the different selections are used in.

FC2	FC1	FC0	FC Mode	Main Applications
0	0	0	0	IOM 1 mux. mode
0	0	1	1	PCM mode
0	1	0	2	PCM mode
0	1	1	3	IOM 2
1	0	0	4	2 ISAC-S per SLD Port
1	0	1	5	reserved
1	1	0	6	IOM 2 or bidirectional applications
1	1	1	7	software timed multiplexed applications

Tab. 4.8: Applications of the Framing Control Modes

The FSC signal in FC mode 7 for software timed multiplexed applications is derived from the FC modes 3 and 6. As shown in figure 4.4, setting CMDR:ST1 starts a cyclic multiplexing process. Its period is defined by the content of TIMR. After each of these periods the EPIC issues one FSC pulse of FC mode. 3, in all other frames the framing pulse of FC mode 6. Figure 4.4 shows this behaviour, assuming TIMR:TVAL6...TVAL0 = 0000010 and CFI mode 0.

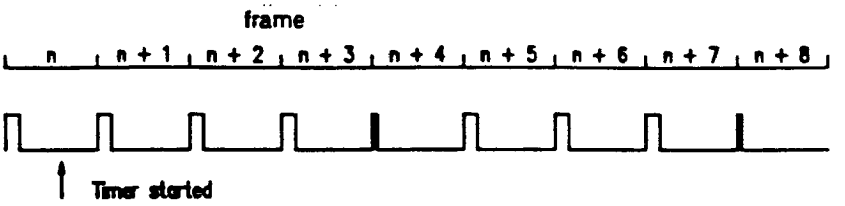

Fig. 4.4: FSC output signal in FSC mode 7

COC ... Clock Output Control for CMD1:CSS = 0; a logical 1 selects the EPIC to output a DCL clock signal with a frequency of twice the CFI data rate (double rate clock, CFI modes 0 and 3 only), a logical 0 produces a single rate clock. Also see figure 4.5.

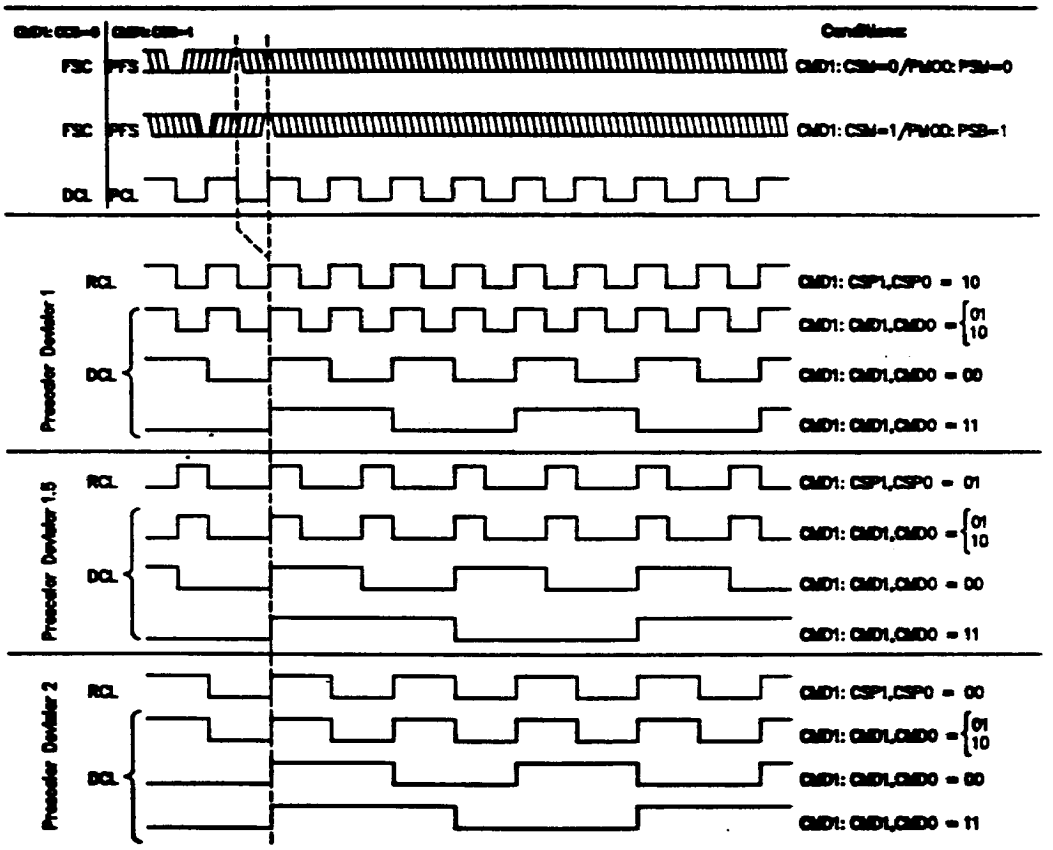

Fig. 4.5: Data Clock and Reference Clock for the different Prescaler Divisors at the CFI.

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CXF ... CFI Transmit on Falling Edge; CFI data is transmitted with the rising edge (CXF = 0) or falling edge (CXF = 1) of the reference clock, as shown in figure 4.5.

CRR ... CFI Receive on Rising Edge; CFI data is sampled with the falling (CRR = 0) or rising edge (CRR = 1) of the reference clock (see figure 4.6). In CFI mode 3, CRR has to be set to logical 0.

CBN9...CBN8... CFI Bit Number 9...8; these bits together with CBNR:CBN7...0 hold the number of bits per CFI frame (see CBNR).

4.2.3. Configurable Interface Bit Number Register (CBNR)

Access in the multiplexed µP interface mode: Read or write, address: 30_H
Access in a demultiplexed µP interface mode: Read or write, address 8_H, OMDR:RBS = 1
Reset value: FF_H

bit 7							bit 0
CBN7	CBN6	CBN5	CBN4	CBN3	CBN2	CBN1	CBN0

CBN7...CBN0 ... CFI Bit Number 7...0; together with CMD2:CBN9,CBN8, these bits hold the bit count of a CFI frame minus 1 bit. CBN9 is the most, CBN0 the least significant bit. E.g., setting CBN9...CBN0 to $3FF_H$, the CFI frame consists of 1024 bits.

4.2.4. Configurable Interface Time Slot Adjustment Register (CTAR)

Access in the multiplexed µP interface mode: Read or write, address: 32_H
Access in a demultiplexed µP interface mode: Read or write, address 9_H, OMDR:RBS = 1
Reset value: 00_H

bit 7							bit 0
0	TSN6	TSN5	TSN4	TSN3	TSN2	TSN1	TSN0

TSN6...TSN0 ... Time Slot Number; the framing signal at the configurable interface marks the downstream time slot numbered according to below formula, if FSC is used as input to the device (i. e. CMD1: CSS = 1):

Time slot Number Downstream = (TSN6...TSN0 - 10)$_8$

Also refer to figure 4.6

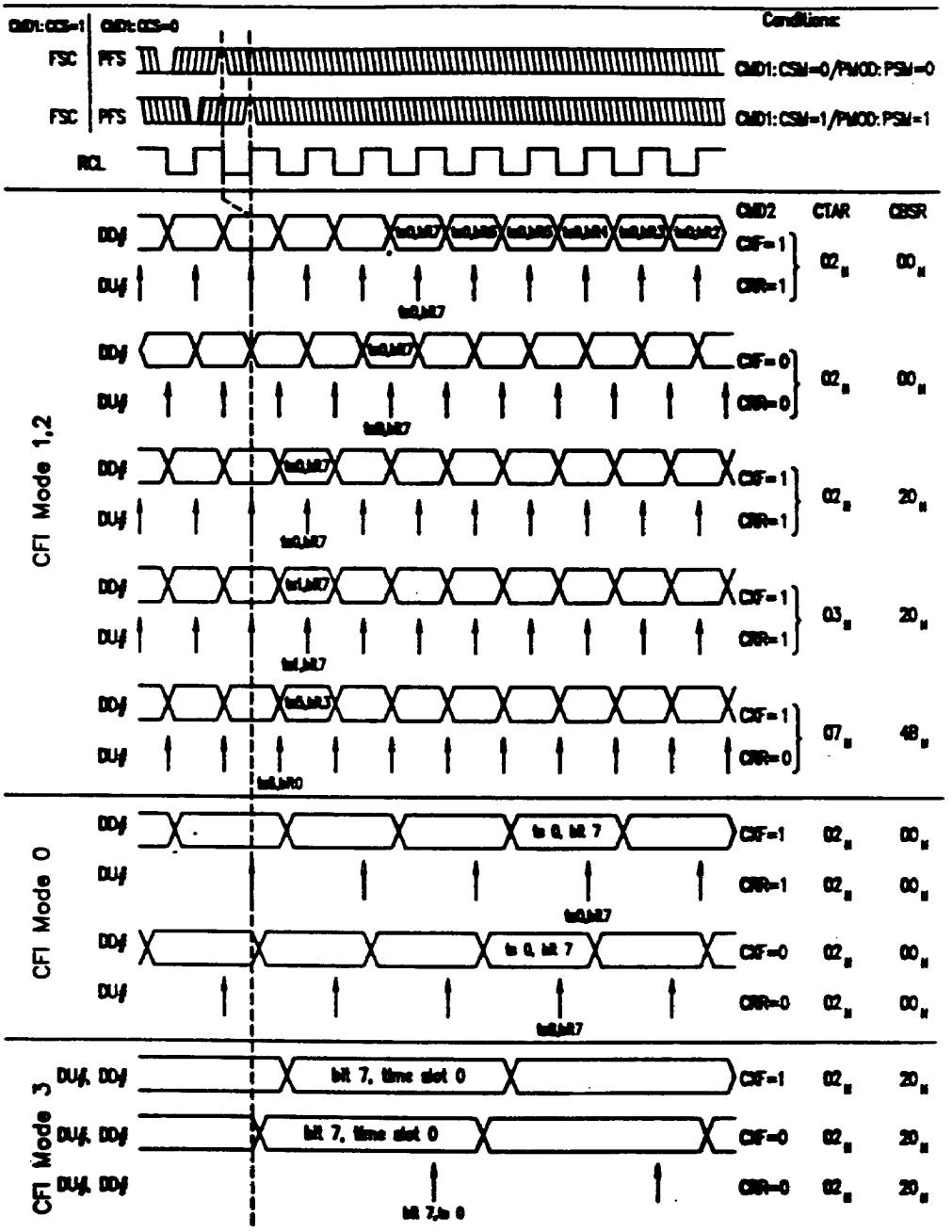


Fig. 4.6: Configurable Interface Bit Timing

4.2.5. Configurable Interface Bit Shift Register (CBSR)

Access in the multiplexed µP interface mode: Read or write, address: 34_H

Access in a demultiplexed µP interface mode: Read or write, address A_H, OMDR:RBS = 1

Reset value: 00_H

bit 7							bit 0
0	CDS2	CDS1	CDS0	CUS3	CUS2	CUS1	CUS0

CDS2...CDS0 ... CFI Downstream Bit Shift 2...0; the framing signal at the configurable interface marks the bit numbered according to the following formula. If CBSR: CUS(3:0) = 0H, it also marks the bit number upstream:

Bit Number Downstream (Upstream) = $(111 - CDS2...CDS0)_B$

This behaviour can also be seen in figure 4.6

CUS3...CUS0 ... CFI Upstream Bit Shift 3...0; using these bits the upstream frame may be shifted by up to 15 clock steps relative to the downstream frame. Thus it is also shifted relative to the CFI-Framesynchronization Signal in both modes of clock source selection (CMD1:CSS). Figure 4.7 outlines this function.

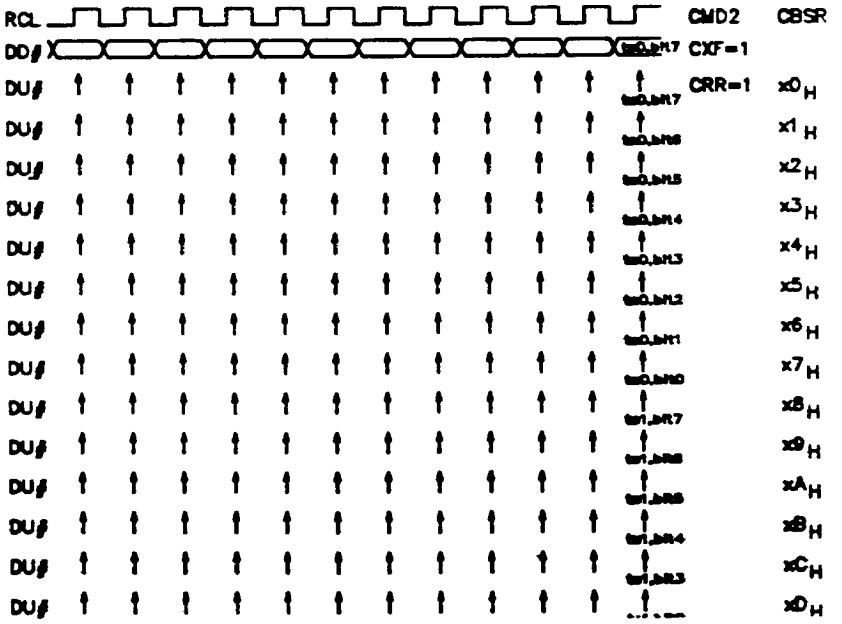


Fig.4.7.: CFI Upstream Bit Shifting

4.2.6. Configurable Interface Subchannel Register (CSCR)

Access in the multiplexed µP interface mode: Read or write, address: 36_H
Access in a demultiplexed µP interface mode: Read or write, address B_H, OMDR:RBS = 1
Reset value: 00_H

bit 7							bit 0
SC31	SC30	SC21	SC20	SC11	SC10	SC01	SC00

SC#1...SC#0 ... Subchannel Control for the logical Port #;these bits select the subtime slot position of the CFI Port No. # to be handled according to the CM entries.

Only one channel may be mapped to one CFI time slot.

E.g., programming SC01, SC00 to 00, 16 kbps channels consisting of the bits 6 and 7 of an 8 bit time slot, 32 kbps time slots consisting of the bits 4 and 7 of an 8 bit time slot or a full 64 kbps time slots may be handled at the CFI port 0.

SC#1	SC#0	Data Rate		
		64 kbps	32 kbps	16kbps
1	1	0...7	0...3	0...1
1	0	0...7	4...7	2...3
0	1	0...7	0...3	4...5
0	0	0...7	4...7	6...7

Tab. 4.9: CFI Subchannel Assignements

For the CFi modes 2 and 1 the following restrictions apply:

CFI mode 2: SC31 = SC21 = SC11 = SC01;
SC30 = SC20 = SC10 = SC00;

CFI mode 1: SC31 = SC11;
SC30 = SC10;
SC21 = SC01;
SC20 = SC00;

In CFI mode 3, SC31 and SC30 control the ports 3 and 7, SC21 and SC20 ports 2 and 6, SC11 and SC10 ports 1 and 5 and SC00 and SC01 ports 0 and 4.

4.3. Memory Access Registers (MAR)

The memory access registers are used to

- directly access the data memory
- directly access the control memory
- program the switching function
- select the signalling application

One of these specific functions is selected by programming the memory access control register.

The address of the memory encodes the time slot and logical port numbers, the data memory addresses (table 4.16) for the channels at the PCM interface, the control memory addresses (table 4.17) for the channels of CFI.

The EPIC performs a memory access specified by the actual content of the three memory access registers following every write operation at MACR. This access takes at most 9.5 reference clock cycles.

4.3.1. Memory Access Control Register (MACR)

Access in the multiplexed µP interface mode: Read and write, address: 00_H

Access in a demultiplexed µP interface mode: Read or write, address 0_H, OMDR:RBS = 0

A write access to this register initiates the memory access.

bit 7 bit 0

RWS	MOC3	MOC2	MOC1	MOC0/ CMC3	CMC2	CMC1	CMC0

RWS ... Read/Write Select; a logical 1 selects the EPIC for a read, a logical 0 for a write operation on the control or data memories.

MOC3...MOC0 ... Memory Operation Code; identifies type and destination of the memory operation according to the below tables.

PCM Interface Data Rate and Subchannel Selection Idle Codes

MOC3	MOC2	MOC1	MOC0	Transferred Bits	Channel Bandwith
0	0	0	0	-	-
0	0	0	1	Bits 7..0	64 kbps
0	0	1	1	Bits 7..4	32 kbps
0	0	1	0	Bits 3..0	32 kbps
0	1	1	1	Bits 7..6	16 kbps
0	1	1	0	Bits 5..4	16 kbps
0	1	0	1	Bits 3..2	16 kbps
0	1	0	0	Bits 1..0	16 kbps

Tab. 4.10: Codes for the Selection of the PCM Channel Bandwidth and Subchannel Position

Using these codes in write accesses the MADR content is transferred to the data memory subject to the subchannel selection (e.g. PCM idle code programming). The code 0010 transfers MADR:MD3...MD0 to the data memory. These bits will then be output at the PCM interface in the bit 3...bit 0 positions of the chosen time slot (MAAR).

In read accesses the complete data memory location content will be copied to MADR for all these codes.

Tristate Codes

MOC3	MOC2	MOC1	MOC0	Function
1	1	0	0	Single Channel Tristate Control
1	1	0	1	Tristate Control Reset

Tab. 4.11: Tristate Codes

Programming one of these codes, MADR:MD3...MD0 is copied to a selected position (1100) or all positions (1101) of the upstream data memory tristate field. MD3 controls the PCM interface tristate function of the bits 7...6, MD2 of bits 5...4, MD1 of bits 3...2 and MD0 of bits 1...0 (high impedance = 0, low impedance = 1).

Resetting the complete DM tristate field takes 1035 reference clock periods.

CM Codes

MOC 3	2	1	0	Transferred Bits	Function
1	0	0	1	MADR:MD7..MD0	Control Memory Access
1	1	1	X	MADR:MD7..MD0,MACR:CMC3..CMC0	see text

Tab. 4.12: CM Codes

These codes are used to enter or retrieve information to or from a CM location. Either the 8 bits of MADR (1001) or these 8 bits plus the 4 bits of MACR:CMC3...CMC0 (111x) are written to the CM.

The code 1001 is used to write/read data to/from the 8 bit data field of the addressed CM location. It may be used to enter a CFI idle code. 64 kbps is the only possible CFI idle code bandwidth.

The code 111x is applicable to program a connection or the signaling function of the EPIC with one memory access. To program a connection, MADR contains the PCM interface channel, MAAR the CFI channel and MACR: CMC3 ... 0 the channel bandwidth control information. (A second memory access may be necessary to change the tristate functionality at the PCM highway). To program the signaling function of the device MACR: CMC3 ... 0 control the signaling scheme as outlined below.

In read accesses the 4 bits of the CM control field are read and stored in MADR: MD3 ... MD0.

CMC3..CMC0 Control Memory Code; these bits may only be used if 111 is selected for MOC3 ... MOC1. In this case bit 3 of MACR is CMC3. CMC3 ... CMC0 are entered to the control memory code field after the MACR access. They control the PCM channel bandwith and subchannel position as well as the signaling function of the EPIC as described below.

If MOC3 ... MOC1 is not selected 111, CMC2 ... CMC0 have to be selected 000. For read operations with MOC3 ... MOC1 = 111, CMC3 ... CMC0 need to be fixed to logical 0.

PCM Interface Subchannel Selection Codes

CMC3	CMC2	CMC1	CMC0	Transferred Bits	Channel Bandwith
0	0	0	0	-	-
0	0	0	1	Bits 7..0	64 kbps
0	0	1	1	Bits 7..4	32 kbps
0	0	1	0	Bits 3..0	32 kbps
0	1	1	1	Bits 7..6	16 kbps
0	1	1	0	Bits 5..4	16 kbps
0	1	0	1	Bits 3..2	16 kbps
0	1	0	0	Bits 1..0	16 kbps

Tab. 4.13: Codes for the Selection of the PCM Interface Subchannels

The selected code is transferred to a CM code field position selected by MAAR. During the switching operation the code then controls the bandwith and subtime slot position at the PCM interface on a per channel basis. Thus more than one CFI subtime slot can be mapped to one PCM time slot.

Programming the loopable unassigned code (0000) for an upstream connection, the corresponding upstream data memory location is not written during switching operation (unassigned channel). In downstream connections, however, the location is read, but not output at the CFI and, thus, can be used to establish loops.

CFI Codes

CMC3	CMC2	CMC1	CMC0	Transferred Bits
1	0	1	1	CS Channel
1	0	1	0	CS Channel
1	0	0	0	CS Channel
1	0	0	1	CS Channel, µP channel setup

Tab.4.14: CFI Codes

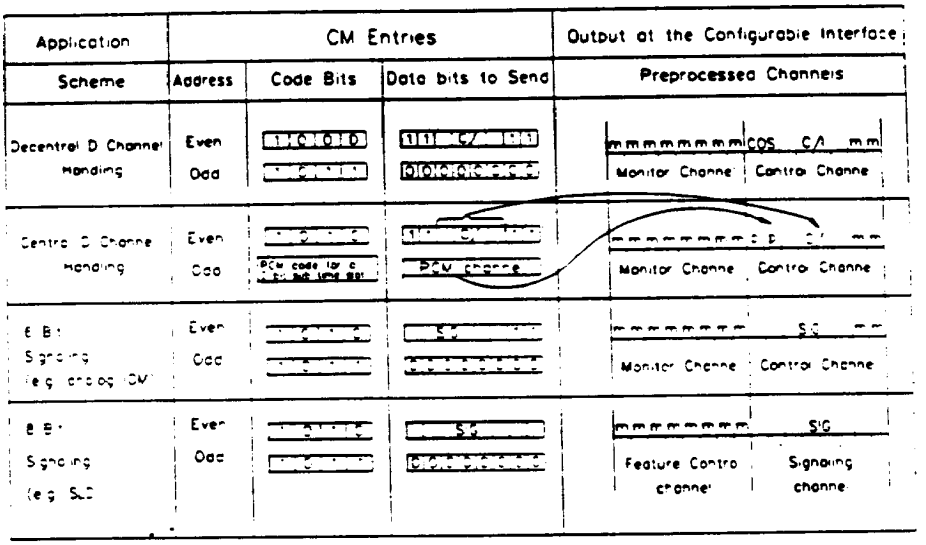
For a description of the CS Channel Function please refer to the following pages.

The CMC3...CMC0 = 1001 choise is also used for accessing a 64 kbps CFI Channel. In this case the CM data field entry is coded by the CM locations address according to table 4.18. Thus e.g. a CFI idle channel may be set up , or CFI data may be read via the µP interface.

CS Codes

The CS codes control the CS channel (Control channel in IOM applications, Signaling channel in SLD applications). To activate the EPICs signaling handling function, two CFI codes per SLA (Subscriber line access) are programmed to two consecutive CM code field positions starting with the even address. These two positions map to the preprocessed time slots, e.g. the Monitor and Control channels in IOM configuration or the Feature Control and Signaling channels in SLD configuration. The signaling schemes defined by these codes are explained in the figures 4.15 and 4.16 for the upstream and downstream directions.

The signaling schemes may be programmed to the SLAs independently from one another.



Tab. 4.15: Programming the CM for Downstream Signaling Handling

Application	CM Entries			Input from the Configurable Interface
Scheme	Address	Code Bits	Data Bits to Read	Preprocessed Channels
Decentral D Channel Handling	Even	1101010	XIX C/I XIX	mmmmmmmm / C/I mm
	Odd	0101010	XIXIXIXIXIX	Monitor Channel / Control Channel
Central D Channel	Even	1101010	XIX C/I XIX	mmmmmmmm / P P C/I mm
	Odd	[illegible]	PCM channel	Monitor Channel / Control Channel
8 Bit Signaling (e.g. analog IOM)	Even	1101110	Actual Value XIX	mmmmmmmm / Value mm
	Odd	1101110	Stable Value XIX	Monitor Channel / Control Channel
Bidirectional 8 Bit Signaling (e.g. SLD)	Even	1101111	Actual Value	mmmmmmmm / Value
	Odd	1101111	Stable Value	Feature Control channel / Signaling channel

Tab. 4.16: Programming the CM for Upstream Signaling Handling

LEGEND

m ... these bits are treated by the monitor handler

COS ... the output resistence of these bits is determined by OMDR:COS

C/I ... these bits are exchanged between the CFI in/output and the CM. A change of the C/I bits in upstream direction causes an interrupt (ISTA:SFI). The location of the change is stored in CSFIFO.

P... This D channel information is switched to and from the PCM interface. The PCM time slot and subtime slot positions are defined by the pointer and the code field entry residing in the odd CM entry of the respective SLA.

SIG ... these bits are included in the CFI data stream from the CM.

Value ... these bits are extracted from the CFI upstream data. The value which occured in the last frame is stored in the actual value bits of the even address CM location, the stable value in the CM location of the odd address. The stable value is found implementing the double last look algorithm: A new value must reoccur after the double last look period programmed in TIMR to become a stable value. A new stable value causes an interrupt (ISTA:SFI, location in SFIFO).

4.3.2. Memory Access Address Register (MAAR)

Access in the multiplexed µP interface mode: Read or write, address: 02H
Access in a demultiplexed µP interface mode: Read or write, address 1H, OMDR:RBS = 0

bit 7							bit 0
U/D	MA6	MA5	MA4	MA3	MA2	MA1	MA0

This register buffers the µP address to the CM or DM. In DM accesses the address encodes the time slot and port of the PCM interface, in CM accesses of the CFI interface.

U/D... For both CM and DM accesses, the U/D bit being programmed as logical 0 selects the downstream direction in the specific memory, a logical 1 selects the upstream direction.

MA6..MA0... The time slot to be handled is programmed to the EPIC via the time slot number bits according to the tables 4.17 and 4.18. In all modes, the MA6 bit is the most significant, the MA0 bit the least significant time slot number bit.

The logical port numbers used for programming may be looked up in the tables 4.3 and 4.7 for the PCM ports and for the IOM ports. The bidirectional pin and logical port numbers match.

Data Memory Address		
PCM Mode 2	Bit U/D Bit MA6 to MA0	Direction Selection Time Slot Number
PCM Mode 1	Bit U/D Bit MA6 to MA3, MA1, MA0 Bit MA2	Direction Selection Time Slot Number Logical PCM Port Number
PCM Mode 0	Bit U/D Bit MA6 to MA3, MA0 Bit MA2 to MA1	Direction Selection Time Slot Number Logical PCM Port Number

Tab. 4.17: Programming PCM ports and time slots for the Data Memory

Control Memory Address		
CFI Mode 2	Bit U/D Bit MA6 to MA0	Direction Selection Time Slot Number
CFI Mode 1	Bit U/D Bit MA6 to MA3, MA2, MA0 Bit MA1	Direction Selection Time Slot Number Logical IOM Port Number
CFI Mode 0	Bit U/D Bit MA6 to MA3, MA0 Bit MA2 to MA1	Direction Selection Time Slot Number Logical IOM Port Number
CFI Mode 3	Bit U/D Bit MA6 to MA4, MA0 Bit MA3 to MA1	Direction Selection Time Slot Number Logical Bidirectional Port Number

Tab. 4.18: Programming CFI ports and time slots for the Control Memory

4.3.3. Memory Access Data Register (MADR)

Access in the multiplexed µP interface mode: Read or write, address: 04_H

Access in a demultiplexed µP interface mode: Read or write, address 2_H, OMDR:RBS = 0

bit 7							bit 0
MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0

This register buffers the µP data to the data and control memories.

4.4. Synchron Transfer Registers

The synchron transfer period between the maskable synchron transfer overflow interrrupt (ISTA:SOV, MASK:SOV) and the maskable synchron transfer interrrupt (ISTA:SIN, MASK:SIN) is 16 RCL periods per active synchron transfer channel.

4.4.1. Synchron Transfer Data Register A (STDA)

Access in the multiplexed µP interface mode: Read or write, address: 06H
Access in a demultiplexed µP interface mode: Read or write, address 3H, OMDR:RBS = 0

bit 7							bit 0
MTDA7	MTDA6	MTDA5	MTDA4	MTDA3	MTDA2	MTDA1	MTDA0

MTDA7..MTDA0 ...µP Transfer Data for Channel A; these bits are extracted by the EPIC from the source data stream as specified in SARA and included into the destination data stream at the location indicated by the SAXA content.

4.4.2. Synchron Transfer Data Register B (STDB)

Access in the multiplexed µP interface mode: Write or read, address: 08H
Access in a demultiplexed µP interface mode: Read or write, address 4H, OMDR:RBS = 0

bit 7							bit 0
MTB7	MTB6	MTB5	MTB4	MTB3	MTB2	MTB1	MTB0

MTDB7..MTDB0 ...µP Transfer Data for Channel B; these bits are extracted from the source data stream as specified in SARB end included into the destination data stream at the location indicated by the SAXB content.

4.4.3. Synchron Transfer Receive Address Receive A (SARA)

Access in the multiplexed µP interface mode: Read or write, address: 0AH
Access in a demultiplexed µP interface mode: Read or write, address 5H, OMDR:RBS = 0

bit 7							bit 0
ISRA	MTRA6	MTRA5	MTRA4	MTRA3	MTRA2	MTRA1	MTRA0

ISRA ... Interface Select Receive for Channel A; selects the PCM interface (logical 0) or the configurable interface (logical 1) as source interface for the synchron transfer channel A.

MTRA6..MTRA0 ... µP Transfer Receive for Channel A; identifies the source port and time slot as stated in table 4.17 and 4.18 for the PCM and CFI interfaces being selected by ISRA, respectively.

4.4.4. Synchron Transfer Receive Address Register B (SARB)

Access in the multiplexed µP interface mode: Read or write, address: $0C_H$

Access in a demultiplexed µP interface mode: Read or write, address 9_H, OMDR:RBS = 0

bit 7							bit 0
ISRB	MTRB6	MTRB5	MTRB4	MTRB3	MTRB2	MTRB1	MTRB0

ISRB ... Interface Select Receive for Channel B; selects the PCM interface (logical 0) or the configurable interface (logical 1) as source interface for the synchron transfer channel B.

MTRB6..MTRB0 ... µP Transfer Receive for Channel B; identifies the source port and time slot as stated in table 4.17 and 4.18 for the PCM and CFI interfaces being selected by ISRB, respectively.

4.4.5. Synchron Transfer Transmit Address Register A (SAXA)

Access in the multiplexed µP interface mode: Read or write, address: $0E_H$

bit 7							bit 0
ISXA	MTXA6	MTXA5	MTXA4	MTXA3	MTXA2	MTXA1	MTXA0

ISXA ... Interface Select Transmit for Channel A; selects the PCM interface (logical 0) or the configurable interface (logical1) as target interface for the synchron transfer channel A.

MTXA6..MTXA0 ... µP Transfer Transmit for Channel A; identifies the destination port and time slot as stated in tables 4.17 and 4.18, in the case the PCM and configurable interfaces are selected, respectively.

4.4.6. Synchron Transfer Transmit Address Register B (SAXB)

Access in the multiplexed µP interface mode: Read or write, address: 10_H
Access in a demultiplexed µP interface mode: Read or write, address 8_H, OMDR:RBS = 0

bit 7							bit 0
ISXB	MTXB6	MTXB5	MTXB4	MTXB3	MTXB2	MTXB1	MTXB0

ISXB ... Interface Select Transmit for Channel B; selects the PCM interface (logical 0) or the configurable interface (logical 1) as target interface for the synchron transfer channel B.

MTXB6..MTXB0... µP Transfer Transmit for Channel B; identifies the destination port and time slot as stated in table 4.17 if the PCM interface is selected, and table 4.18 in the case the configurable interface programmed.

4.4.7. Synchron Transfer Control Register (STCR)

Access in the multiplexed µP interface mode: Read or write, address: 12_H
Access in a demultiplexed µP interface mode: Read or write, address 9_H, OMDR:RBS = 0
Reset Value: 00_H

bit 7							bit 0
TBE	TAE	CTB2	CTB1	CTB0	CTA2	CTA1	CTA0

TAE, TBE ... Transfer Channel A (B) Enable; A logical 1 enables the µP transfer, a logical 0 disables the transfer of the corresponding channel.

CTA2...CTA0, CTB2..CTB0... Channel Type A (B); these bits determine the bandwidth of the channel and the position of the relevant bits in a time slot according to table 4.19.

CT#2	CT#1	CT#0	Bandwith	Relevant Bits
0	0	0	Not Allowed	-
0	0	1	64 kbit/s	bits 7...0
0	1	0	32 kbit/s	bits 3...0
0	1	1	32 kbit/s	bits 7...4
1	0	0	16 kbit/s	bits 1...0
1	0	1	16 kbit/s	bits 3...2
1	1	0	16 kbit/s	bits 5...4
1	1	1	16 kbit/s	bits 7...6

Tab. 4.19: Synchron Transfer Channel Type

4.5. Monitor/Feature Control Registers (MFCH)

4.5.1. MF Channel Active Indication Register (MFAIR)

Access in the multiplexed µP interface mode: Read, address: 14_H
Access in a demultiplexed µP interface mode: Read or write, address A_H, OMDR:RBS = 0
Reset value: undefined

bit 7							bit 0
0	SO	SAD5	SAD4	SAD3	SAD2	SAD1	SAD0

SO... MF Channel Search on; this bits indicates if the EPIC is still busy looking for an active MF Channel (logical 1) or not (logical 0).

SAD5...SAD0 ... Subscriber Address; with OMDR:MFPS and CMDR:MFSO set to logical 1 (Search for Command/Acknowledgement within the handshake procedure) after an interrupt (ISTA, MASK:MAC) these bits point to the port and time slot, where an active MF channel was found. For the coding of time slot and port numbers refer to MFSAR: SAD5...SAD0.

4.5.2. MF Channel Subscriber Address Register (MFSAR)

Access in the multiplexed µP interface mode: Write, address: 14_H
Access in a demultiplexed µP interface mode: Read or write, address A_H, OMDR:RBS = 0
Reset value: undefined

bit 7							bit 0
MFTC1	MFTC0	SAD5	SAD4	SAD3	SAD2	SAD1	SAD0

MFTC 1...0 MF Channel Transfer Control 1,0; these bits, in addition to CMDR:MFT1,0 and OMDR:MFPS control the MF Channel transfer as detailed in the following tables:

Transmit Selection (CMDR:MTF1,MTF0 = 01)

MFTC1,0	Recipient
0 0	as programmed in MFSAR:SAD5...SAD0
0 1	broadcast: all MF channels
1 0	test operation
1 1	reserved

Tab. 4.20: Transmit Selection

For broadcast transmission with active handshake protocol instantaneous acknowledgement by all recipients is assumed and arriving acknowledgements are ignored. The MF bytes are transmitted at full speed, i.e. one byte per frame. In test operation (MFT1,0 = 10), the data in MFFIFO is not transmitted and can instantaneously be read.

Selections Transmit + Receive and Transmit Continuous (CMDR:MTF1, MTF0 = 10 or 11)

MFTC1,0	Number of expected receive bytes
0 0	1
0 1	2 (not allowed for active handshake protocol)
1 0	8 (not allowed for active handshake protocol)
1 1	16 (not allowed for active handshake protocol)

Tab. 4.21: Receive Byte Count

Table 4.20 states the number of bytes written into MFFIFO with the handshake protocol not active. When the handshake protocol is active, the selection MFTC1,0 = 00 is the only allowed choice.

SAD5...SAD0 ... These bits define the addressed subscriber. To achieve a time slot identification according to table 4.18, an additional least significant bit set to logical 0 and an additional most significant bit depending on the transfer direction (CMDR:MFT1,MFT0) has to be assumed.

4.5.3. MF Channel FIFO (MFFIFO)

Access in the multiplexed µP interface mode: Read or write, address: 16_H, 16 bytes deep

Access in a demultiplexed µP interface mode: Read or write, address B_H, OMDR:RBS = 0

Reset value: the MFFIFO is empty

bit 7							bit 0
MFD7	MFD6	MFD5	MFD4	MFD3	MFD2	MFD1	MFD0

The contents of this register is transferred byte by byte in the monitor (IOM configuration) or feature control (SLD configuration) channels as specified by MFSAR:SAD5...SAD0. MFFIFO is reset by setting CMDR:MFFR or by selecting OMDR:OMS0 = 0.

4.6. Status/Control Registers (SCR)

4.6.1. Signaling FIFO (C/I FIFO)

Access in the multiplexed µP interface mode: Read, address: 18_H, 9 bytes deep
Access in a demultiplexed µP interface mode: Read or write, address C_H, OMDR:RBS = 0
Reset value: 0xxx xxxx

bit 7							bit 0
SBV	SAD6	SAD5	SAD4	SAD3	SAD2	SAD1	SAD0

SBV ... Signaling Byte Valid; a logical 1 indicates SAD6...SAD0 to be valid. This bit is set to logical 0 if the corresponding SAD6...SAD0 is invalid.

The SBV bits of all C/I FIFO bytes are reset by selecting OMDR:OMS0 = 0 or by instructing the EPIC to reset the C/I FIFO (CMDR:CFR = 1)

SAD6...SAD0 ... Subscriber Address; this address points to the location in the CM where the received C/I channel has changed. If SBV signals a valid pointer, all 8 bits of the signaling FIFO may be used as CM address, since SBV being logical 1 identifies the upstream block of the CM. If SAD0 is logical 0 (even address), a C/I channel of a digital subscriber is addressed. If it is logical 1 (odd address) the stable value of a signaling channel (analog subscriber) is addressed.

4.6.2. Timer Register (TIMR)

Access in the multiplexed µP interface mode: Write, address: 18_H
Access in a demultiplexed µP interface mode: Read or write, address C_H, OMDR:RBS = 0
Reset value: 00_H

bit 7							bit 0
SSR	TVAL6	TVAL5	TVAL4	TVAL3	TVAL2	TVAL1	TVAL0

SSR ... Signaling Channel Sample Rate; the double last look period is fixed to 125 microseconds (logical 1) or determined by TVAL6...TVAL0 (logical 0).

TVAL6...0 ... Timer Value; The timer period is given by these bits in intervals of 250 µs and is used in three functions of the EPIC:

- double last look algorithm (controlled by SSR)
- interrupt generation (CMDR:ST)

* CFI multiframe generation (CMD2:FC2...FC0)

The timer is started as soon as CMDR:ST is set to logical 1 and stopped by programming the timer register or by selecting OMDR:OMS0 = 0.

4.6.3. Status Register (STAR)

Access in the multiplexed µP interface mode: Read, address: $1A_H$
Access in a demultiplexed µP interface mode: Read or write, address D_H, OMDR:RBS = 0
Reset value: 05_H

bit 7							bit 0
MAC	TAC	PSS	MFTO	MFAB	MFAE	MFRW	MFFE

MAC ... Memory Access; a memory access is in operation, if this bit is logical 1. Hence, the memory access registers may not be used.

TAC ... Timer Active; if this bit is set, the timer runs (TIMR).

PSS ... PCM Synchronization Status; the PCM interface is synchronized (logical 1) or not synchronized (logical 0). (ISTA:PFI, MASK:PFI, PBNR)

MFTO ... MF Channel Transfer in Operation; the MF channel transfer is still in operation (logical 1) or completed (logical 0).

MFAB ... MF Channel Transfer Aborted; a logical 1 indicates that the remote transmitter aborted a handshaked message transfer.

MFAE ... MF FIFO Access Enable; the MFFIFO may be either read or written (logical 1) or may not be accessed (logical 0).

MFRW ... MF FIFO Read/Write; if MFAE = 1 the MFFIFO may be read (logical 1) or is ready to be written (logical 0).

MFFE ... MF FIFO Empty; the MFFIFO is empty (logical 1) or not empty (logical 0).

4.6.4. Command Register (CMDR)

Access in the multiplexed µP interface mode: Write, address: $1A_H$

Access in a demultiplexed µP interface mode: Read or write, address D_H, OMDR:RBS = 0

Reset value: 00_H

bit 7							bit 0
0	ST	TIG	CFR	MFT1	MFT0	MFSO	MFFR

ST ... Start Timer; setting this bit to logical 1 starts the timer running cyclically from 0 to the value programmed in TIMR:TVAL6...0. A logical 0 does not affect the timer.

TIG... Timer Interrupt Generation; setting this bit together with ST to logical 1 causes the EPIC to generate a periodic interrupt whenever the timer runs out. (See TIMR:TVAL6...0 and ISTA:TIN). A logical 0 disables the interrupt.

CFR ... C/I FIFO Reset; setting this bit resets the signaling FIFO, which takes 2 RCL periods.

MFT1, MFT0 ... MF Channel Transfer; these bits start a MF Channel transfer according to the following table:

MFT1	MFT0	Function
0	0	Inactive
0	1	Transmit
1	0	Transmit + Receive same timeslot
1	1	Transmit Continuous (OMDR:MFPS = 1)
1	1	Transmit + Receive same line (OMDR:MFPS = 0)

Tab. 4.22: MF Channel Transfer Direction Control

The contents or MFFIFO are exchanged in the channel programmed to MFSAR:SAD5..SAD0 controlled by MFSAR:MFTC1..0. By programming MFT1, MFT0 = 01, the MFFIFO contents are transmitted. By selecting MFT1, MFT0 = 10 they are transmitted and an answer is expected in the same timeslot. For Transmit + Receive on the same line (handshake protocol not

active), the PEB 2055 expects bytes at the same line, but 4 time slots later than programmed to MFSAR:SAD5...SAD0 (SLD configuration). MFT1,MFT0 = 11(active handshake protocol) is chosen, if more than 16 bytes are to be transmitted, the first 16 of which reside in MFFIFO. After transmitting the MFFIFO contents or receiving the answer, the EPIC generates a maskable interrupt (ISTA:MFFI, MASK:MFFI). The actual state of the transfer can be evaluated by reading STAR:MFTO..MFTE.If the MFFIFO is empty and Transmit + Receive is selected,the EPIC starts receiving bytes immedeately.

MFSO... MF Channel Search ON; if this bit is set to logical 1, the EPIC starts to search for active MF channels. If an active channel is found the channel address is stored in MFAIR and an interrupt is generated (ISTA:MAC). The search is stopped when an active MF channel has been found or when OMDR:OMS0 = 0.

MFFR... MF FIFO Reset; setting this bit resets the MFFIFO within 2 RCL periods. After which, MFFR is reset again.

4.6.5. Interrupt Status Register (ISTA)

Access in the multiplexed µP interface mode: Read, address: $1C_H$

Access in a demultiplexed µP interface mode: Read or write, address E_H, OMDR:RBS = 0

Reset value: 00_H

bit 7							bit 0
TIN	SFI	MFFI	MAC	PFI	PIM	SIN	SOV

TIN ... Timer Interrupt; if this bit is set to logical 1, a timer interrupt (CMDR:ST0, TIMR) has occured. The bit is reset by reading ISTA.

SFI ... Signaling FIFO Interrupt; a logical 1 indicates a change in an upstream C/I or signaling channel. The bit is reset when FIFO is empty.

MFFI ... MF FIFO Interrupt; if this bit is set, the last MF channel command (issued by CMDR:MFT1, MFT0) has been executed and the EPIC is ready to accept the next command (STAR:MFTO...MFFE). This bit is reset by the ISTA access.

MAC ... Monitor Channel Active Interrupt; a logical 1 indicates an active monitor channel, for the case CMDR:MFSO = 1. MFAIR contains the address of this channel. This bit is cleared by the ISTA access.

PFI... PCM Framing Interrupt; this bit being logical 1 indicates the lost or regained synchronization at the PCM interface. Synchronization is considered lost by the EPIC if the PFS signal is not repeated with a period determined by PBNP. Synchronization is considered regained if two consecutive PFS pulses with the correct period are received. PFI is reset by reading ISTA.

PIM ... PCM Input Mismatch; a logical 1 indicates a PCM input mismatch (PICM,PMOD:AIS0,1); PIM is reset by reading ISTA.

SIN ... Synchron Transfer Interrupt; the synchron transfer registers can be read and written if this bit is logical 1; this bit is reset by reading ISTA.

SOV ... Synchron Transfer Overflow; a logical 1 indicates that the data of one of the active synchron transfer channels (STCR:TAE,TBE) has not been accessed within the µP access period of the synchron transfer facility. This bit is reset by reading ISTA.

4.6.6. Mask Register (MASK)

Access in the multiplexed µP interface mode: Write, address: $1C_H$

Access in a demultiplexed µP interface mode: Read or write, address E_H, OMDR:RBS = 0

Reset value: 00_H

bit 7							bit 0
TIN	SFI	MFFI	MFAC	PFI	PIM	SIN	SOV

A logical 1 disables the corresponding interrupt as described in ISTA.

A masked interrupt is stored internally and reported in ISTA immediately if the mask is released.

A SFI interrupt, however, is also reported in ISTA if masked. In this case an interrupt is not generated.

4.6.7. Operation Mode Register (OMDR)

Access in the multiplexed µP interface mode: Read or write, 1E$_H$ or 3E$_H$

Access in a demultiplexed µP interface mode: Read or write, address F$_H$, OMDR:RBS = X

Reset value: 00$_H$

bit 7							bit 0
OMS1	OMS0	PSB	PTL	COS	MFPS	CSB	RBS

OMS1...OMS0 ... Operation Mode Select; these bits determine the operation mode the EPIC is working in according to the following table:

OMS1	OMS0	Function
0	0	CM reset mode; In this mode the EPIC does not operate normaly. Instead, a CM Access via the memory access registers accessess all CM positions. Only accesses with MACR:MOC3 = 1 are performed. A typical application is resetting the CM (MACR = 70$_H$, MADR:XX$_H$). Such a complete CM access is finished within 256 RCL periods.
1	0	CM initialization mode; In this selection the EPIC does not operate normally . This selection allows for a fast programming of the CM (e.g. for monitor and C/I channel selection) reducing the memory access busy time to maximally 2.5 RCL cycles.
1	1	Normal operation mode; memory access period 9.5 RCL cycles maximally.
0	1	Test mode. In this mode the EPIC subtains normal operation. However, a memory access does not only affect the one location of MAAR, but all positions in the specific memory.

Tab. 4.23: Operation modes

Setting OMS0 to logical 0 stops the software timer (CMDR:ST1; TIMR) and resets MFFIFO as well as C/I FIFO.

PSB ... PCM Standby; a logical 0 switches the PCM interface outputs to high impedance.

COS ... CFI Output Driver Selection; programming a logical 1, the CFI output drivers are open drain drivers for unassigned channels; programming a logical 0, they are tristate drivers.

MFPS ... MF Channel Protocol Selection; a logical 1 enables the handshake facility of the EPIC, with a logical 0 it is disabled.

PTL... PCM Test Loop; the PCM interface output and input lines are internally connected, if PTL is logical 1. In this case, the PCM data are still output according to the DM tristate field, but the PCM input is disabled.

CSB ... CFI Standby; a logical 0 switches the CFI outputs to high impedance.

RBS... Register Bank Selection; in the demultiplexed µP access mode this bit switches between the registers mainly used for initialization (logical 1) and those mainly used in operation (logical 0).

4.6.8. Version Number Status Register (VNSR)

Access in the multiplexed µP interface mode: Read, address: $3A_H$

Access in a demultiplexed µP interface mode: Read or write, address D_H, OMDR:RBS = 1

Reset Value: $0X_H$

bit 7							bit 0
IR	0	0	0	VN3	VN2	VN1	VN0

These bits contain the version number of the device according to below table:

VN3	VN2	VN1	VN0	Device Versions
0	0	0	0	A1, A2, A3

IR... Initialization Request; The code memory has to be reprogrammed due to loss of data (IR = 1). The IR bit is set after power failure or inappropriate clocking and reset when a code memory initialization (CMDR:OMS1,0 = 10) is finished.

5. Electrical Specification

5.1. Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

Ambient temperature under bias	0 to 70°C
Storage temperature	- 65 to 125°C

5.2. DC Characteristics

Ambient temperature under bias range; VDD = 5V ± 5%, VSS = 0V.

Symbol	Parameter	Limit Value min	max	Unit	Test Condition
V_{IL}	Input low voltage	- 0.4	0.8	V	
V_{IH}	Input high voltage	2.0	V_{DD} + 0.4	V	
V_{OL}	Output low voltage		0.45	V	I_{OL} = 7 mA for DD0-DD3, DU0-DU3 I_{OL} = 2 mA for all other
V_{OH}	Output high voltage	2.4		V	I_{OH} = - 400 µA
V_{OH}	Output high voltage	V_{DD} - 0.5		V	I_{OH} = -100 µA
I_{CC}	Operational power supply current		9.5 6.5	mA	VDD = 5V, Inputs at 0V or VDD, no output loads. clock frequency > 4096 kHz clock frequency ≤ 4096 kHz

Tab. 5.1: DC Characteristics of the EPIC

5.3. Capacitances

TA = 25°C, VDD = 5V ± 5%, VSS = 0V.

Symbol	Parameter	Limit Value min	Limit Value max	Unit	Test Condition
C_{IN}	Input capacitance		10	pF	
C_{IO}	I/O capacitance		20	pF	
C_{OUT}	Output capacitance		15	pF	

Tab. 5.2: Input/Output Capacitances of the EPIC

5.4. AC Characteristics

Ambient temperature under bias range, VDD = 5V ± 5%

Inputs are driven at 2.4 V for a logical 1 and at 0.4 V for a logical 0. Timing measurements are made at 2.0 V for a logical 1 and at 0.8 V for a logical 0. The AC testing input/output waveforms are shown below.

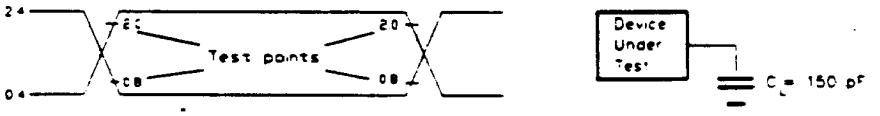


Fig. 5.1: I/O Waveform for AC Tests

5.4.1. Microprocessor Interface Timing

Symbol	Parameter	Limit Values min	max	Unit	Test condition
TAA	ALE pulse width	30	-	ns	-
TAL	Address setup time to ALE	10	-	ns	-
TLA	Address hold time from ALE	15	-	ns	-
TALS	Address latch setup time to $\overline{WR}$, $\overline{RD}$	0	-	ns	-
TAS	Address setup time to $\overline{WR}$, $\overline{RD}$	10	-	ns	-
TAH	Address hold time from $\overline{WR}$, $\overline{RD}$	30	-	ns	-
TDSD	$\overline{RD}$ Delay after $\overline{WR}$ setup	0	-	ns	-
TRR	$\overline{RD}$ pulse width	120	-	ns	-
TRD	Data output delay from $\overline{RD}$	-	100	ns	-
TDF	Data float from $\overline{RD}$	-	25	ns	-
TRI	$\overline{RD}$ control interval	70	-	ns	-
TWW	$\overline{WR}$ pulse width	60	-	ns	-
TDW	Data setup time to $\overline{WR}$ + $\overline{CS}$	30	-	ns	-
TWD	Data hold time from $\overline{WR}$ + $\overline{CS}$	10	-	ns	-
TWI	$\overline{WR}$ control interval	70	-	ns	-

Tab. 5.3: µP Interface Timing Parameters

Intel Bus Mode

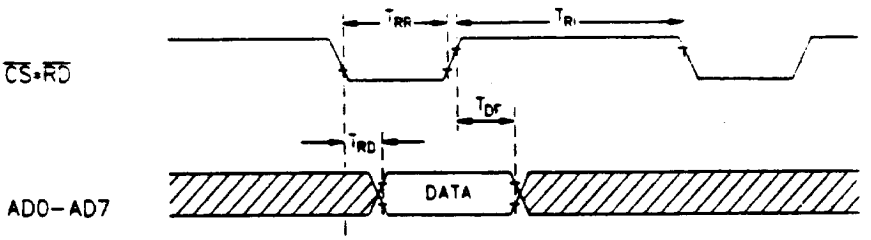


Fig. 5.2: µP Read Cycle

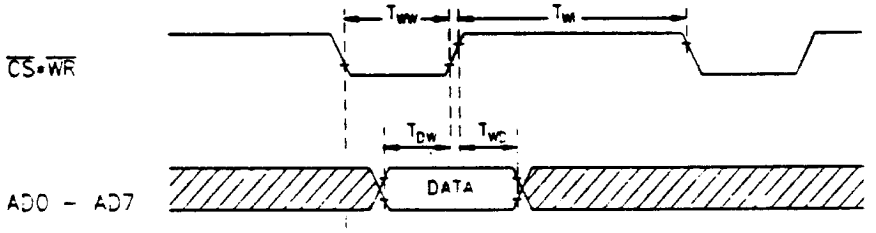


Fig. 5.3: µP Write Cycle

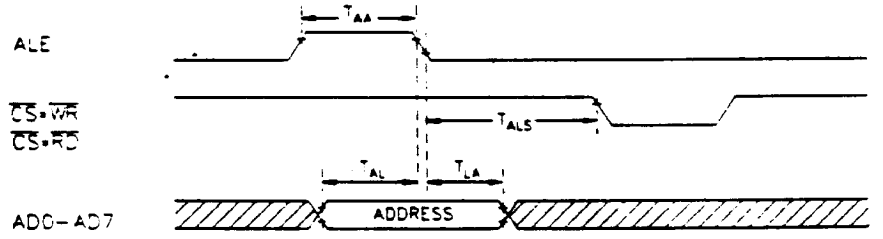


Fig. 5.4: Multiplexed Address Timing

Fig. 5.5: Demultiplexed Address Timing

Motorola Bus Mode

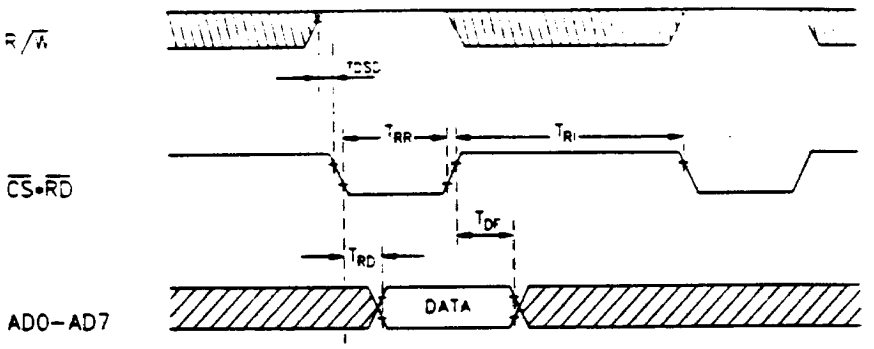


Fig. 5.6: µP Read Cycle

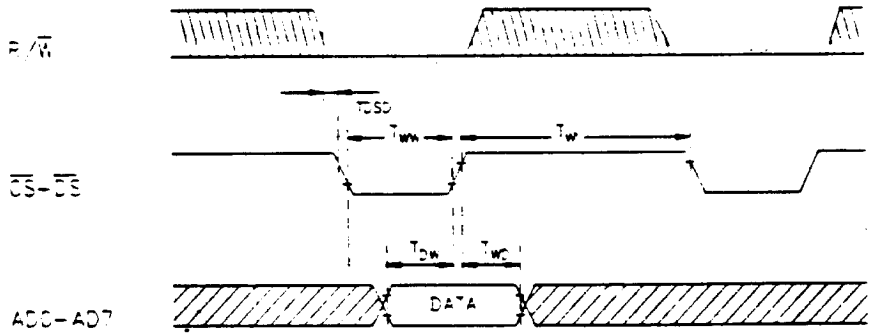


Fig. 5.7: µP Write Cycle

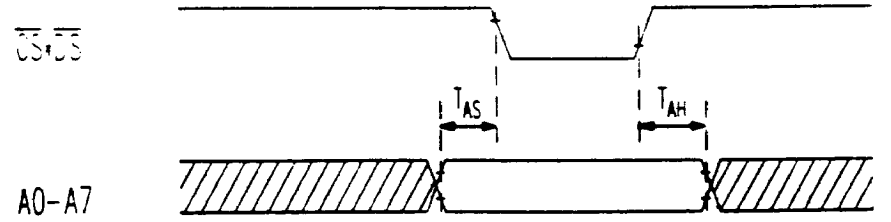


Fig. 5.8: Address Timing

5.4.2. Timing of PCM and Configurable Interfaces

Symbol	Parameter	Limit Values min	Limit Values max	Unit	Condition
T_{CP} T_{CPL} T_{CPH}	Clock period Clock period low Clock period high	240 80 100	- - -	ns ns ns	clock frequency ≤ 4096 kHz
T_{CP} T_{CPL} T_{CPH}	Clock period Clock period low Clock period high	120 50 50	- - -	ns ns ns	clock frequency > 4096 kHz
T_{FS} T_{FH}	Frame setup time Frame hold time	20 50	- -	ns ns	
T_{DCD}	Data clock delay time	-	125	ns	
T_S T_H	Serial data input setup time Serial data input hold time	7 35	- -	ns ns	PCM input data frequency > 4096 kbps
T_S T_H	Serial Data input setup time Serial data input hold time	15 50	- -	ns ns	PCM input data frequency ≤ 4096 kbps
T_S T_H	Serial Data input setup time Serial data input hold time	15 50	- -	ns ns	CFI input data frequency > 4096 kbps
T_S T_H	Serial Data input setup time Serial data input hold time	0 75	- -	ns ns	CFI input data frequency ≤ 4096 kbps
T_D	PCM Serial Data output delay time	-	55	ns	
T_T	Tristate control delay	-	60	ns	
T_{DF}	CFI Serial Data output delay time (falling clock edge)	-	60	ns	
T_{DR}	CFI Serial Data output delay time (rising clock edge)	-	80	ns	

Tab. 5.4: PCM and Configurable Interface Characteristics

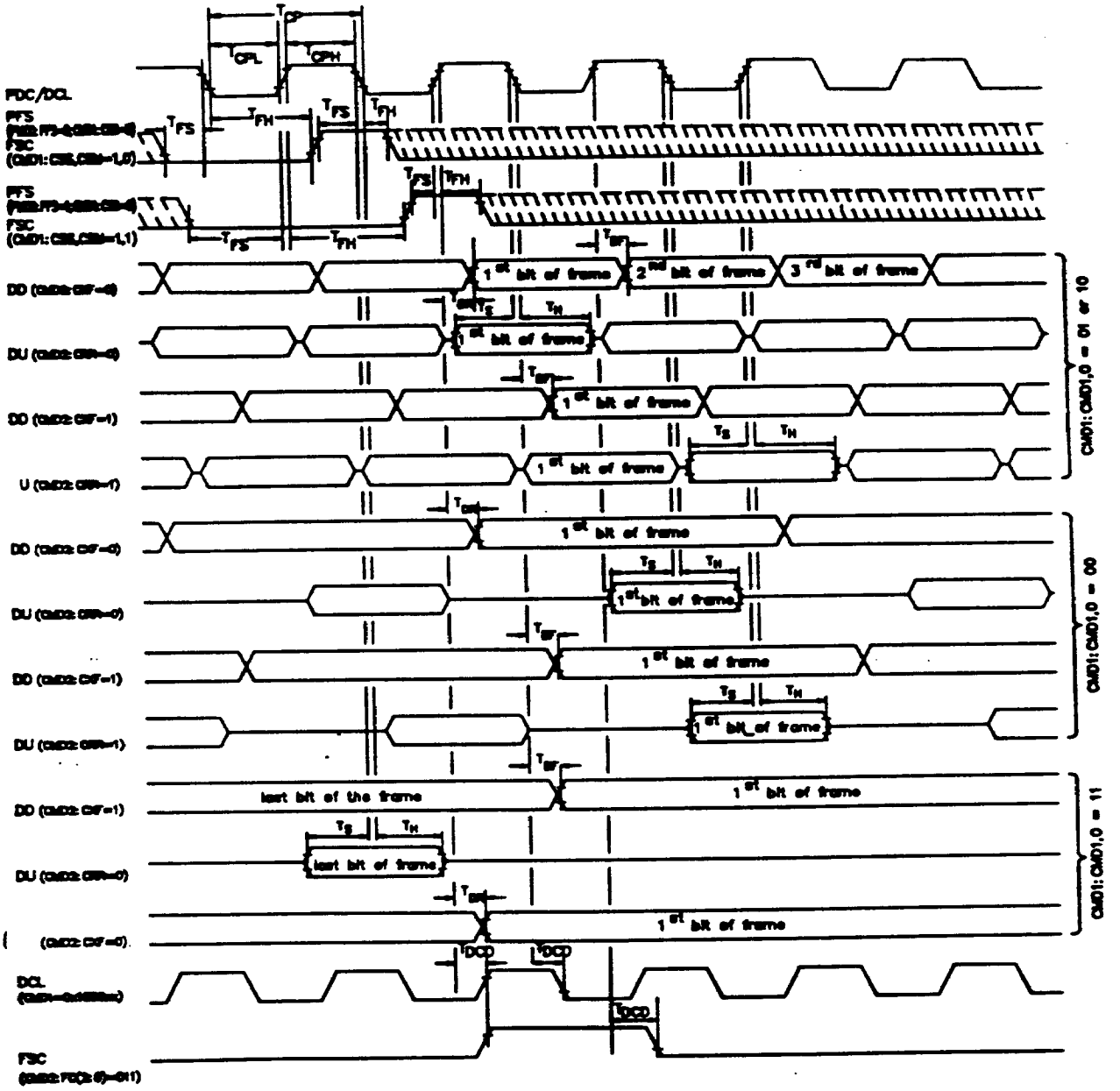


Fig. 5.9: AC Characteristics at the CFI with CMD:CSP1,0 = 10 (Prescalor Divisor = 1)

90

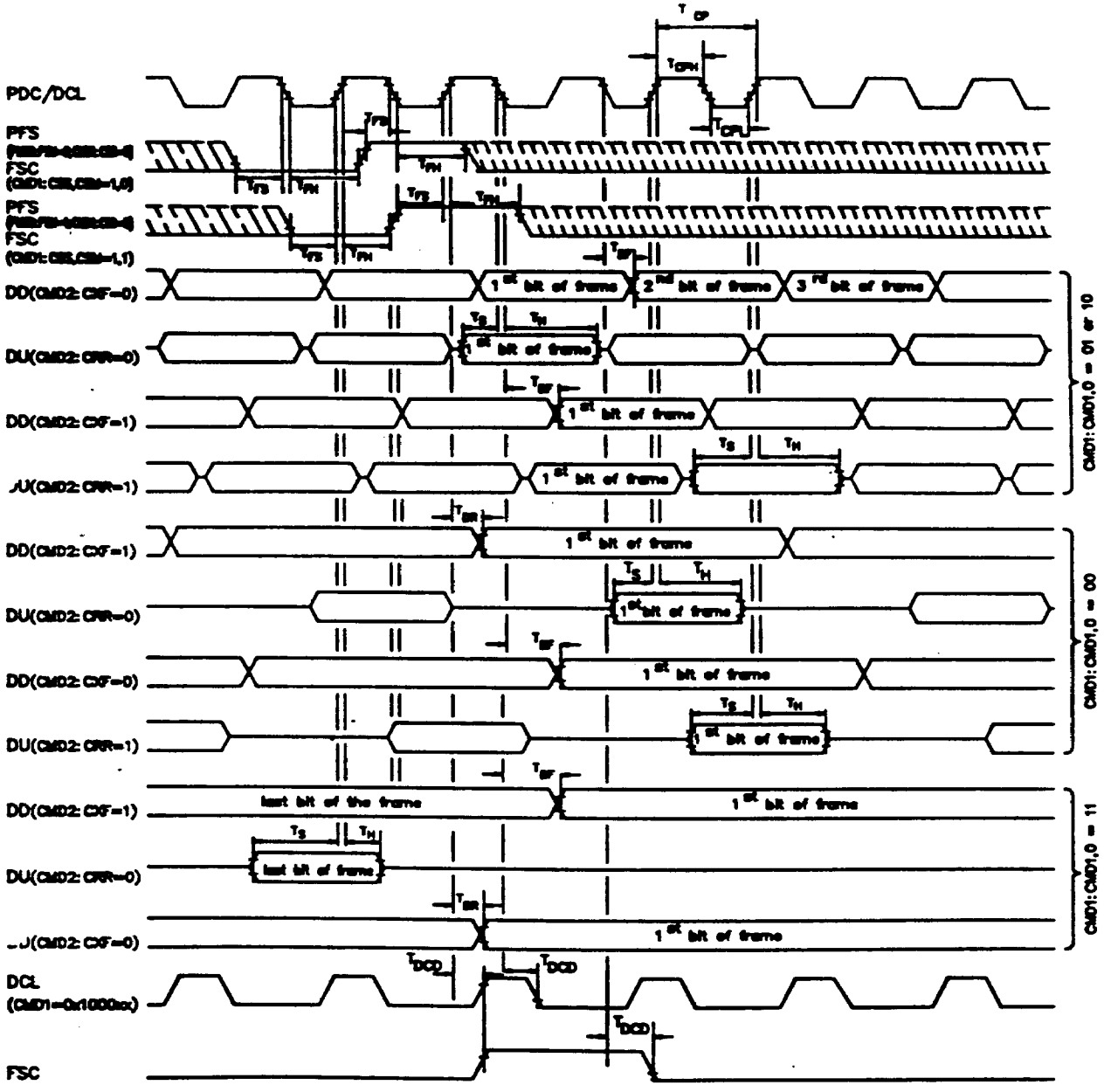


Fig. 5.10: AC Characteristics at the CFI with CMD1:CSP = 01 (Prescalor Divisor = 1.5)

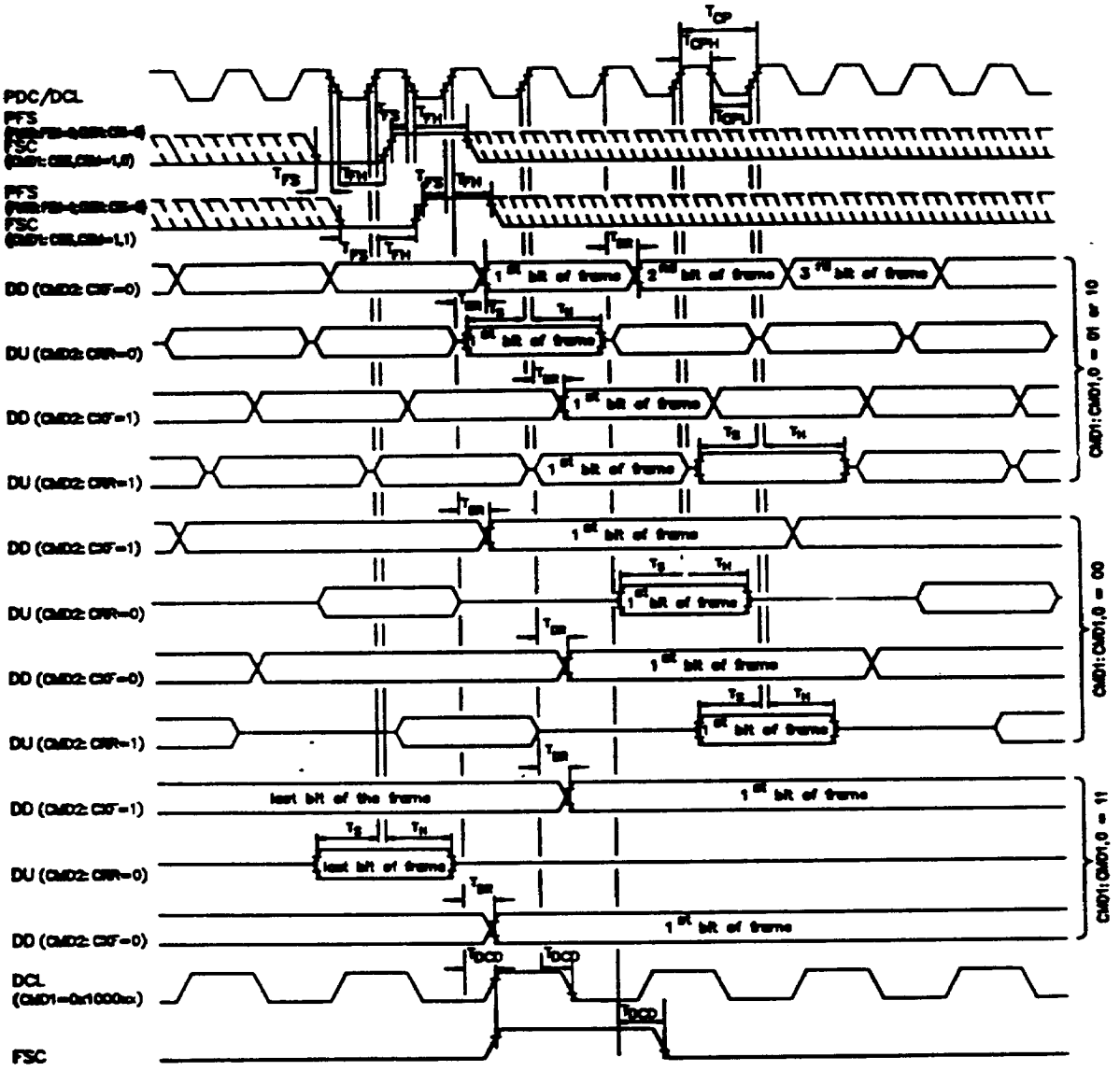


Fig. 5.11: AC Characteristics at the CFI with CMD:CSP1,0 = 00 (Prescalor Divisor = 2)

92

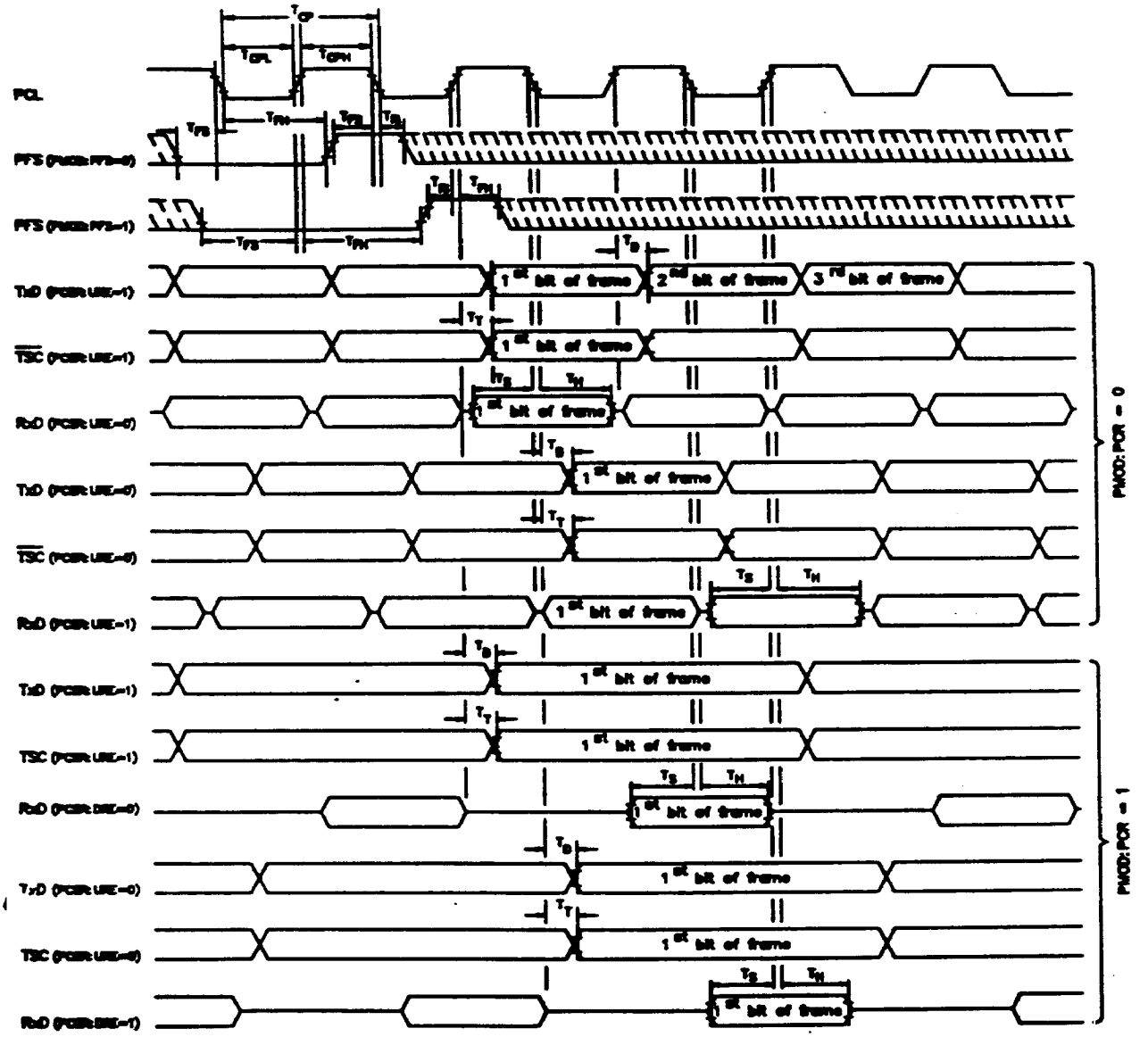


Fig. 5.12: AC Characteristics at the PCM Interface

5.5. Package Outline

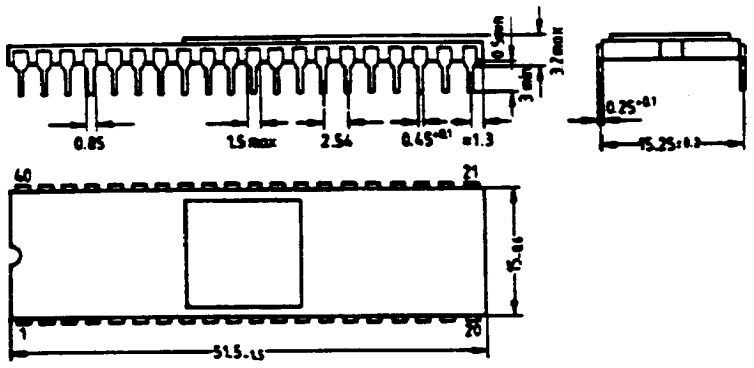


Fig. 5.13: Ceramic Package, 40 Pins, C-DIP 40

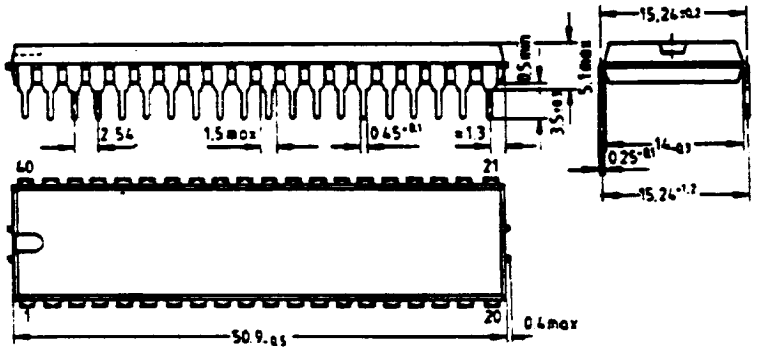


Fig. 5.14: Plastic Package, 40 Pins, P-DIP 40

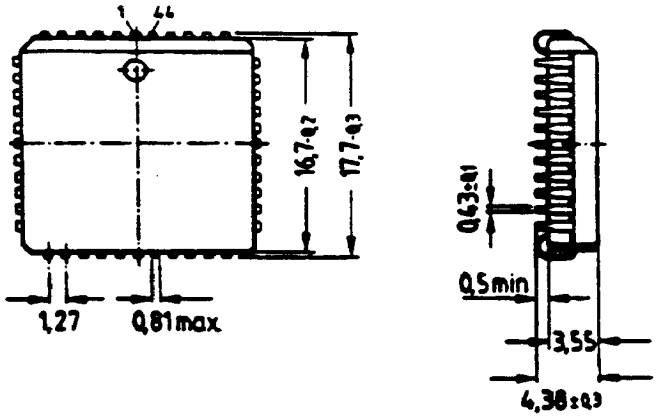


Fig. 5.15: Plastic Leadless Package, 44 Pins, PLCC 44

5.6. Ordering Codes

Type	Ordering Code	Package Outline
PEB 2055 P	Q67100 H 6036	P-DIP 40
PEB 2055 C	Q67100 H 6034	C-DIP 40
PEB 2055 W	Q67100 H 6035	PLCC 44

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