1.1 Scope.

This specification covers the detail requirements for a 8-bit resolution D/A converter (DACPORT®) complete with output amplifier, full microprocessor interface, precision reference and requiring only +5V.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number[1]
−1	AD558S(X)/883B
−2	AD558T(X)/883B

NOTE
[1]See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-16	16-Pin DIP (TO-116 Style)
E	E-20A	20-Terminal Leadless Chip Carrier

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

V_{CC} to Ground . . . . . 0 to +18V
Digital Inputs (Pins 1-10) . . . . . 0 to +7.0V
V_{OUT} . . . . . Indefinite Short to Ground
Momentary Short to V_{CC}
Power Dissipation 450mW
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature Range (Soldering 10sec) . . . . . 300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 30°C/W
θ_{JA} = 100°C/W

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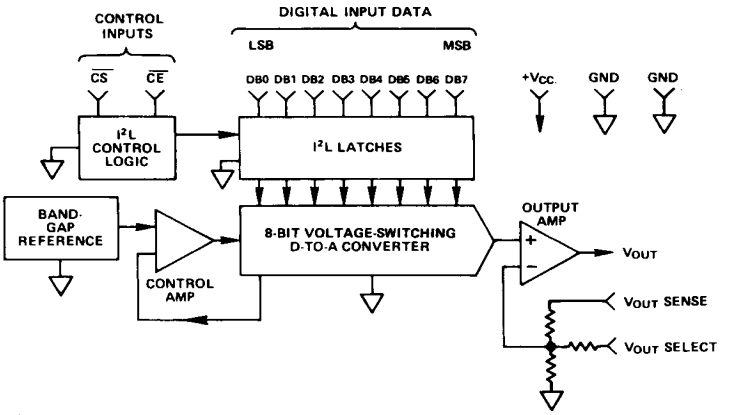
Table 1.

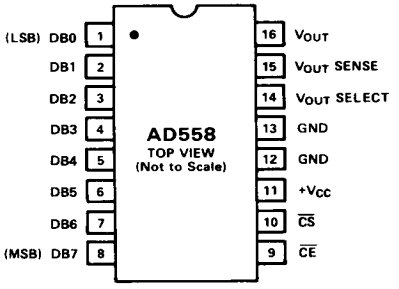
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1]	Units
Relative Accuracy	RA	−1	1/2	1/2	3/4		All Bits with Positive Errors On and All Bits with Negative Errors On	± LSB max
		−2	1/4	1/2	3/8	1/4		
Differential Nonlinearity	DNL	−1, 2	1	1	1		All Major Carriers	± LSB max
Zero Error	V_{OS}	−1	1	1	2	1	All Bits Off	± LSB max
		−2	1/2	1	1	1/2		
Gain Error	A_E	−1	1.5	1.5	2.5	1.5	No Load and 5mA Load	± LSB max
		−2	0.5	1.5	1.0	0.5	All Bits On	
Output Voltage Settling Time		−1, 2	3.0				0 to 10V Range[2]	μs max
			1.5				0 to 2.56V Range[2]	
Power Supply Rejection Ratio	PSRR	−1, 2	0.03	0.03	0.03		Note 3	%/% max
Power Supply Current	I_{CC}	−1, 2	25	25	25		All Bits On	± mA max
Power Dissipation	PD	−1, 2	125	125	125		V_{CC} = +5V All Bits On	mW max
			375	375	375		V_{CC} = +15V All Bits On	
Digital Input High Voltage	V_{IH}	−1, 2	2.0	2.0	2.0			+ V min
Digital Input Low Voltage	V_{IL}	−1, 2	0.8	0.8	0.8			+ V max
Digital Input High Current	I_{IH}	−1, 2	100	100	100		V_{IH} = 7V	± μA max
Digital Input Low Current	I_{IL}	−1, 2	100	100	100		V_{IL} = 0V	± μA max
Write Pulse Width[4]	t_{WR}	−1, 2	200		270			ns min
Data Setup Time[4]	t_{DS}	−1, 2	200		270			ns min
Data Hold Time[4]	t_{DH}	−1, 2	10		10			ns min

NOTES
[1] V_S = +5V for 0 to 2.56V range, V_S = +15V for 0 to 10V range (unless otherwise noted).
[2] Settling time is specified for a positive full scale step to ± 1/2LSB.
[3] V_{CC} = 4.5V to 5.5V for 0 to 2.56V range, V_{CC} = 11.4V to 16.5V for 0 to 10V range.
[4] Timing per Figure 1.

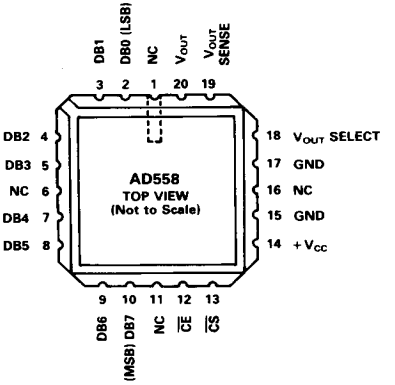
3.2.1 Functional Block Diagram and Terminal Assignments.



D Package (DIP)



E Package (LCC)

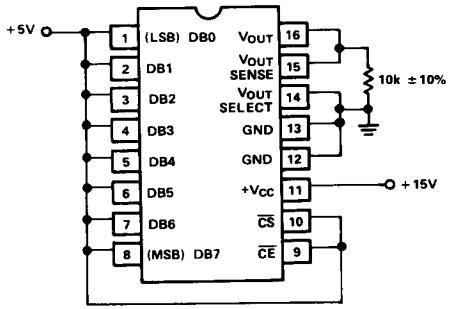


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (56).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



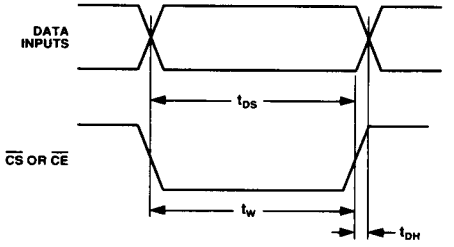


Figure 1. AD558 Timing Diagram

Table 2. AD558 Control Logic Truth Table

Input Data	$\overline{CE}$	$\overline{CS}$	DAC Data	Latch Condition
0	0	0	0	"transparent"
1	0	0	1	"transparent"
0	∫	0	0	latching
1	∫	0	1	latching
0	0	∫	0	latching
1	0	∫	1	latching
X	1	X	previous data	latched
X	X	1	previous data	latched

Notes: X = Does not matter
∫ = Logic Threshold at Positive-Going Transition