512Kx32 FLASH

DESCRIPTION

The EDI7F33512, EDI7F233512 and EDI7F433512 are organized as 512Kx32 and 2x512Kx32 and 4x512Kx32 respectively. The modules are based on AMD's AM29LV004T - 512Kx8 Flash Device in TSOP packages which are mounted on an FR4 substrate.

The modules offer access times between 80 and 120ns allowing for operation of high-speed microprocessors without wait states.

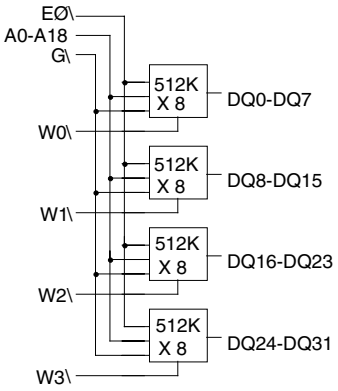
FEATURES

- 512Kx32, 2x512Kx32 and 4x512Kx32 Densities
- Based on AMDs - AM29LV004T Flash Device
- Fast Read Access Time - 80ns
- 3.3- Volt-Only Reprogramming
- Flexible, Sector Architecture
  - One 16Kbyte, two 8Kbyte, one 32Kbyte and seven 64Kbyte sectors
  - Any combination of sectors can be erased
  - Also supports full chip erase
- Embedded Erase Algorithms
  - Automatically preprograms and erases the chip or specified sector
- Embedded Program Algorithms
  - Automatically writes and verifies data at specified address
- Data Polling and Toggle Bit feature for detection of program or erase cycle completion
- Low Power Dissipation
  - 20mA per Device Active Current
  - 10µA per Device CMOS Standby Current
- Typical Endurance >100,000 Cycles
- Single 3.3 Volt ±10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- Commercial and Industrial Temperature Range
- Package
  - 80 Pin SIMM (JEDEC)

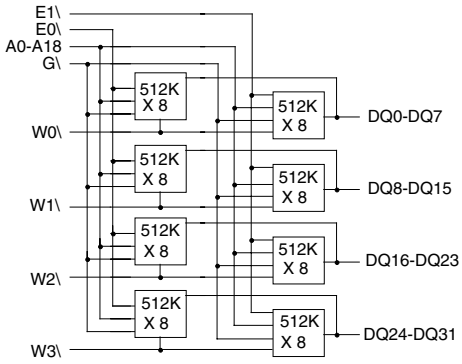
FIG. 1

BLOCK DIAGRAMS

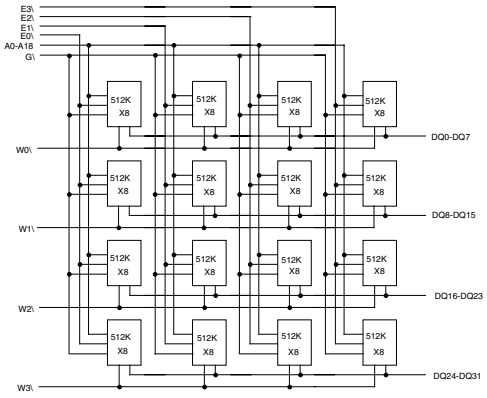
EDI7F33512V-BNC: 512Kx32 80 PIN SIMM



EDI7F233512V-BNC: 2x512Kx32 80 PIN SIMM



EDI7F433512V-BNC: 4x512Kx32 80 PIN SIMM



CAPACITANCE

(f=1.0MHz, VIN = VCC or VSS)

Parameter	Sym	512K Max	2x512K Max	4x512K Max	Unit
Address Lines	CA	35	70	140	pF
Data lines	CDQ	15	30	60	pF
Chip & Write Enable Lines	CC	15	30	60	pF
Output Enable lines	CG	35	70	140	pF

PIN CONFIGURATIONS

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	VSS	21	*	41	A11	61	DQ9
2	VCC	22	*	42	A10	62	DQ8
3	NC	23	*	43	A9	63	DQ7
4	G\	24	*	44	A8	64	DQ6
5	W0\	25	VSS	45	A7	65	DQ5
6	W1\	26	DQ29	461	A6	66	DQ4
7	NC	27	DQ30	47	A5	67	DQ3
8	DQ16	28	DQ31	48	A4	68	DQ2
9	DQ17	29	W2\	49	A3	69	DQ1
10	DQ18	30	NC	50	A2	70	DQ0
11	DQ19	31	NC	51	A1	71	NC
12	DQ20	32	NC	52	AO	72	VCC
13	DQ21	33	NC	53	W3\	73	PD1
14	DQ22	34	A18	54	VSS	74	PD2
15	DQ23	35	A17	55	DQ15	75	PD3
16	DQ24	36	A16	56	DQ14	76	PD4
17	DQ25	37	A15	57	DQ13	77	PD5
18	DQ26	38	A14	58	DQ12	78	PD6
19	DQ27	39	A13	59	DQ11	79	PD7
20	DQ28	40	A12	60	DQ10	80	VSS

**TBD*

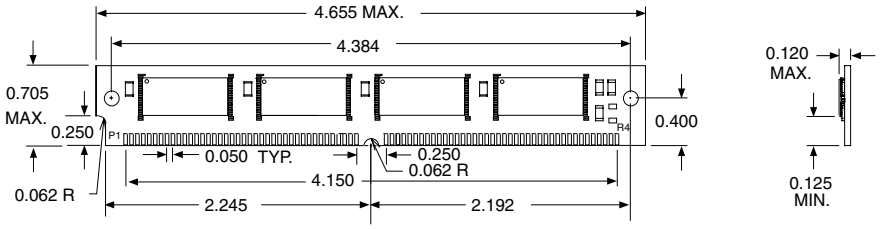
Simm Density			
Pin	2Mb	4Mb	8Mb
21	NC	NC	E3\
22	NC	NC	E2\
23	NC	E1\	E1\
24	E0\	E0\	E0\

Presence Detect Pin Out			
Pin	512K	2x512K	4x512K
PD1	VSS	NC	VSS
PD2	VSS	NC	NC
PD3	VSS	NC	NC
PD4	NC	VSS	VSS

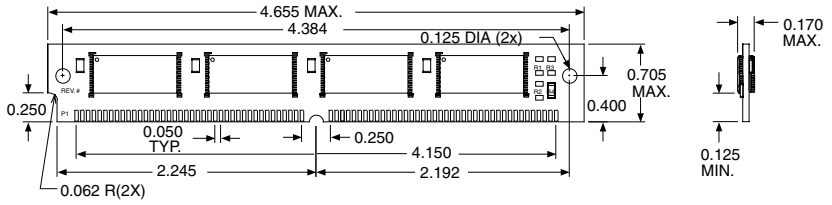
A0-A18	Address input
E0\-E3\	Chip Enable
W0\-W3\	Write Enable
G\	Output Enable
DQ0-DQ31	Data Input/Output
PD	Presence Detect
VCC	Power 3.3V±10%
VSS	Ground
NC	No Connect

ORDERING INFORMATION

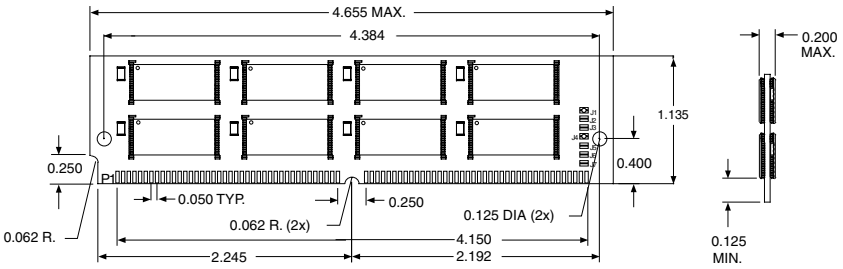
Part Number	Speed (ns)	Package
EDI7F33512V80BNC	80	366
EDI7F33512V90BNC	90	366
EDI7F33512V100BNC	100	366
EDI7F33512V120BNC	120	366



Part Number	Speed (ns)	Package
EDI7F233512V80BNC	80	367
EDI7F233512V90BNC	90	367
EDI7F233512V100BNC	100	367
EDI7F233512V120BNC	120	367



Part Number	Speed (ns)	Package
EDI7F433512V80BNC	80	368
EDI7F433512V90BNC	90	368
EDI7F433512V100BNC	100	368
EDI7F433512V120BNC	120	368



ALL DIMENSIONS ARE IN INCHES

DATASHEET APPROVALS

ECO# 15633

EDI PART NO. EDI7F33512V NEW REV 1A DATE 10/1/02

APPROVAL:	INITIAL	DATE	CORRECTION ON PAGES
~~JUAN GUZMAN~~ L.K.			
~~MUKESH TRIVEDI~~ M.A.			
PAUL MARIEN			
LARRY WINROTH			
DAVE KELLY			
MARK DOWNEY			
DAVE HARRISON			
TONY LEE			
BOB KHEDERIAN			
LUIS ESTELLA			

	YES	NO
WILL THIS DATASHEET GO ON THE WEB?		
IS THIS A NEW DATASHEET?		
WILL THIS DATASHEET REPLACE AN EXISTING DATASHEET THAT'S ALREADY ON THE WEB?		

LINE:_____
FAMILY:_____
PROD.TYPE:_____
ORG:_____
DENSITY:_____
SPEED:_____
PKG:_____
VOLTAGE:_____

IF YES, WHAT DATASHEET IS IT REPLACING? _____

WHAT SECTION SHOULD THIS DATASHEET BE PLACED IN ON THE WEB? _____

AFTER REVIEWING OR MAKING CORRECTIONS ON THE DATASHEET (S)
PLEASE SIGN-OFF ON THIS SHEET AND ,MAKE YOUR CORRECTIONS –ON **THE ORIGINAL COPY(S).**

AFTER REVIEWING THE DATA SHEET, TEST ENGINEERING WILL COMPLETE THE SECTION BELOW.

TEST PROGRAM CHANGE REQUIRED:
YES:_____NO_____DATE:_____

TEST ENGINEER SIGNATURE_____

IF YES, DO NOT RELEASE DATA SHEET UNTIL TEST PROGRAM CHANGE IS COMPLETED.
TEST PROGRAM CHANGE COMPLETION DATE:_____
TEST PROGRAM NAME AND REVISION_____
TEST ENGINEER SIGNATURE_____