

74LS641, LS642, 74LS641-1, LS642-1 Transceivers

Octal Bus Transceiver (Open Collector)
Product Specification

Logic Products

FEATURES

- Octal bidirectional bus interface
- Open Collector Outputs
 - 'LS641, non-inverting
 - 'LS642, inverting
- PNP inputs for reduced loading
- Hysteresis on all Data inputs
- 48mA sink capability ('LS641-1, LS642-1)

FUNCTION TABLE, 'LS641

INPUTS		INPUTS/OUTPUTS	
CE	S/R	A _n	B _n
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	(Z)	(Z)

FUNCTION TABLE, 'LS642

INPUTS		INPUTS/OUTPUTS	
CE	S/R	A _n	B _n
L	L	A = \bar{B}	Inputs
L	H	Inputs	B = \bar{A}
H	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance "off" state

TYPE	TYPICAL PROPAGATION DELAY (A to B)	TYPICAL SUPPLY CURRENT (TOTAL)
74LS641 & -1	17ns	58mA
74LS642 & -1	17ns	58mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V _{CC} = 5V ±5%; T _A = 0°C to +70°C
Plastic DIP	N74LS641N N74LS641-1N N74LS642N N74LS642-1N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

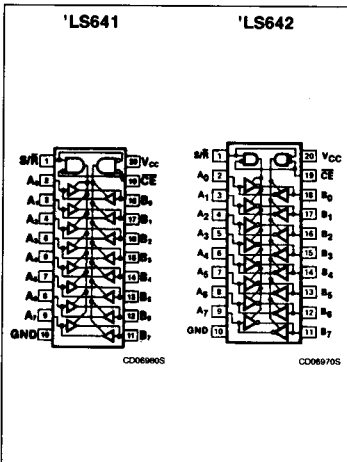
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS & -1
All	Inputs	1LSul
All	Outputs	30LSul

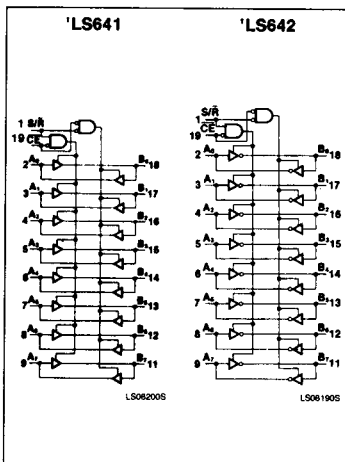
NOTE:

A 74LS unit load (LSul) is 20μA I_{IH} and -0.4mA I_{IL}.

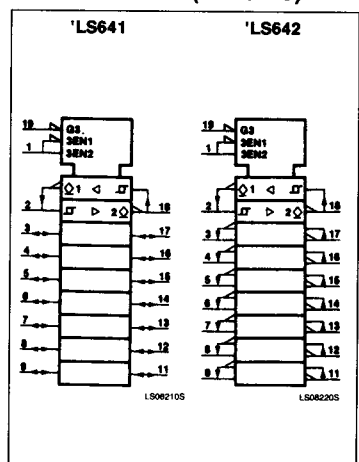
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Transceivers

74LS641, LS642, 74LS641-1, LS642-1

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74LS & -1	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74LS & -1			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			+0.6	V
I _{IK}	Input clamp current			-18	mA
V _{OH}	HIGH-level output voltage			5.5	V
I _{OL}	LOW-level output current			24	mA
		74LS-1 only		48	mA
T _A	Operating free-air temperature	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS641			74LS641-1			UNIT			
		Min	Typ ²	Max	Min	Typ ²	Max				
ΔV _T	Hysteresis (V _{T+} - V _{T-})	V _{CC} = MIN, A or B input			0.2	0.4		0.2	0.4	V	
I _{OH}	HIGH-level output current	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, V _{OH} = 5.5V					100			100	μA
V _{OL}	LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = 12mA		0.25	0.4		0.25	0.4	V	
			I _{OL} = 24mA (74LS)		0.35	0.5		0.35	0.5	V	
			I _{OL} = 48mA (74LS-1)					0.4	0.5	V	
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}					-1.5		-1.5	V	
I _I	Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V	A or B input					0.1	mA	
			V _I = 7.0V	S/ \bar{R} or \overline{CE} input					0.1	mA	
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 2.7V					20		20	μA	
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V					-0.4		-0.4	mA	
I _{CC}	Supply current ³ (total)	V _{CC} = MAX	I _{CC} H Outputs HIGH		48	70		48	70	mA	
			I _{CC} L Outputs LOW		62	90		62	90	mA	
			I _{CC} Z Outputs OFF		64	95		64	95	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- Measure I_{CC} with outputs open.

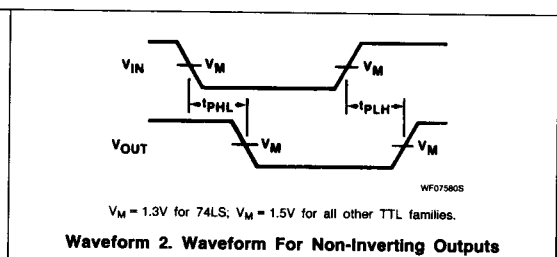
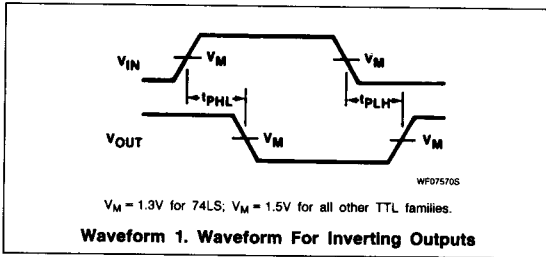
Transceivers

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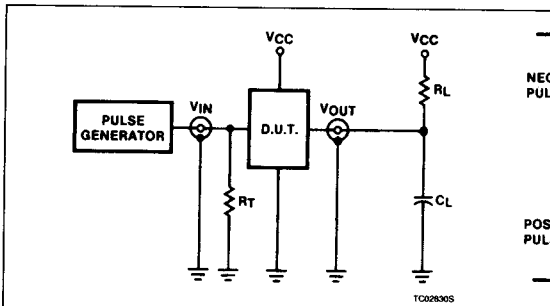
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	$C_L = 45\text{pF}$, $R_L = 667\Omega$		UNIT	
		Min	Max		
t_{PLH} t_{PHL}	Propagation delay A input to B output	Waveform 1		25	ns
t_{PLH} t_{PHL}	Propagation delay B input to A output	Waveform 1		25	ns
t_{PLH}	Propagation delay CE, S/R inputs to A output	Waveform 1		40	ns
	CE input to B output	Waveform 1			
	S/R input to B output	Waveform 2			
t_{PHL}	Propagation delay CE, S/R inputs to A output	Waveform 2		50	ns
	CE input to B output	Waveform 2			
	S/R input to B output	Waveform 1			

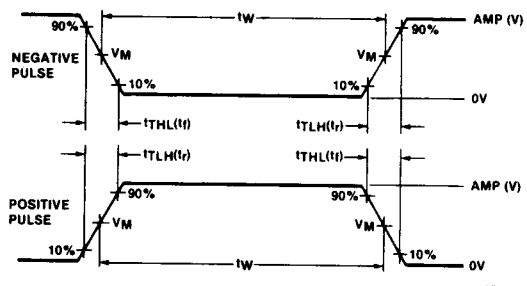
AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Open Collector Outputs



$V_M = 1.3\text{V}$ for 74LS; $V_M = 1.5\text{V}$ for all other TTL families.

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns