ABRIDGED VERSION

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A TDK Group Company

# SSI 34P3216A
## Read Preamp/Channel for Tape Storage

**Advance Information**

February 1996

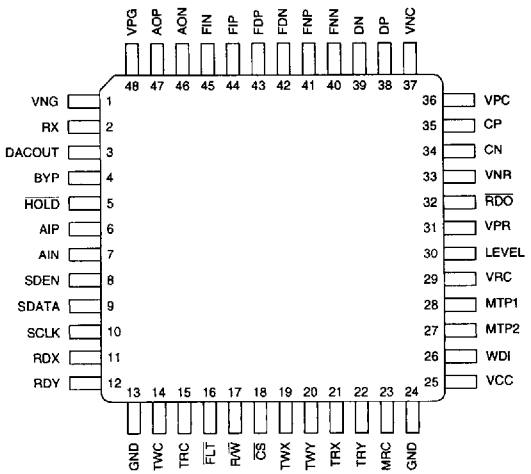
## DESCRIPTION

The SSI 34P3216A is a high performance BiCMOS single chip read channel IC that contains all the functions needed for signal amplification and qualification in tape storage applications, allowing for both MR and thin film tape heads. Functional blocks include the preamplifier, AGC, programmable filter, and pulse detector. Programmable functions of the SSI 34P3216A device are controlled through a bi-directional serial port and banks of internal registers. The SSI 34P3216A utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in a high performance device with low power consumption. The SSI 34P3216A supports a sleep mode for minimal power dissipation in non-operational periods. The SSI 34P3216A provides a low noise read path with selectable gains of 50 V/V and 100 V/V, write current control, and data protection circuitry. Power supply fault protection is provided by disabling the write current generator during power sequencing. A Power Down mode (Idle) is provided to reduce power consumption to less than 20 mW. The SSI 34P3216A requires only a +5V power supply and is available in a 48-lead TQFP package.

## FEATURES

- **Fast attack/decay modes for rapid AGC recovery**
- **Programmable cutoff frequency of 0.4 to 4.0 MHz**
- **Bi-directional serial port for register access**
- **Register programmable power management (Sleep mode <20 mW)**
- **Low Operating Power (400 mW typical @ 5V)**
- **Serial port programmable gain, 100 V/V and 50 V/V**
- **High Performance**
  - **Input noise = 1.2 nV/√Hz max**
  - **Input capacitance = 19 pF max**
  - **Write current range = 5-30 mApk, 5 bit DAC**
  - **Head output voltage swing = 3.0 Vpk min**
- **Designed for two terminal tape, MIG, or MR heads**
- **Power supply fault protection**
- **MRBias current range = 4-20 mA, 6 bit DAC**

## PIN DIAGRAM




**48-lead TQFP**

CAUTION: Use handling procedures necessary for a static sensitive component.

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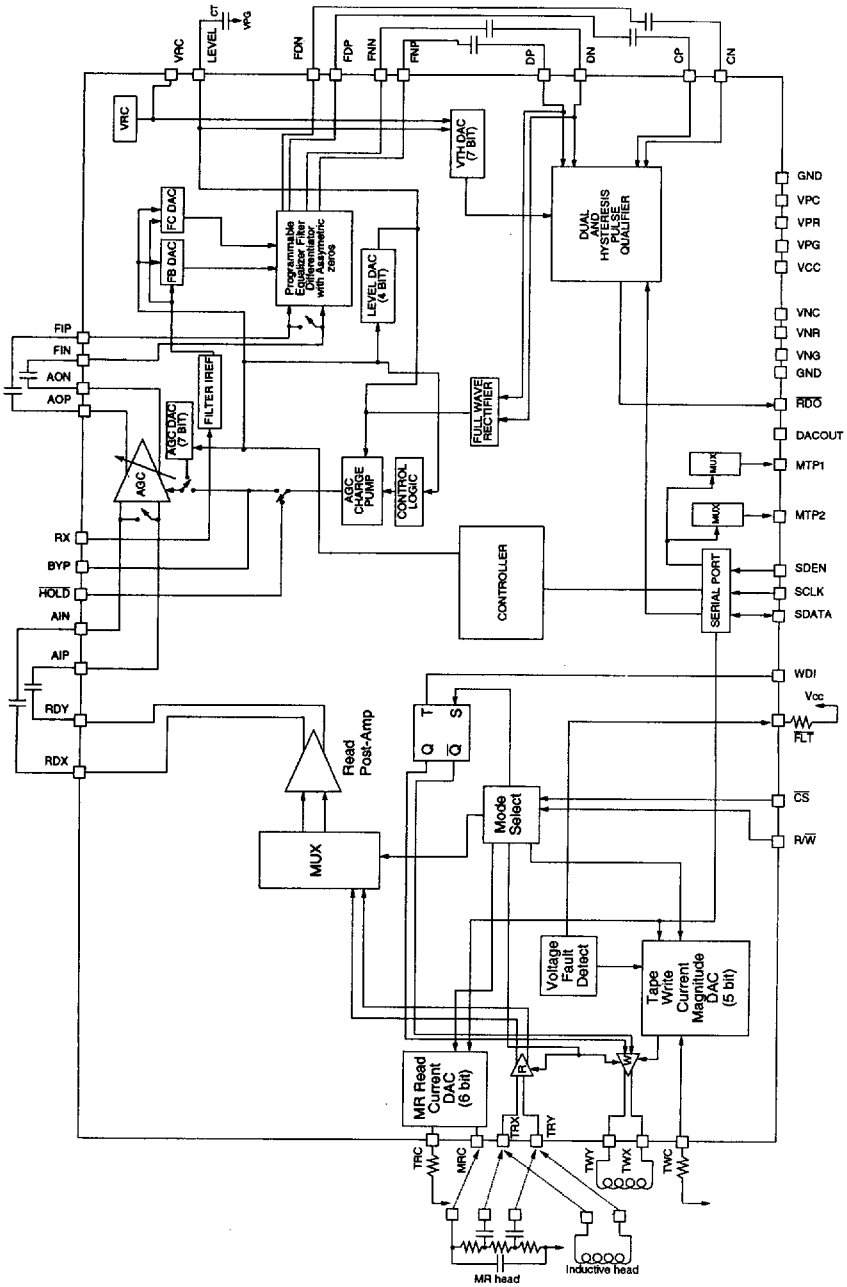
## BLOCK DIAGRAM



## FUNCTIONAL DESCRIPTION

The SSI 34P3216A is a high performance BiCMOS single chip read channel IC that contains all the functions needed for signal amplification and qualification in tape storage applications. Functional blocks include the preamplifier, AGC, programmable filter, and pulse detector. A circuit block diagram is shown in Figure 1.

### PREAMPLIFIER

#### Write Mode

In write mode (R/$\overline{W}$ = low and $\overline{CS}$ = low) the current is conducted through the head alternately into the TWX terminal or the TWY terminal according to the state of an internal flip-flop. The flip-flop is triggered by the negative transition of the Write Data Input line (WDI). A preceding read mode selection initializes the write data flip-flop, WDFF, to pass write current through the "x" side of the head. The write current magnitude for the tape head is determined by the value of an external resistor (Rtwc) connected between TWC and GND, and is given by:

Itw(min) = (Vtwc • 4.8)/Rtwc
Itw = Itw(min) + (1.6 • DAC)/Rtwc
(Rtwc = 2 kΩ, Vtwc = 2V, 0 ≤ DAC ≤ 31)

The tape write current magnitude is adjusted by a five-bit on board D/A converter via the serial port.

#### Read Mode

In read mode, (R/$\overline{W}$ high and $\overline{CS}$ low), the circuit functions as a low noise gain selectable differential amplifier. The read amplifier outputs (RDX, RDY) are emitter follower sources, providing low impedance outputs. The amplifier polarity is non-inverting between TRX, TRY inputs and RDX, RDY outputs. An option for either MR or inductive may be used. If MR is used an MR bias current pin is supplied. This current will have a nominal range of 4-20 mA and 6 bits of resolution. The formula for this current range is as follows:

Imr(min) = (Vtrc • 6.67)/Rtrc
Imr = Imr(min) + (0.833 • DAC)/Rtrc
(Rtrc = 3.33 kΩ, 0 ≤ DAC ≤ 63)

#### Idle Mode

Taking $\overline{CS}$ high selects the Idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

#### Mode Selection And Indication Circuit

Logical control inputs which select mode and head channel are TTL compatible. Their functions are described in Table 1.

**TABLE 1: Mode Select Table**

| $\overline{CS}$ | R/$\overline{W}$ | MODE |
|---|---|---|
| 1 | X | Idle |
| 0 | 1 | Tape Read |
| 0 | 0 | Tape Write |

#### Power Supply Fault Protection

The SSI 34P3216A contains a power supply fault protection circuitry that drives the $\overline{FLT}$ pin low when the power supply is at approximately 3.8V or lower.

### PULSE DETECTOR

The pulse detector, in conjunction with the programmable filter, provides all the data processing functions necessary for detection and qualification of encoded read signals. The signal processing circuits include a wide band variable gain amplifier, a precision wide bandwidth fullwave rectifier, and a dual rate charge pump. The entire signal path is fully-differential to minimize external noise pick up.

#### AGC Circuit

The gain of the AGC amplifier is controlled by the voltage ($V_{BYP}$) stored on the BYP hold capacitor ($C_{BYP}$). A dual rate charge pump drives $C_{BYP}$ with currents that depend on the instantaneous differential voltage at the DP/DN pins. Attack currents lower $V_{BYP}$ which reduces the amplifier gain, while decay currents increase $V_{BYP}$ which increases the amplifier gain. When the signal at DP/DN is greater than 100% of the correct AGC level,

**AGC Circuit** (continued)

the nominal attack current of 0.18 mA is used to reduce the amplifier gain. If the signal is greater than 125% of the programmed AGC level, a fast attack current of eight (8) times nominal is used to reduce the gain. This dual rate approach allows AGC gain to be quickly decreased when it is too high yet minimizes distortion when the proper AGC level has been acquired.

A constant decay current of 4 μA acts to increase the amplifier gain when the signal at DP/DN is less than the programmed AGC level. The large ratio (0.18 mA : 4 μA) of the nominal attack and nominal decay currents enable the AGC loop to respond to the peak amplitudes of the incoming read signal rather than the average value. A fast decay current mode is provided to allow the AGC gain to be rapidly increased, if required. In fast decay mode, the decay current is increased by a factor of 21.

When the chip is in power down mode, the AGC dual rate charge pump is disabled. Upon power up, the Low-Z/fast decay sequence should be executed to rapidly recover from any transients or drift which may have occurred on the BYP hold capacitor.

The AGC amplifier can be set into a fixed gain mode. The gain is programmable over a 2 to 51 V/V range in 0.4 V/V steps by a 7-bit DAC. If the AGC gain DACA = 0, the amplifier is in AGC mode.

### BYP Control Voltage

The BYP capacitor voltage will be held constant (subject to leakage currents) during sleep mode, write mode, or when the $\overline{\text{HOLD}}$ signal is low. Upon the transition of $\overline{\text{CS}}$ from high to low, there is a 1 μs delay inserted before the AGC charge pump is allowed to drive the BYP capacitor.

### AGC Mode Control

When R/$\overline{\text{W}}$ is driven low, the dual rate charge pump is disabled causing the AGC amplifier gain to be held constant. The input impedance of both the AGC amplifier and the programmable filter is reduced also. When the R/$\overline{\text{W}}$ pin transitions from low to high, the Low_Z mode is activated. In this mode, the input impedance at both the AGC amplifier and the programmable filter remain low to allow for quick recovery of the AC coupling capacitors. Directly following the Low_Z mode is the fast decay mode which allows rapid acquisition of the proper AGC level. The duration of the Low_Z and fast decay mode is internally set at a nominal 1 μs. When the pulse detector is powered-down, $V_{BYP}$ will be held constant subject to leakage currents only. Upon power-up, the Low_/fast decay sequence is executed to rapidly recover from any transients or drift which may have occurred on the BYP hold capacitor.

External control for enabling the dual rate charge pump is also provided. Driving the $\overline{\text{HOLD}}$ pin low forces the dual rate charge pump output current to zero. In this mode, $V_{BYP}$ will be held constant subject to leakage currents only.

### RDO Output Pin

A CMOS compatible, 50 ns - 250 ns wide, Raw Data Output ($\overline{\text{RDO}}$) signal is provided. This pin will be placed in high impedance mode when R/$\overline{\text{W}}$ is low to reduce noise and accompanying jitter during write mode. Its falling edge indicates the presence of a valid data pulse.

## QUALIFIER SELECTION

The SSI 34P3216A provides both hysteresis and dual comparator pulse qualification circuits that may be selected for read mode operation. The pulse qualifier method is selected by setting the MSB in the data threshold control register (DTCR). The lower 7 bits of the DTCR also set the hysteresis level of the comparators for read mode.

### Dual Comparator Qualification

When in dual comparator mode, independent positive and negative threshold qualification comparators are used to suppress the error propagation of a positive and negative threshold hysteresis comparator. However a slight amount of hysteresis is included to increase the comparator output time when a signal that just exceeds the threshold level is detected. This eases the timing with respect to the zero crossing clock comparator. A differential comparator with programmable hysteresis threshold allows differential signal qualification for noise rejection. The floating hysteresis threshold, VTH, is driven by a multiplying

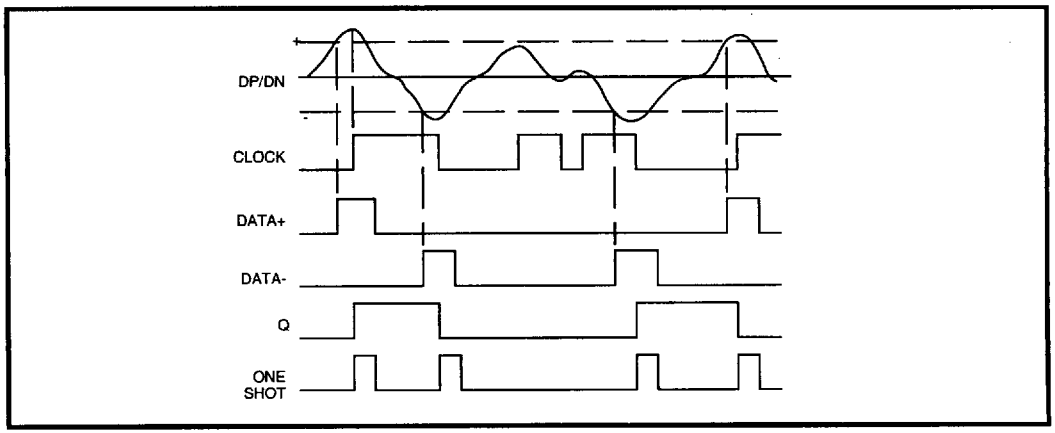



**FIGURE 1: Dual Comparator Timing Diagram**

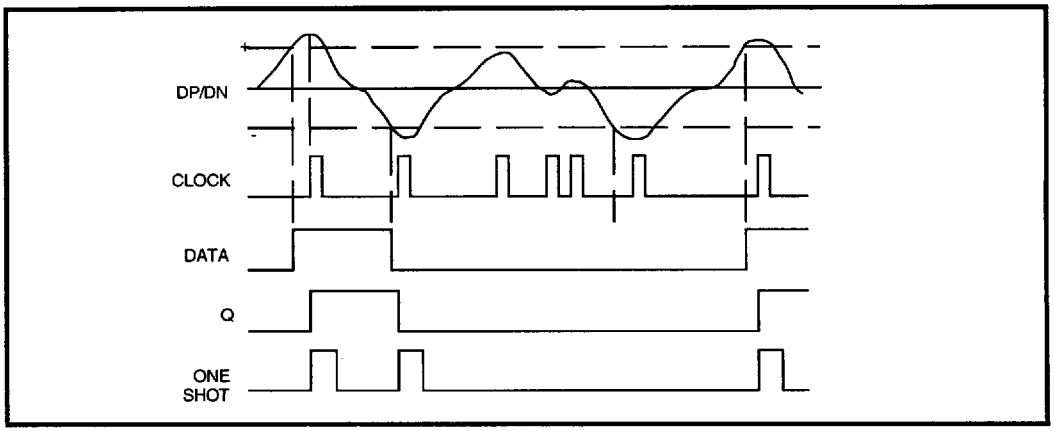



**FIGURE 2: Hysteresis Comparator Timing Diagram**

## DUAL COMPARATOR QUALIFICATION (continued)

DACT which is driven by LEVEL and referenced to VRC. Hysteresis thresholds from 10 to 80% may be set with a resolution of 1%. An external resistor/capacitor combination (RT/CT) can be used to set the hysteresis threshold time constant. A current DACL can also be used to discharge the LEVEL pin. The four LSBs of the Level Decay Register determine the value of the pull-down current. The LSB value of DACL is 3.125 µA, and DACL is offset by 1 LSB such that "0000" corresponds to 3.125 µA, and "1111" results in 50 µA. A qualified signal zero crossing at the CP-CN inputs triggers the output one shot. When Bit 4 of the Level Decay Register is set to zero the threshold is not driven by the LEVEL pin, rather the threshold is driven by a 1V internal reference. In essence the threshold is treated as if the DP/DN signal level is always 1 Vp-pd. Therefore, the programmed data threshold sets a fixed level as opposed to a percentage of the signal envelope. Dual comparator timing is shown in Figure 1.

### Hysteresis Comparator Qualification

When the hysteresis qualification mode is selected, all of the same rules apply to the qualifier section except that the same threshold qualification comparators and clock comparators are used to implement a polarity checking rule. In this mode, a positive peak that clears the established threshold level will set the hysteresis comparator and trigger the bidirectional one-shot that creates the read data pulses. In order to get another pulse clocked out, a peak of the opposite polarity must clear the negative threshold level to reset the hysteresis comparator and trigger the bidirectional one-shot. Hysteresis comparator timing is shown in Figure 2.

## CONTINUOUS-TIME FILTER CIRCUIT

The SSI 34P3216A contains an electronically controlled 7-pole low-pass filter. The transconductance-capacitance ($g_m$-C) filter approximates a linear phase or constant group delay response. Programmable bandwidth and boost/equalization are provided by internal 7-bit control DACs. Differentiation pulse slimming equalization which does not affect the filter's group delay response is accomplished by two programmable complimentary real axis zeros. Programmable phase equalization is also available, providing up to ±20% variation in low-frequency group delay value.

The filter implements a 0.05° equiripple linear phase response. The normalized transfer function (i.e., $s = jw_c = j2\pi f_c = j$, where $j^2 = -1$) is:

$$Vo/Vi = H_{14} \bullet H_2 \bullet H_3$$

where

$$H_{14} = [-2.54628\,\partial\, s^2 + 2.76833\,\beta\, s + 1.13440\,(1 - \partial)] / (s^3 + 2.54628\, s^2 + 2.76833\, s + 1.13440)$$

$$H_2 = 5.37034 / (s^2 + 1.14558\, s + 5.37034)$$

$$H^3 = 2.95139 / (s^2 + 1.54203\, s + 2.95139)$$

The normalized pole frequencies and quality factors of the biquads and bicubic sections are:

w1 = 1.14762 Q1 = 0.68110

w2 = 2.3174 Q2 = 2.02290

w3 = 1.71746 Q3 = 1.11409

w4 = 0.86133

The frequency is denormalized by replacing s by $s/2\pi$ Fc. The parameters ∂ and ß are discussed below. ∂ is always positive, and ß can be positive or negative.

The differential signals from the AGC are AC coupled to the inputs of the filter. The programmable bandwidth and boost/equalization features are controlled by internal DACs whose registers are programmable by the serial port. The current reference for the frequency DACF is set using a single external resistor connected from pin RX to ground. No external components are required for the boost/equalization control.

The programmable bandwidth is set by the filter cutoff DACF according to the following equation.

$$Fc = 4/127 \bullet FCDAC$$

The data mode cutoff register is used to determine the filter's unboosted -3 dB cutoff frequency (Fc). This is the -3 dB frequency for both ∂ and ß equal to 0. When boost/equalization is added, the actual -3 dB point will move out, as discussed below.

The filter's magnitude and group delay characteristics can be altered by adjusting the parameters ∂ and ß. ∂ boosts the filter response at high frequencies while leaving the group delay unaltered. The effect on read data pulses is symmetrical slimming. ß controls the filter's phase or group delay response. ß boost is necessary to correct asymmetry in incoming data pulses. A side effect of ß group delay equalization is a slight change in magnitude response.

**Alpha Boost (magnitude equalization)**

The SSI 34P3216A employs a novel magnitude equalization scheme in which the filter's magnitude characteristics for different values of ∂ pivot around a point of constant gain. The normalized constant gain pivot point is $w_p$ = 0.6675. As shown in Figure 3, for nonzero values of ∂, the filter gain for frequencies above $w_p$ is increased, while frequencies below $w_p$ are attenuated. The advantages of this new technique over the conventional realization, which only boosts higher frequencies, are faster AGC recovery between data and servo modes and reduced AGC dynamic range requirements.

Alpha Boost (∂ ≠ 0, ß = 0) does not affect the filter's group delay response. The amount of alpha boost that will be added to the unboosted -3 dB cutoff frequency (Fc) is set by the Filter Boost DACS according to the following equation:

$$\text{Alpha Boost} = 20 \log_{10} [0.02347 \times \text{DACS} + 1] \text{ (dB)}$$

For example, with DACS set for maximum output, there will be 12 dB of boost added at Fc. This will result in the gain at Fc being 9 dB higher that at DC, versus being -3 dB when unboosted. In absolute values, the DC gain will become -7.35 dB and the gain at Fc will equal 1.65 dB. Table 2 provides information on alpha boost versus ∂ (ß = 0), DACS, DC gain and gain at Fc.

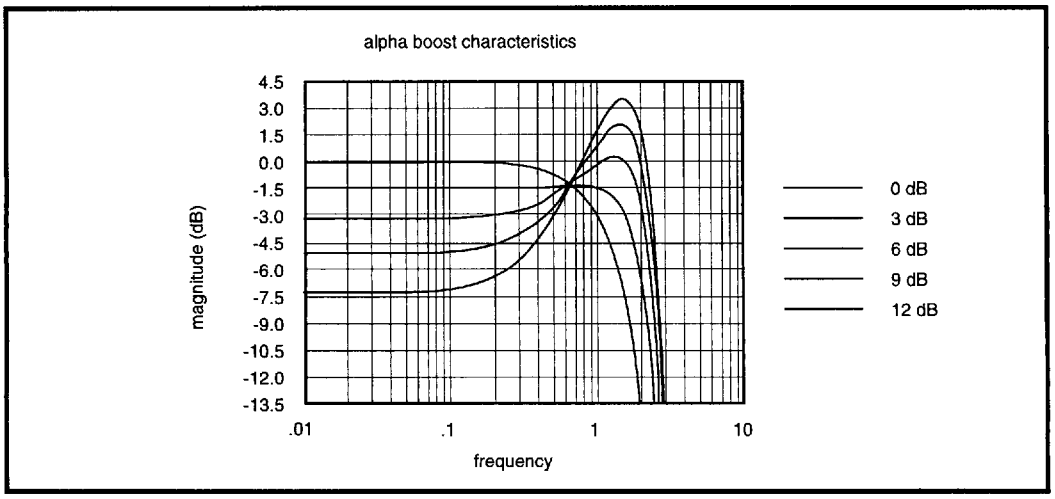



**FIGURE 3: Pivoting Alpha Boost Magnitude Characteristics**

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## FUNCTIONAL DESCRIPTION (continued)

**TABLE 2: Alpha Boost Versus ∂ (ß = 0)**

| ∂ BOOST (DB) | ∂ | DACS | DC GAIN (w = 0) (DB) | GAIN AT FC (DB) |
|---|---|---|---|---|
| 0 | 0.00000 | 0 | 0 | -3 |
| 1 | 0.05156 | 5 | -0.47 | -2.47 |
| 2 | 0.10342 | 11 | -0.95 | -1.95 |
| 3 | 0.15526 | 18 | -1.47 | -1.47 |
| 4 | 0.20671 | 25 | -2.02 | -1.02 |
| 5 | 0.25746 | 33 | -2.59 | -0.59 |
| 6 | 0.30719 | 42 | -3.19 | -0.19 |
| 7 | 0.35562 | 53 | -3.82 | 0.18 |
| 8 | 0.40247 | 64 | -4.48 | 0.52 |
| 9 | 0.44755 | 77 | -5.16 | 0.84 |
| 10 | 0.49066 | 92 | -5.86 | 1.14 |
| 11 | 0.53167 | 109 | -6.59 | 1.41 |
| 12 | 0.57047 | 127 | -7.35 | 1.65 |

If alpha boost is applied, the minimum amount must be 1 dB. DACS values should equal 0 or 5 - 127. Values 1, 2, 3, and 4 are invalid.

**Beta Boost (group delay equalization)**

When ß = 0, the 7-pole filter approximates a constant group delay response delay response in equiripple sense over a normalized frequency range between DC and w ≈ 2. For w = 0, the group delay equals:

$$GDL(0) = 1/(w_1Q_1) + 1/(w_2Q_2) + 1/(w_3Q_3) + 1/w_4(ß = 0)$$

The denormalized filter group delay at DC as a function of Fc is therefore:

$$GDL(0) = 3.17630 / (2\pi Fc) \text{ (seconds, } ß = 0)$$

By applying beta boost (∂ = 0, ß ≠ 0) the group delay response of the filter can be altered, and given a positive or negative slope as shown in Figure 4. The group delay Δ% is defined as the percentage change in absolute group delay value at Fc/10 with respect to that without the equalization applied (ß = 0). The group delay Δ% at low frequencies can be programmed between -20% and +20% by means of DACG which is controlled by two 8-bit registers (allowing independent controls for data and servo modes), with the MSB acting as a sign bit, as follows:

$$\text{Group Delay } \Delta\% = -0.15748 \bullet \text{DACG (\%)}$$

where 0 ≤ DACG ≤ 127 or

$$\text{Group Delay } \Delta\% = 0.15748 \bullet (\text{DACG} - 128) \text{ (\%)}$$

where 128 ≤ DACG ≤ 255

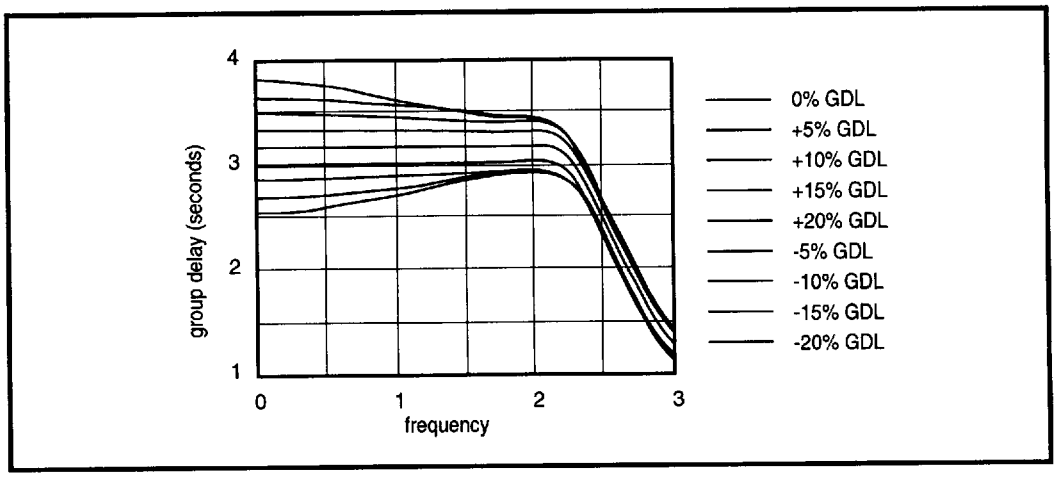


**FIGURE 4: Beta Boost Group Delay Characteristics**

The relationship between ß, DACG and group delay Δ% is given in Table 3.

**TABLE 3: Group Delay Δ%, ß and Beta Boost ($\partial$ = 0)**

| GROUP DELAY (Δ%) | ß | DACG |
|---|---|---|
| -20 | 0.26030 | 127 |
| -15 | 0.19523 | 96 |
| -10 | 0.13015 | 64 |
| -5 | 0.06508 | 32 |
| 0 | 0.00000 | 0 |
| 5 | -0.06508 | 160 |
| 10 | -0.13015 | 192 |
| 15 | -0.19523 | 224 |
| 20 | -0.26030 | 255 |

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## FUNCTIONAL DESCRIPTION (continued)

### Combined Alpha and Beta Boost

A side effect of ß group delay equalization is a small amount of non-pivoting high-frequency magnitude boost. However, when both $\partial \neq 0$ and $ß \neq 0$, the total amount of boost is largely dominated by alpha boost only. Table 4 lists the actual boost versus alpha boost and percentage group delay variation. Figures 5 and 6 illustrate the effect of beta boost for alpha boost equal to 0 dB and 12 dB respectively.

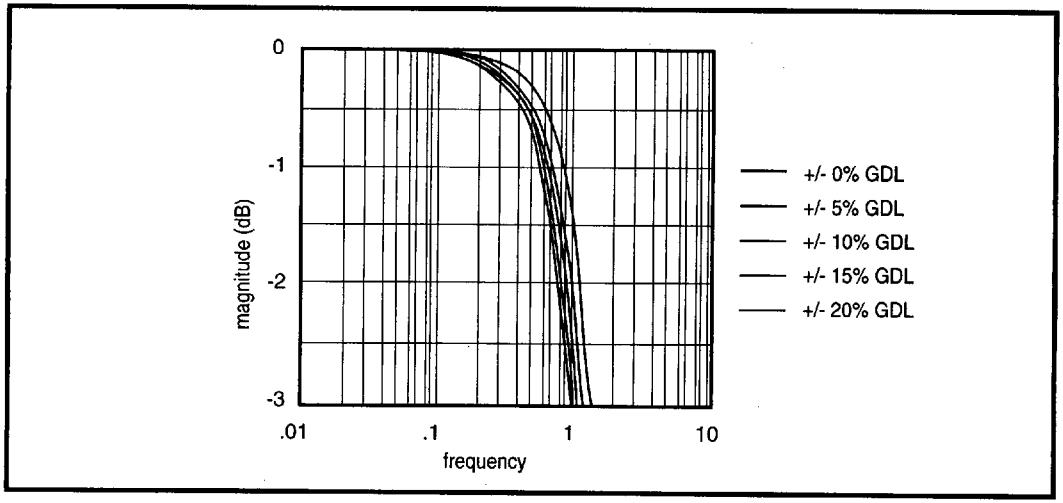



**FIGURE 5: Effect of Beta Boost for Alpha Boost = 0 dB**

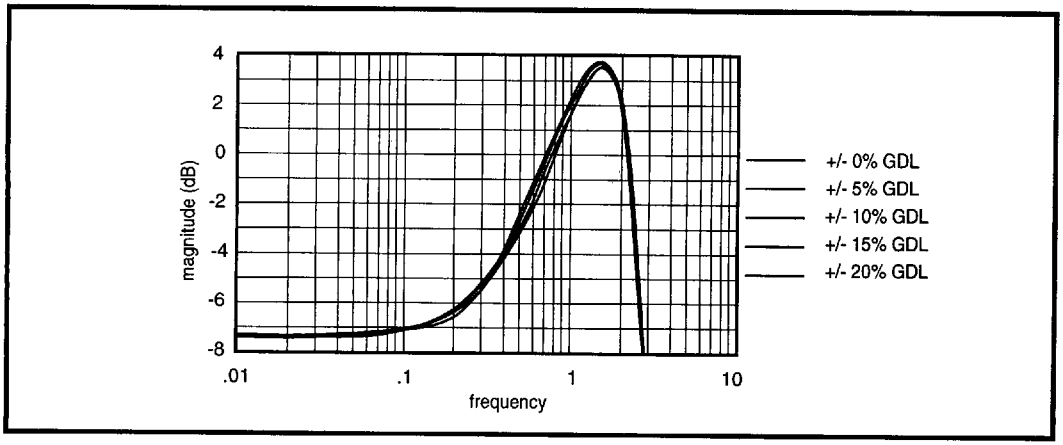



**FIGURE 6: Effect of Beta Boost for Alpha Boost = 12 dB**

**TABLE 4: Actual Boost vs. Alpha Boost and Δ% Group Delay Variation**

| ∂ BOOST (DB) | ±20% | ±15% | ±10% | ±5% | 0% |
|---|---|---|---|---|---|
| 0 | 1.46 | 0.88 | 0.41 | 0.09 | 0.00 |
| 1 | 2.31 | 1.78 | 1.36 | 1.09 | 1.00 |
| 2 | 3.18 | 2.70 | 2.32 | 2.08 | 2.00 |
| 3 | 4.07 | 3.63 | 3.29 | 3.07 | 3.00 |
| 4 | 4.98 | 4.57 | 4.26 | 4.06 | 4.00 |
| 5 | 5.89 | 5.59 | 5.23 | 5.05 | 5.00 |
| 6 | 6.82 | 6.48 | 6.21 | 6.05 | 6.00 |
| 7 | 7.76 | 7.44 | 7.20 | 7.04 | 7.00 |
| 8 | 8.71 | 8.41 | 8.18 | 8.04 | 8.00 |
| 9 | 9.66 | 9.38 | 9.17 | 9.03 | 9.00 |
| 10 | 10.62 | 10.35 | 10.16 | 10.03 | 10.00 |
| 11 | 11.58 | 11.33 | 11.15 | 11.03 | 11.00 |
| 12 | 12.55 | 12.32 | 12.14 | 12.03 | 12.00 |

The -3 dB frequency ($F_{-3\,dB}$) is defined as the frequency for which the filter gain is 3 dB below the gain at DC. For ∂ = 0 and ß = 0, $F_{-3\,dB}$ = Fc and the gain at $F_{-3\,dB}$ equals -3 dB. When boost is applied $F_{-3\,dB}$ increases. As a result of the pivoting alpha boost, the DC gain and hence the gain at $F_{-3dB}$ also changes. Table 5 gives the ratio between Fc and $F_{-3\,dB}$ as a function of alpha boost and Δ% group delay variation and the gain at $F_{-3\,dB}$.

While the amount of boost is defined at Fc, the peak in the magnitude transfer function occurs at a different frequency. Tables 6 and 7 contain the ratios of Fpeak/ Fc and the gain at Fpeak as a function of alpha boost and Δ% group delay variation, respectively.

**TABLE 5: $F_{-3\,dB}$/Fc vs. Alpha Boost and Δ% Group Delay Variation**

| ∂ BOOST (dB) | ±20% | ±15% | ±10% | ±5% | 0% | GAIN AT $F_{-3\,dB}$ (dB) |
|---|---|---|---|---|---|---|
| 0 | 1.32 | 1.18 | 1.07 | 1.02 | 1.00 | -3.00 |
| 1 | 1.54 | 1.41 | 1.30 | 1.23 | 1.21 | -3.47 |
| 2 | 1.76 | 1.66 | 1.58 | 1.52 | 1.51 | -3.95 |
| 3 | 1.95 | 1.89 | 1.85 | 1.81 | 1.80 | -4.47 |
| 4 | 2.12 | 2.09 | 2.06 | 2.04 | 2.04 | -5.02 |
| 5 | 2.25 | 2.23 | 2.21 | 2.21 | 2.20 | -5.59 |
| 6 | 2.35 | 2.34 | 2.33 | 2.33 | 2.33 | -6.19 |
| 7 | 2.44 | 2.43 | 2.43 | 2.43 | 2.43 | -6.82 |
| 8 | 2.52 | 2.52 | 2.51 | 2.51 | 2.51 | -7.48 |
| 9 | 2.60 | 2.59 | 2.59 | 2.59 | 2.59 | -8.16 |
| 10 | 2.67 | 2.67 | 2.66 | 2.66 | 2.66 | -8.86 |
| 11 | 2.74 | 2.73 | 2.73 | 2.73 | 2.73 | -9.59 |
| 12 | 2.81 | 2.80 | 2.80 | 2.80 | 2.80 | -10.35 |

## FUNCTIONAL DESCRIPTION (continued)

**TABLE 6: Fpeak/Fc vs. Alpha Boost and Δ% Group Delay Variation**

| ∂ BOOST (DB) | ±20% | ±15% | ±10% | ±5% | 0% |
|---|---|---|---|---|---|
| 0 | no peak | no peak | no peak | no peak | no peak |
| 1 | no peak | no peak | no peak | no peak | no peak |
| 2 | 0.74 | 0.56 | no peak | no peak | no peak |
| 3 | 0.95 | 0.88 | 0.80 | 0.73 | 0.71 |
| 4 | 1.10 | 1.08 | 1.06 | 1.05 | 1.04 |
| 5 | 1.22 | 1.22 | 1.22 | 1.22 | 1.22 |
| 6 | 1.30 | 1.30 | 1.31 | 1.32 | 1.32 |
| 7 | 1.35 | 1.37 | 1.37 | 1.38 | 1.38 |
| 8 | 1.39 | 1.41 | 1.42 | 1.42 | 1.42 |
| 9 | 1.43 | 1.44 | 1.45 | 1.45 | 1.46 |
| 10 | 1.45 | 1.46 | 1.47 | 1.48 | 1.48 |
| 11 | 1.47 | 1.48 | 1.49 | 1.49 | 1.50 |
| 12 | 1.49 | 1.50 | 1.51 | 1.51 | 1.51 |

**TABLE 7: dB Gain @ Fpeak vs. Alpha Boost and Δ% Group Delay Variation**

| ∂ BOOST (DB) | ±20% | ±15% | ±10% | ±5% | 0% |
|---|---|---|---|---|---|
| 0 | no peak | no peak | no peak | no peak | no peak |
| 1 | no peak | no peak | no peak | no peak | no peak |
| 2 | -0.59 | -0.89 | no peak | no peak | no peak |
| 3 | -0.38 | -0.80 | -1.09 | -1.27 | -1.32 |
| 4 | 0.00 | -0.42 | -0.74 | -0.95 | -1.02 |
| 5 | 0.48 | 0.10 | -0.19 | -0.37 | -0.43 |
| 6 | 1.00 | 0.68 | 0.43 | 0.27 | 0.22 |
| 7 | 1.53 | 1.25 | 1.04 | 0.90 | 0.86 |
| 8 | 2.04 | 1.79 | 1.61 | 1.50 | 1.47 |
| 9 | 2.52 | 2.31 | 2.15 | 2.06 | 2.03 |
| 10 | 2.97 | 2.79 | 2.65 | 2.57 | 2.54 |
| 11 | 3.39 | 3.22 | 3.10 | 3.03 | 3.00 |
| 12 | 3.77 | 3.62 | 3.51 | 3.45 | 3.43 |

## MODE CONTROL

The read/write (R/$\overline{W}$) input controls the device operating mode. Read mode (R/$\overline{W}$ = high) is an asynchronous mode and may be initiated or terminated at any position on the media. Write mode is also an asynchronous mode, but should not be terminated prior to the last output write data pulse.

### Operating Modes and Control

The SSI 34P3216A has several operating modes that support read, write, and power management functions. Mode selection is accomplished by controlling the R/$\overline{W}$ and $\overline{CS}$ pins.

### External Mode Control

All operating modes of the device are controlled by driving the R/$\overline{W}$ and $\overline{CS}$ pins with CMOS compatible signals. For normal operation the $\overline{CS}$ pin is driven low. During normal operation the SSI 34P3216A is controlled by the R/$\overline{W}$ pin. When R/$\overline{W}$ is high the device is in read mode. When R/$\overline{W}$ is low, the device is in write mode.

### DAC Testing and Test Points

TDAC1 and TDAC0 in the Level Decay Register control what signals get multiplexed to the test points and the testing of the DACs. The DACs are tested by monitoring their outputs on DACOUT.

| TDAC1 | TDAC0 | MTP1 | MTP2 | DACOUT |
|---|---|---|---|---|
| 0 | 0 | Disable | Disable | Filter Cutoff DACs |
| 0 | 1 | S2 | R2 | Filter Boost DACs |
| 1 | 0 | RDI | DOUT | Vth Test |
| 1 | 1 | Disable | Disable | threshold DAC |

### Power Down Control

For power management, the $\overline{CS}$ pin can be used in conjunction with R/$\overline{W}$ $\overline{POWER}$ and $\overline{PD}$ $\overline{POWER}$ (bits 6 and 7 of the Tape Write Register) to set the operating mode of the device. When the $\overline{CS}$ pin is brought high ("1") the device is placed into sleep mode (<20 mW) and all circuits are powered down except the serial port circuitry. This allows the user to program the serial port registers while still conserving power. Register information is retained during the sleep mode so it is not necessary to reprogram the serial port registers after returning to an active mode. When the $\overline{CS}$ pin is driven low ("0"), the contents of R/$\overline{W}$ $\overline{POWER}$ and $\overline{PD}$ $\overline{POWER}$ determine which blocks will be active. If R/$\overline{W}$ $\overline{POWER}$ = 0 the preamp will be enabled, and if $\overline{PD}$ $\overline{POWER}$ = 0 the AGC, Filter, and qualifier will also be enabled.

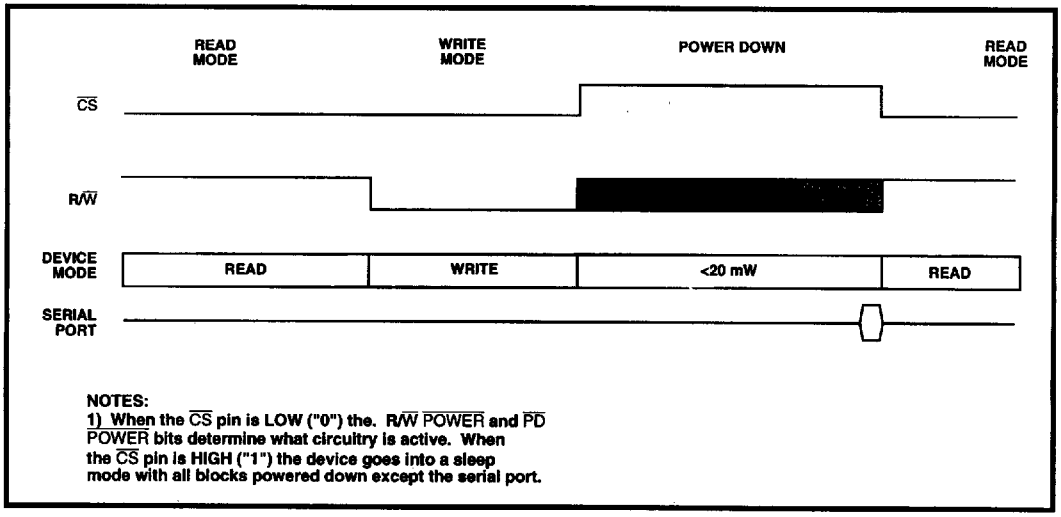



**FIGURE 7: Power Control Timing**

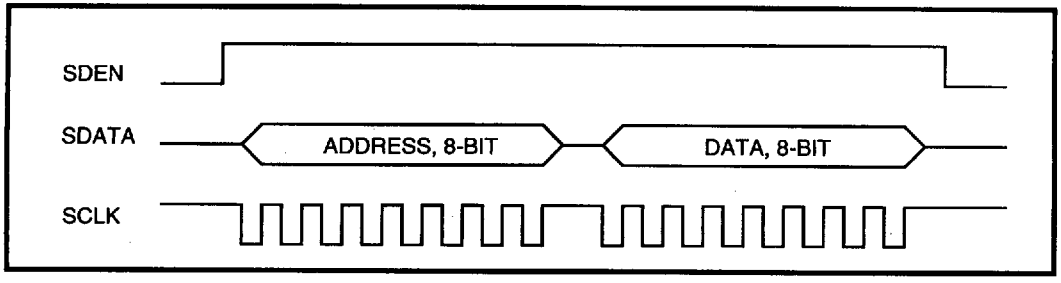



**FIGURE 8: Serial Port Data Transfer Format**

## FUNCTIONAL DESCRIPTION (continued)

### SERIAL INTERFACE

The serial interface is a CMOS bi-directional port for reading and writing programming data from/to the internal registers of the SSI 34P3216A. The serial port data transfer format is shown in Figure 8. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin. After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/W bit which determines if the transfer is a read (1) or a write (0). The remaining 7 bits determine the internal register to be accessed. Table 5 provides register mapping information. The second byte contains the programming data. In read mode (R/W = 1) the SSI 34P3216A will output the register contents of the selected address. In write mode the device will load the selected register with data presented on the SDATA pin. At initial power-up, the contents of the internal registers will be in an unknown state and must be programmed prior to operation. During power down modes, the serial port remains active and register programming data is retained. Detailed timing information is provided in Figure 9.

## REGISTER DESCRIPTION

**Data Mode Cutoff Register** **Address 00010110 = 11d**

| | | |
|---|---|---|
| Bit 7 | DAC Test: | 1 = Filter Cutoff DAC enabled at DACOUT<br>0 = Filter Cutoff DAC disabled at DACOUT |
| Bits 6-0 | Fc Cutoff = 2/127 • DACF | |

**Filter Boost Register** **Address 00000110 = 3d**

| | | |
|---|---|---|
| Bit 7 | DAC Test: | 1 = Filter Boost DAC enabled at DACOUT<br>0 = Filter Boost DAC disabled at DACOUT |
| Bits 6-0 | Alpha Boost = 20 $\log_{10}$ [0.02347 • DACS +1] (dB) | |

**Group Delay Eq. Register** **Address 00110110 = 27d**

| | | |
|---|---|---|
| Bit 7 | Group Delay Sign: | 1 = positive<br>0 = negative |
| Bits 6-0 | Group Delay Magnitude = 0.15748 • DACG | |

**AGC Gain Register** **Address 00100100 = 18d**

| | | |
|---|---|---|
| Bit 7 | FD Test: | 1 = AGC in Fast Discharge Mode (for test only)<br>0 = AGC not in Fast Discharge Mode (normal operation) |
| Bits 6-0 | AGC Gain: | 0 = Closed loop AGC<br>Fixed AGC Gain = 0.39 • DACA + 1.61 |

## REGISTER DESCRIPTION (continued)

**Data Threshold Register** **Address 00010100 = 10d**

| | |
|---|---|
| Bit 7 | Dual Hyst: 1 = Dual Mode (no polarity check)<br>0 = Hyst Mode (polarity check) |
| Bits 6-0 | Data Threshold % = 93/127 • DACT |

**Level Decay Register** **Address 01000100 = 34d**

| | |
|---|---|
| Bit 7 | TDAC1: Refer to DAC Testing and Test Points |
| Bit 6 | TDAC0: Refer to DAC Testing and Test Points |
| Bit 5 | RDIO Test: 1 = RDIO in fast edge mode (for test only)<br>0 = RDIO not in fast edge mode (normal operation) |
| Bit 4 | Threshold: 1 = Level Driven |
| | 0 = Fixed |
| Bits 3-0 | Level Decay Current (μA) = 3.125 • DACL + 3.125 |

**Tape Write Register** **Address 00110100 = 26d**

| | |
|---|---|
| Bit 7 | R/$\overline{W}$ $\overline{POWER}$: 1 = power down<br>0 = power on |
| Bit 6 | $\overline{PD}$ $\overline{POWER}$: 1 = power down<br>0 = power on |
| Bit 5 | Filter Test: 1 = power down<br>0 = power on |
| Bits 4-0 | Itw (mA) = Itw (min) + (1.6 • DACW)/Rtwc Rtwc = 2 kΩ |

**MR Tape Read Register** **Address 01010100 = 42d**

| | |
|---|---|
| Bit 7 | Preamp Gain Select: 1 = 100 V/V 0 = 50 V/V |
| Bit 6 | MR Enable: 1 = Enable<br>0 = Disable |
| Bits 5-0 | Imr (mA) = Imr (min) + (0.833 • DACR)/Rtrc Rtrc = 3.33K |

## PIN DESCRIPTION

### POWER SUPPLY PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VPG | I | Positive Supply |
| VCC | I | Positive Supply |
| VPC | I | Positive Supply |
| VPR | I | Positive Supply |
| VNG | I | Negative Supply |
| GND | I | Negative Supply |
| VNC | I | Negative Supply |
| VNR | I | Negative Supply |

### INPUT PINS

| | | |
|---|---|---|
| $\overline{CS}$ | I | CHIP SELECT: CMOS compatible power control input. A low level CMOS input enables power to circuitry. A high level CMOS input shuts down all circuitry except the serial port. |
| R/$\overline{W}$ | I | READ/WRITE PIN: CMOS compatible read/write input. A high level CMOS input selects read mode. A low level input select write mode. |
| WDI | I | WRITE DATA IN: Negative transition toggles direction of head current |
| AIP, AIN | I | AGC AMPLIFIER INPUTS: Differential AGC amplifier input pins |
| DP, DN | I | ANALOG INPUTS FOR DATA PATH: Differential analog inputs to data comparators, full-wave rectifier |
| CP, CN | I | ANALOG INPUTS FOR CLOCK PATH: Differential analog inputs to the clock comparator. |
| $\overline{HOLD}$ | I | $\overline{HOLD}$ CONTROL: CMOS compatible control pin which, when pulled low, disables the AGC charge pump and holds the AGC amplifier gain at its present value |
| FIP, FIN | I | FILTER SIGNAL INPUTS: The AGC output signals must be AC coupled into these pins |
| TRX, TRY | I | X, Y Tape Read Head Connections |

## PIN DESCRIPTION (continued)

### OUTPUT PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| RDX, RDY | O | X, Y READ DATA: Differential read signal output from the preamp |
| TWX, TWY | O | X, Y TAPE WRITE HEAD CONNECTIONS |
| MTP1-2 | O | MULTIPLEXED TEST POINTS: Open emitter ECL output test points. Internal test signals are routed to these test points as determined by the MCTR MSB register. External resistors are required to use these pins. They should be removed during normal operation to reduce power dissipation. |
| $\overline{RDO}$ | O | READ DATA OUT: CMOS output pin |
| FDP, FDN | O | DIFFERENTIAL DIFFERENTIATED OUTPUTS: Filter differentiated outputs. These outputs are AC coupled into the CP/CN inputs. |
| FNP, FNN | O | DIFFERENTIAL NORMAL OUTPUTS: Filter normal low pass output signals. These outputs are AC coupled into the DP/DN inputs. |
| AOP, AON | O | AGC AMPLIFIER OUTPUT: Differential AGC amplifier output pins. These outputs are AC coupled into the filter inputs (FIP/FIN). |
| $\overline{FLT}$ | O | POWER FAULT DETECTION: Open collector output pin. This outputs a low signal when low power supply (approximately 3.8V) is detected. |
| MRC | O | MR BIAS CURRENT: MR bias current source programmed from a combination of TRC and the serial port |

### ANALOG PINS

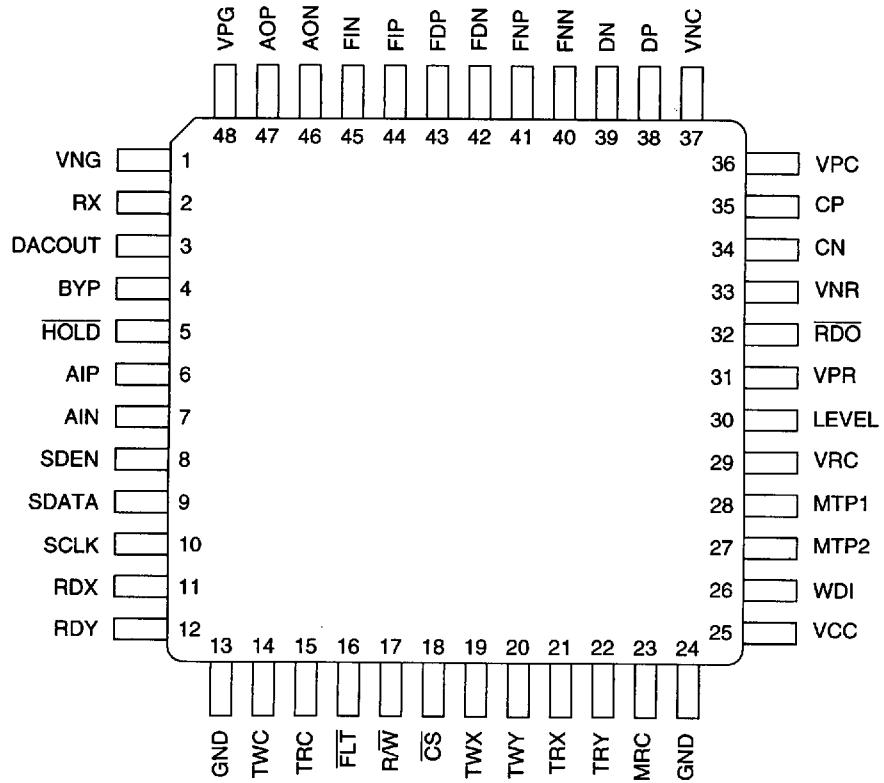
| | | |
|---|---|---|
| TWC | - | TAPE WRITE CURRENT: used to set the magnitude of the write current |
| TRC | - | MR READ CURRENT SET: used to set the magnitude of the MR bias current |
| BYP | - | The AGC read mode integration capacitor $C_{BYP}$, is connected between BYP and VPG |
| DACOUT | O | DAC VOLTAGE TEST POINT / WRITE DAC CURRENT SINK: This test point monitors the outputs of the internal DACs |
| LEVEL | O | An NPN emitter output that provides a full-wave rectified signal from the DP, DN inputs. An external capacitor should be connected from LEVEL to VCC to set the hysteresis threshold time constant in conjunction with the level decay current DACL (Register 34d). |
| RX | I | REFERENCE RESISTOR INPUT: An external 9.09 kΩ, 1% resistor is connected from this pin to VNG to establish a precise reference current for the filter |
| VRC | O | Internal bandgap reference voltage, with respect to VCC |

**SERIAL PORT PINS**

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| SDEN | I | SERIAL DATA ENABLE: CMOS compatible input. A high level input enables the serial port. |
| SDATA | I/O | SERIAL DATA: Bi-directional CMOS compatible pin. NRZ programming data for the internal registers is applied to this input. Writes to registers when R/W bit is 0. Reads from registers when R/W bit is 1. |
| SCLK | I | SERIAL CLOCK: CMOS compatible input. The clock applied to this pin is synchronized with the data applied to SDATA. |

# SSI 34P3216A
# Read Preamp/Channel for Tape Storage

## PACKAGE PIN DESIGNATIONS
(Top View)




**48 - Lead TQFP**

CAUTION: Use handling procedures necessary for a static sensitive component.

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



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