Features

- Zero ppm multiplication error
- Input crystal frequency of 5 - 30 MHz
- Input clock frequency of 4 - 50 MHz
- Output clock frequencies up to 200 MHz
- Peak to Peak Jitter less than 200ps over 200ns interval (100~200MHz)
- Period jitter less than 100ps(70~200MHz)
- Duty cycle of 45/55% up to 120 MHz at +3.3V and 150MHz at +5V
- 9 selectable frequencies controlled by S0, S1 pins
- Operating voltages of 3.0 to 5.5V
- Tri-state output for board level testing

General

The PT7C4511 is a high performance frequency multiplier, which integrates Analog Phase Lock Loop techniques.

The PT7C4511 is the most cost effective way to generate a high quality, high frequency clock output from a lower frequency crystal or clock input. It is designed to replace crystal oscillators in most electronic systems, clock multiplier and frequency translation.

Using Phase-Locked-Loop (PLL) techniques, the device uses a standard fundamental mode, inexpensive crystal to produce output clocks up to 200 MHz.

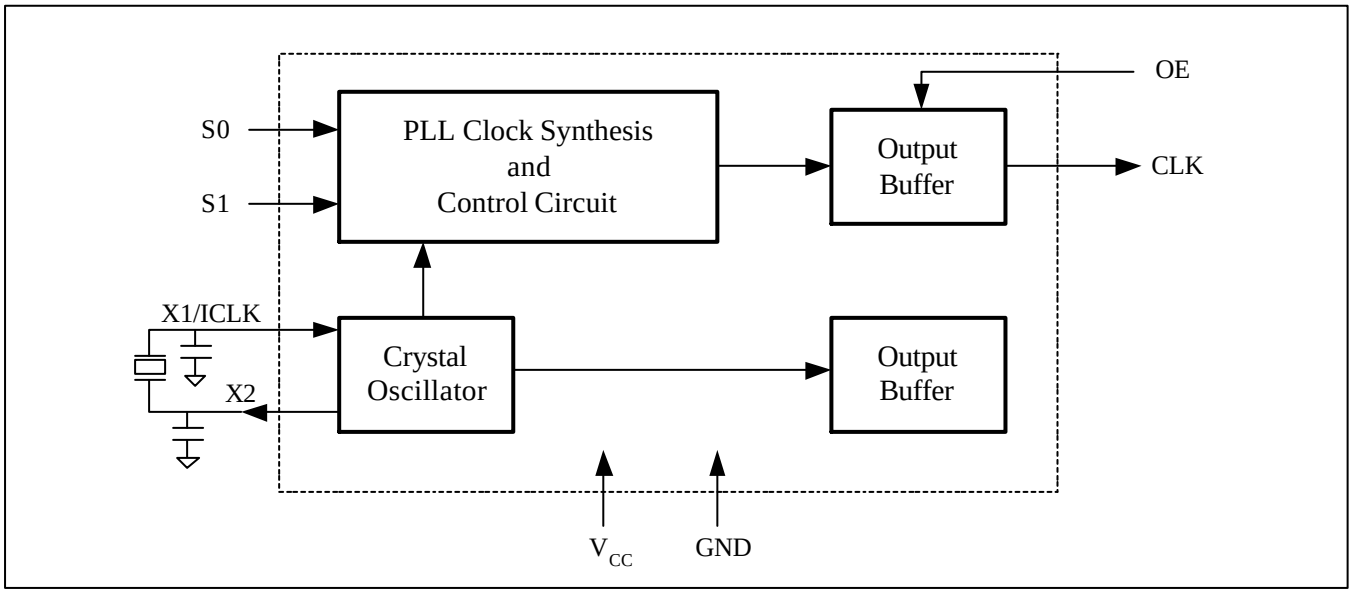
The complex Logic divider is the ability to generate nine different popular multiplication factors, allowing one chip to output many common frequencies.

The device also has an Output Enable pin that tri-states the clock output when the OE pin is taken low. This product is intended for clock generation and frequency translation with low output jitter (variation in the output period)

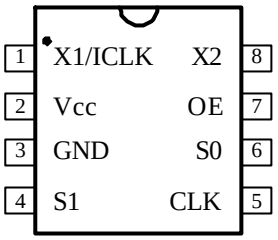
Ordering Information

Part Number	Package
PT7C4511W	8 - Pin SOIC

Block Diagram



Pin Assignment



SOIC-8 package

Pin Description

Pin	Name	Type	Description
1	X1/ICLK	XI	**Crystal connection or clock input.**
2	Vcc	P	Supply voltage: +3.0V to +5.5V.
3	GND	P	Connect to ground.
4	S1	TI	Multiplier select pin 1. Connect to GND or Vcc or float (no connection).
5	CLK	O	Clock output per Table below.
6	S0	TI	Multiplier select pin 0. Connect to GND or Vcc or float (no connection).
7	OE	I	Output Enable. Tri-states CLK output when low. Internal pull-up.
8	X2	XO	Crystal connection. Leave unconnected for clock input.

Clock Output Table

S1	S0	CLK
0	0	×4 [1)]
0	M [2)]	×(16/3)
0	1	×5
M	0	×2.5
M	M	×2
M	1	×(10/3)
1	0	×6
1	M	×3
1	1	×8

1) **Note:** CLK output frequency = ICLK × 4.
2) **Note:** M = leave unconnected (self-biases to Vcc/2).

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested)

Storage temperature ..... -65 to 150°C
Ambient Operating Temperature .....0 to 70°C
Supply Voltage to Ground Potential (V_{CC}) ..... -0.3 to +7.0V
Inputs (Referenced to GND) ..... -0.5 to Vcc+0.5V
Clock Output (Referenced to GND) ..... -0.5 to Vcc+0.5V
Soldering Temperature (Max of 10 seconds) ..... 260°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Sym.	Description	Test condition	Min	Typ	Max	Unit
V_{CC}	Supply Voltage		3		5.5	V
V_{IH}	H-Level Input Voltage		2			V
V_{IL}	L-Level Input Voltage				0.8	V
T_A	Operating Temperature		0		70	°C

DC Electrical Characteristics

(V_{CC} = 3.3V± 0.3V, T_A= 0~70°C, unless noted)

Sym.	Parameter	Test Condition	Pin	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage		Vcc	3		5.5	V
Icc	Supply Current	no load, 20MHz crystal	Vcc		12	20	mA
V_{IH}	Input Logic High		ICLK	(Vcc/2)+1	Vcc/2		V
			OE	2			V
V_{IL}	Input Logic Low		ICLK		Vcc/2	(Vcc/2)-1	V
			OE			0.8	V
V_{IH}	Input Logic High		S0, S1	Vcc-0.5			V
V_{IM}	Input mid-level		S0, S1		Vcc/2		V
V_{IL}	Input Logic Low		S0, S1			0.5	V
V_{OH}	High-level output voltage	I_{OH} = -12mA	CLK	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 12mA	CLK			0.4	V

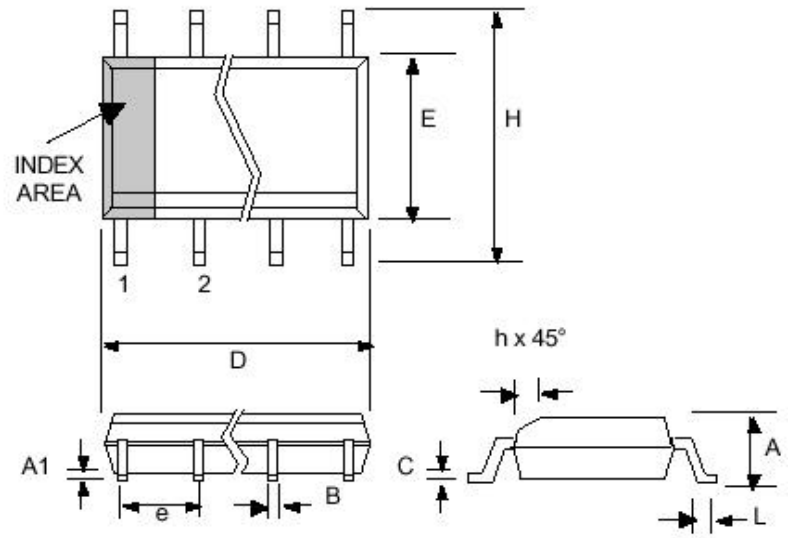
AC Electrical Characteristics

(V_{CC} = 3.3V± 0.3V, T_A = 0~70°C, unless noted)

Sym.	Parameter	Test Condition	Pin	Min.	Typ.	Max.	Unit
f_{IN}	Input Frequency	crystal	ICLK	5		30	MHz
f_{OUT}	Output frequency	V_{CC}: 4.5 to 5.5V	CLK	20		200	MHz
		V_{CC}: 3.0 to 3.6V	CLK	20		180	MHz
t_r	Output clock rise time	0.8 to 2.0V	CLK		1		ns
t_f	Output clock fall time	2.0 to 0.8V	CLK		1		ns
Duty	Output clock duty cycle	At V_{CC}/2,V_{CC}: 3V, up to 120MHz	CLK	45	50	55	%
		At V_{CC}/2,V_{CC}: 5V, up to 150MHz					
	PLL bandwidth			10			kHz
	Output enable time	OE high to output on				50	ns
	Output disable time	OE low to tri-state				50	ns
	Period Jitter	70MHz~200MHz	CLK		50	100	ps
	Jitter over 200ns interval	100MH~200MHz	CLK			200	ps
	Output jitter refer to ICLK	40~150MHz	CLK		100~250		ps

Package Outline and Package Dimensions

(For current dimensional specifications, see JEDEC pub. no. 95.)



8 Pin SOIC

	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.0532	0.0688	1.35	1.75
A1	0.0040	0.0098	0.10	0.24
B	0.0130	0.0200	0.33	0.51
C	0.0075	0.0098	0.19	0.24
D	0.1890	0.1968	4.80	5.00
E	0.1497	0.1574	3.80	4.00
E	0.50BSC		1.27BSC	
H	0.2284	0.2440	5.80	6.20
H	0.0099	0.0195	0.25	0.50
L	0.0160	0.0500	0.41	1.27

Notes

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