OKI Semiconductor MSM7620

Echo Canceller

GENERAL DESCRIPTION

The MSM7620 is an improved version of the MSM7520 with the same basic configuration. The MSM7620 includes following improvements: a modified through mode, timing control of the control pin input, and a thinner package. The MSM7620 also provides a pin-for-pin replacement with the MSM7520.

The MSM7620 is a low-power CMOS IC device for cancelling echo (in an acoustic system or telephone line) generated in a speech path.

Echo is cancelled (in digital signal processing) by estimating the echo path and generating a pseudo-echo signal.

Used as an acoustic echo canceller, the MSM7620 cancels the acoustic echo between the loud speaker and the microphone which occurs during hands free communication, such as on a car phone or a conference system phone.

Used as a line echo canceller, the device cancels the line echo impedance mismatching in a hybrid. In addition, a quality conversation is made possible by controlling the level and preventing howling with a howling detector, double talk detector, attenuation function and a gain control function, and by controlling the silence level with a center clipping function.

The MSM7620 I/O interface supports μ -law PCM. The use of a single chip CODEC, such as the MSM7543, allows the configuration an economic and efficient echo canceller to be configured.

FEATURES

- Handles both acoustic echoes and telephone line echoes.
- Cancellable echo delay time:

MSM7620-001 For a single chip: 27 ms (max.) MSM7620-011 For a cascade connection (can also be used for a single chip) Master chip: 27 ms (max.) Slave chip: 31 ms (max.) Cancelable up to 213 ms (one master plus six slaves)

- For a single chip: 27 ms (max.)
- Echo attenuation : 30 dB (typ.)
- Clock frequency : 18 MHz (36 MHz cannot be used)

External input and internal oscillator circuit are provided.

- Power supply voltage : 5 V (4.5 V to 5.5 V)
- Power consumption : 150 mW (typ.) When powered down: 20 mW (typ.)
- Package options:

32-pin plastic SSOP (SSOP32-P-640-0.80-K) (Product name : MSM7620-001GS-K) 64-pin plastic QFP (QFP64-P-1414-0.80-BK) (Product name : MSM7620-011GS-BK)



BLOCK DIAGRAM MSM7620-001 (Single chip only)





* If the MSM7620-011 is used in the slave mode, only the diagonally hatched blocks and the pins marked with * are used.

PIN CONFIGURATION (TOP VIEW)



32-Pin Plastic SSOP

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	*	9	SIN	17	*	25	SCKO
2	NLP	10	RIN	18	*	26	*
3	HCL	11	SCK	19	*	27	RST
4	ADP	12	SYNC	20	X1/CLKIN	28	WDT
5	V _{SS}	13	SOUT	21	X2	29	GC
6	ATT	14	ROUT	22	*	30	*
7	INT	15	*	23	PWDWN	31	*
8	IRLD	16	V _{SS}	24	SYNCO	32	V _{DD}

*: No connect pin

Note: Pin 26 of the MSM7520 is CKSEL, while that of the MSM7620 is in open state. It is possible to replace the MSM7520 with the MSM7620.



64-Pin Plastic SSOP

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	NLP	17	*	33	PD12	49	*
2	HCL	18	*	34	PD13	50	*
3	ADP	19	PD0	35	X1/CLKIN	51	PD14
4	MS	20	PD1	36	X2	52	PD15
5	ATT	21	PD2	37	*	53	*
6	INT	22	PD3	38	PWDWN	54	SF2
7	*	23	PD4	39	*	55	OF1
8	IRLD	24	PD5	40	SYNCO	56	*
9	*	25	PD6	41	SCKO	57	*
10	SIN	26	PD7	42	*	58	*
11	RIN	27	PD8	43	*	59	SF1
12	SCK	28	PD9	44	RST	60	OF2
13	SYNC	29	PD10	45	WDT	61	*
14	SOUT	30	PD11	46	GC	62	V _{DD}
15	ROUT	31	*	47	V _{DD}	63	*
16	V _{SS}	32	*	48	V _{DD}	64	*

*: No connect pin

Note: Pins 43, 53, and 61 of the MSM7520 are CKSEL, V_{DD}, and TST2 respectively. While these pins of the MSM7620 are in open state, it is possible to replace the MSM7520 with the MSM7620.

PIN DESCRIPTION (1/5)

Т

-

P	in			
32-pin	64-pin	Symbol	Туре	Description
SSOP	QFP			
2	1	NLP	I	 The control pin for the center clipping function. This forces the SOUT output to a minimum value (FF) when the SOUT signal is below -57 dBm0. Effective for reducing low-level noise. Single Chip or Master Chip in a Cascade Connection H: Center clip ON L: Center clip OFF Slave Chip in a Cascade Connection Fixed at L This input signal is loaded in synchronization with the falling edge of the INT signal or the rising edge of the RST signal.
3	2	HCL	1	 The through mode control. When this pin is in the through mode, RIN and SIN data are output to ROUT and SOUT. At the same time, the coefficient of the adaptive FIR filter is cleared. Single Chip or Master Chip in a Cascade Connection H: Through mode L: Normal mode (echo canceller operates) Slave Chip in a Cascade Connection Same as master This input signal is loaded in synchronization with the falling edge of the INT signal or the rising edge of the RST signal.
4	3	ADP	Ι	 AFF coefficient control pin. This pin stops updating of the adaptive FIR filter (AFF) coefficient and sets the coefficient to a fixed value, when this pin is configured to be the coefficient fix mode. This pin is used when holding the AFF coefficient which has been once converged. Single Chip or Master Chip in a Cascade Connection H: Coefficient fix mode L: Normal mode (coefficient update) Slave Chip in a Cascade Connection Fixed at L This input signal is loaded in synchronization with the falling edge of the INT signal or the rising edge of the RST signal.
_	4	MS	I	Selection of the Master Chip and slave chip when used in a cascade connection. L: Single chip or master chip H: Slave chip

Р	in			
32-pin	64-pin	Symbol	Туре	Description
SSOP	QFP			
6	5	ATT	Ι	Control for the ATT function that prevents howling by attenuators (ATT) for the RIN input and SOUT output. If there is input only to RIN, then the ATT for the SOUT output is activated. If there is input only to SIN, or if there is input to both SIN and RIN, the ATT for the RIN input is activated. The attenuations of ATT are approximately 6 dB. • Single Chip or Master Chip in a Cascade Connection H: ATT OFF L: ATT OFF L: ATT ON L is recommended for echo cancellation. • Slave Chip in a Cascade Connection • Fixed at L This input signal is loaded in synchronization with the falling edge of the INT signal or the rising edge of the RST signal.
7	6	ĪNT	I	 Interrupt signal which starts 1 cycle (8 kHz) of the signal processing. Signal processing starts when H-to-L transition is detected. Single Chip or Master Chip in a Cascade Connection Connect the IRLD pin. Slave Chip in a Cascade Connection Connect the IRLD pin of the master chip. INT input is invalid for 100 μs after reset due to initialization. Refer to the control pin connection example.
8	8	IRLD	0	 Load detection signal when the SIN and RIN serial input data are loaded in the internal registers. Single Chip Connect to the INT pin. Master Chip in a Cascade Connection Connect to the INT pin of the master chip and all the slave chips. Slave Chip in a Cascade Connection Leave open. Refer to the control pin connection example.
9	10	SIN	I	Transmit serial data. Input the μ -law PCM signal synchronized to SYNC and SCK. Data is read in at the fall of SCK.

(3/5)

P	in			
32-pin	64-pin	Symbol	Туре	Description
SSOP	QFP			
10	11	RIN		Receive serial data.
				Input the $\mu\text{-law}$ PCM signal synchronized to SYNC and SCK. Data is read in at the fall of SCK.
11	12	SCK	I	Clock pin for transmit/receive serial data. This pin uses the external
				SCK or the SCKO.
				Input the PCM CODEC transmit/receive clock (64 to 2048 kHz).
12	13	SYNC	I	Sync signal for transmit/receive serial data. This pin uses the external
				SYNC or SYNCO.
				Input the PCM CODEC transmit/receive sync signal (8 kHz).
13	14	SOUT	0	Transmit serial data.
				This pin outputs the μ -law PCM signal synchronized to SYNC and SCK.
				This pin is in a high impedance state while there is no data output.
14	15	ROUT	0	Receive serial data.
				This pin outputs the μ -law PCM signal synchronized to SYNC and SCK.
				This pin is in a high impedance state while there is no data output.
_	19	PD0	I/0	Bidirectional bus for parallel data transfer between the Master Chip and
				Slave Chip when used in a cascade connection.
_	30	PD11		The PD15 pin corresponds to MSB.
	33	PD12		This pin is in a high impedance state while there is no data output. Data
	34	PD13		is loaded in at the falling edge of SFx.
	51	PD14		
	52	PD15		
20	35	X1/CLKIN		External input for the basic clock or for the crystal oscillator.
				Input the basic clock (18 MHz).
			-	Refer to the internal clock generator circuit example.
21	36	X2	0	Crystal oscilator.
				Leave this pin open if inputting the basic clock externally.
				This pin is not affected by a reset or power-down.
		DIMENTIN		Retter to the internal clock generator circuit example.
23	38	PWDWN		Power-down mode control.
				L: Power-down mode
				In Normal Operation mode During newer down, all input ning are disabled and output ning are in
				builing power-down, an input pins are disabled and output pins are in
				High impedance · SOUT BOUT DD0 to 15
				$H \cdot \overline{OF1} \cdot \overline{OF2}$
				Holds the last state · WDT IRLD
				Not affected: X2 MCKO
				Reset after power-down is released.

(4/5)

Р	in							
32-pin	64-pin	Symbol	Туре	Description				
SSOP	QFP							
24	40	SYNCO	0	8 kHz sync signal for the PCM CODEC. Connect this pin to the SYNC pin and the PCM CODEC transmit/receive sync pin. Leave it open if using an external SYNC.				
25	41	SCKO	0	Transmit clock signal (200 kHz) for the PCM CODEC. Connect this pin to the SCK pin and the PCM CODEC transmit/receive clock pin. Not affected by reset. Outputs "0" during power-down. Leave it open if using an external SCK.				
27	44	RST	Ι	Reset signal. L: Reset mode H: Normal operation mode During initialization, input signals, except for <u>PWDWN</u> are disabled for 100 μs after reset (after <u>RST</u> is returned from L to H). Input the basic clock during the reset. Output pins during reset are in the following sates : High impedance: SOUT, ROUT, PD0 to 15 L: WDT H: <u>OF1</u> , <u>OF2</u> Not affected: X2, SYNCO, SCKO, <u>IRLD</u> , MCKO				
28	45	WDT	0	Test pin. Leave this pin open.				
29	46	GC		 Input signal for the gain controller when RIN input is controlled and the RIN input level is controlled and howling is prevented. When this pin is "1" the gain controller starts controlling the level above –24 dBm0 of RIN input level and has a control range of 0 to –8.5 dB. Single Chip or Master Chip in a Cascade Connection H: Gain control ON L: Gain control OFF H is recommended for echo cancellation. Slave Chip in a Cascade Connection Fixed at L This pin is loaded in synchronization with the falling edge of the INT signal or the rising edge of RST. 				

P	in			
32-pin	64-pin	Symbol	Туре	Description
SSOP	QFP			
	54	SF2	I	Parallel data transfer flag.
				• Single Chip
				Fixed at H
				Master Chip in a Cascade Connection
				Fixed at H
				Slave Chip in a Cascade Connection
				Connect OF2 of the master chip to the first stage slave chip.
				Connect OF1 of the previous stage slave chip to the second and
				later stage slave chips.
				Refer to the control pin connection example.
_	55	OF1	0	Parallel data transfer flag.
				• Single Chip
				Leave this pin open.
				Master Chip in a Cascade Connection
				Connect to the SF1 of all slaves.
				Slave chip in a Cascade Connection
				Connect to the SF2 of the next stage slave chip.
				Connect the last stage slave chip to the SF1 of the master chip.
				Refer to the control pin connection example.
_	59	SF1	I	Parallel data transfer flag.
				• Single Chip
				Connect OF2.
				Master Chip in a Cascade Connection
				Connect $\overline{OF1}$ of the last stage slave chip.
				Slave Chip in a Cascade Connection
				Connect OF1 of master chip for all slave chips.
				Refer to the control pin connection example.
	60	0F2	0	Parallel data output flag.
				• Single Chip
				Connect to SF1.
				Master Chip in a Cascade Connection
				Connect to $\overline{SF2}$ of the first stage slave chip.
				Slave Chip in a Cascade Connection
				Leave open.
				Refer to the control pin connection example.

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V _{DD}		–0.3 to 7	V
Input Voltage	VIN	Ta = 25°C	-0.3 to V _{DD} + 0.3	V
Power Dissipation	PD		1	W
Storage Temperature	T _{STG}	_	–55 to 150	°C

ABSOLUTE MAXIMUM RATINGS

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
Power Supply Voltage	V _{DD}	—	4.5	5	5.5	V
Power Supply Voltage	V _{SS}	—	_	0	_	V
Input Ligh Voltage	V	Pins other than X1	2.4	_	V _{DD}	V
Input High voltage	VIH	X1 pin	3.5	_	V _{DD}	V
Input Low Voltage	VIL	_	0	_	0.8	V
Operating Temperature Range	Та	—	-40		85	°C

ELECTRICAL CHARACTERISTICS DC Characteristics

 $(Ta = -40^{\circ}C \text{ to } +85^{\circ}C)$

Parameter	Symbol	Con	dition	Min.	Тур.	Max.	Unit
Output High Voltage	V _{OH}	I _{OH} = 40 μA		4.2	_	V _{DD}	V
Output Low Voltage	V _{OL}	I _{0L} = 1.6 mA		0	_	0.4	V
High Level Input Current	IIH	$V_{IH} = V_{DD}$		_	0.1	10	μA
		V _{IL} =	SF1, SF2	-100	-50	-10	μA
Low Level Input Current	Iu	V _{SS} to V _{DD}	with pull-up				•
			Input other than	-10	-0 1	_	ıιΔ
			the above	10	0.1		μπ
High Level Output Current	I _{OZH}	$V_{OH} = V_{DD}$		—	0.1	10	μA
	I _{OZL}	V _{OL} =	PD15 to PD0	100	-50	10	
Low Lovel Output Current		V_{SS} to V_{DD}	with pull-up	-100		10	μΑ
			Input other than	10			
			the above	-10	-0.1	_	μΑ
Power Supply Current						40	
(Operating)	IDDO	-	_	_	30	40	mA
Dower Cumply Current/Ctand by)		When extarnal	input is used		4	F	
Power Supply Current(Stand-by)		as basic clock		_	4	5	mA
	IDDS	When oscillati	on circuit is		0	0	
PWDWN= L		used as basic clock		_	б	8	MA
Input Capacitance	Cı	-	_	_	_	15	pF
Output Load Capacitance	CLOAD	-	_	_		20	pF

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
Echo Attenuation	L _{RES}	R _{IN} = −10 dBm0 (5 kHz band white noise) E. R. L. (echo return loss) = 6 dB T _D = 2 ms ATT, GC, NLP: OFF	_	30	_	dB
Cancellable Echo Delay Time for a Single Chip or a Master Chip in a Cascade	TD	R _{IN} = -10 dBm0 (5 kHz band white noise) E.R.L. = 6 dB			27	ms
Cancellable Echo Delay Time for a Slave Chip in a Cascade	T _{DS}	ATT, GC, NLP: OFF	_	_	31	ms

Echo Canceller Characteristics (Refer to Characteristics Diagram)

AC Characteristics

	(Ta = -40°C				= -40°C to	+85°C)
Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
Clock Frequency	fc	_	17.5	18.0	18.5	MHz
Clock Cycle Time	t _{MCK}	_	54.1	55.56	57.1	ns
Clock Duty Ratio	t _{DMC}	_	40	50	60	%
Clock "H" Level Pulse Width	t _{MCH}	_	23.5	—	—	ns
Clock "L" Level Pulse Width	t _{MCL}	_	23.5	—	—	ns
Clock Rise Time	tr	—	—	—	5	ns
Clock Fall Time	t _f	—	_	_	5	ns
Sync Clock Output Time	t _{DCM}	_	—	—	100	ns
Internal Sync Clock Frequency	f _{CO}	fc = 18 MHz	—	200	—	kHz
Internal Sync Clock Output Cycle Time	t _{CO}	fc = 18 MHz	—	5	—	μs
Internal Sync Clock Duty Ratio	t _{DCO}	fc = 18 MHz	—	50	—	%
Internal Sync Signal Output Delay Time	t _{DCC}	fc = 18 MHz	_	_	5	ns
Internal Sync Signal Period	t _{CYO}	fc = 18 MHz	_	125	—	μs
Internal Sync Signal Output Width	t _{WS0}	fc = 18 MHz	_	t _{CO}	—	μs
Transmit/receive Operation Clock Frequency	f _{SCK}	—	64		2048	kHz
Transmit/receive Sync Clock Cycle Time	t _{SCK}	—	0.488	_	15.6	μs
Transmit/receive Sync Clock Duty Ratio	t _{DSC}	—	40	50	60	%
Transmit/receive Sync Signal Period	t _{CYC}	—	123	125	—	μs
Supe Timing	t _{XS}	—	45	_		ns
	t _{SX}	—	45	_		ns
Sync Signal Width	t _{WSY}	—	t _{SCK}		t _{CYC} -t _{SCK}	μs
Receive Signal Setup Time	t _{DS}	—	45		_	ns
Receive Data Input Time	t _{ID}	—	_	7t _{SCK}	—	μs
IRLD Signal Output Delay Time	t _{DIC}	—	—	_	138	ns
IRLD Signal Output Width	t _{WIR}	—	—	t _{SCK}		μs
Sarial Autout Dalay Tima	t _{SD}	_	_	_	90	
Serial Output Delay Time	t _{XD}		_	_	90	115

AC Characteristics (Continued)

					$(Ta = -40^{\circ}C to +85^{\circ}C)$			
Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit		
Reset Signal Input Width	t _{WR}	—	1	_		μs		
Reset Start Time	t _{DRS}	_	5	_		ns		
Reset End Time	t _{DRE}	_		_	52	ns		
Processing Operation Start Time	t _{DIT}	—	100	_		μs		
Power Down Start Time	t _{DPS}	—		—	111	ns		
Power Down End Time	t _{DPE}	—		_	15	ns		
Control Pin Setup Time (INT)	t _{DTS}	—	20	_	—	ns		
Control Pin Hold Time (INT)	t _{DTH}	_	120	_		ns		
Control Pin Setup Time (RST)	t _{DSR}	—	20	_		ns		
Control Pin Hold Time (RST)	t _{DHR}	—	10	—	—	ns		
Parallel Data Output Signal Width	t _{WPD}	—		2t _{MCK}		ns		
Flag Signal Output Time	t _{DF}	—		t _{MCK}	—	ns		
Flag Signal Output Width	t _{WFO}	—		t _{MCK} /2	—	ns		
Flag Signal Input Width	t _{WFI}	OFz connected to SFx		t _{WFO}		ns		
Data Read Setup Time	t _{FS}	_		20		ns		
Data Read Hold Time	t _{FH}	_	_	10		ns		

t_{FH}

TIMING DIAGRAM Clock Timing



Serial Input Timing



Serial Output Timing



Operation Timing After Reset



Note: INT is invalid in the diagonally shaded interval.

Power Down Timing



*Input MCK in the t_{DPS} interval.

Control Pin Load-in Timing



Parallel Output Timing



Parallel Input Timing



HOW TO USE THE MSM7620

The MSM7620 cancels the echo which returns to SIN using the RIN signal. Connect the base signal to the R-side and the echo generated signal to the S-side.

Connection Methods According to Echos

Example 1: Cancelling acoustic echo (to handle acoustic echo from line input)



Example 2: Cancelling line echo (to handle line echo from microphone input)







Example 4: Cancelling of both acoustic echo and line echo

(to handle both acoustic echo from line input and line echo from microphone input)



Control Pin Connection Example



Four-stage Cascade Connection Master + (slave \times 3)



Internal Clock Generator Circuit Example



ERL vs. echo attenuation RIN input level vs. echo attenuation **40** ∟ 40 L 30 30 Echo attenuation [dB] Echo attenuation [dB] 20 20 10 10 0 0 30 20 -20 40 10 0 -10 -50 -40 -30 -10 0 ERL. [dB] RIN input level [dBm] 0 dBm = 2.2 dBm0 **Measurement Conditions Measurement Conditions** RIN input = -10 dBm 5 kHz band white noise RIN input: 5 kHz band white noise (0 dBm = 2.2 dBm0)Echo delay time $T_D = 2 \text{ ms}$ Echo delay time $T_D = 2 \text{ ms}$ ERL = -6 dBATT, GC, NLP = OFF ATT, GC, NLP = OFF Echo delay time vs. echo attenuation 30 Echo attenuation [dB] 20 10 0 1 2 3 4 5 6 7chip 100 200 0 50 150 Echo delay time [ms] ERL = -6 dB**Measurement Conditions** RIN input = -10 dBmATT, GC, NLP = OFF 5 kHz band white noise The second through seventh chips (0 dBm = 2.2 dBm0)are connected in a cascade.

ECHO CANCELLER CHARACTERISTICS DIAGRAM



Measurement System Block Diagram





Bidirectional Connection Example APPLICATION CIRCUIT

Cascade Connection Example



RECOMMENDATIONS FOR ACTUAL DESIGN

- Set echo return loss (ERL) to be attenuated. If the echo return loss is set to be amplified, the echo can not be eliminated. Refer to the characteristics diagram for ERL vs. echo attenuation quantity.
- 2. Set the level of the analog input so that the PCM CODEC does not overflow.
- 3. The recommended input level is -10 to -20 dBm0. Refer to the characteristics diagram for the RIN input level vs. echo attenuation quantity.
- 4. Applying the tone signal to this echo canceller will decrease echo attenuation. If the tone signal is input to the Sin pin during the time that a signal is input to the Rin pin, this echo canceller operates faultily. A signal must be input to either the Rin pin or the Sin pin. Pins ADP and HCL must be driver at "H" if the tone signal is input to the Sin pin during the time that a signal is input to the Rin pin.
- For changes in the echo path (retransmit, circuit switching during transmission, and so on.), convergence may be difficult. Perform a reset to make it converge. If the state of the echo path changes after a reset, convergence may again be difficult. In cases such as a change in the echo path, perform a reset when possible.
- When turning the power ON, set the PWDWN pin to "1" and input the basic clock simultaneous by with power ON. If powering down immediately after power ON, be sure first input 10 or more clocks of the basic clock.
- 7. After powering ON, be sure to reset.
- 8. After the power down pin is changed to a "1" from a "0", be sure to reset.
- 9. If this canceller is used to cancel acoustic echoes, an echo attenuation may be less than 30 dB.

EXPLANATION OF TERMS

Attenuating Function :	This function prevents howling and controls the noise level with an attenuator for the RIN input and SOUT output. Refer to the
	explanation of pins (ATT pin).
Echo Attenuation :	If there is talking (input only to RIN) in the path of a rising echo arises, the echo attenuation refers to the difference in the echo return loss (cancelled amount) when the echo canceller is not used and when it is used.
	Echo attenuation = (SOUT level during through mode operation) - (SOUT level during echo canceller operation) [dB]
Echo Delay Time :	This is the time from when the signal is output from ROUT until it returns to SIN as an echo or other similar device.
Acoustic Echo :	When using a hands free phone, and so on, the signal output from the speaker echoes and is input again to the microphone. The return signal is referred to as acoustic echo.
Telephone Line Echo :	This is a signal which is delayed midway in a telephone line and returns as an echo, due to reasons such as a hybrid impedance mismatch.
Gain Control Function :	This function prevents howling and controls the sound level by with a gain controller for the RIN input. Refer to the explanation of pins (GC pin).
Center Clipping Function :	This function forces the SOUT output to a minimum value when the signal is below -57 dBm0. Refer to the explanation of pins (NLP pin).
Double Talk Detection :	Double talk refers to a state in which the SIN and RIN signals are input simultaneously. In a double talk state, a signal outside the echo signal which is to be cancelled can be input to the SIN input, resulting in misoperation.
	canceller
Howling Detection :	This is the oscillating state caused by the acoustic coupling between the loud speaker and the microphone during hands free talking. Howling not only interferes with talking, but can also cause in misoperation of the echo canceller.
	The howling detector prevents such misoperation and prevents
Echo Return Loss (ERL) :	howling. When the signal output from ROUT returns to SIN as an echo, ERL refers to how much loss there is in the signal level during ROUT. ERL = (ROUT level) - (SIN level of the ROUT signal which returns as an echo) [dB] If ERL is positive (ROUT > SIN), the system is an attenuator system. If ERL is positive (ROUT > SIN), the system is an attenuator system.
	in Like to negative (NOO1 < 5114), the system is an amplifier system.

PACKAGE DIMENSIONS

(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).