



## Frequency Generator and Integrated Buffer for PENTIUM™

### General Description

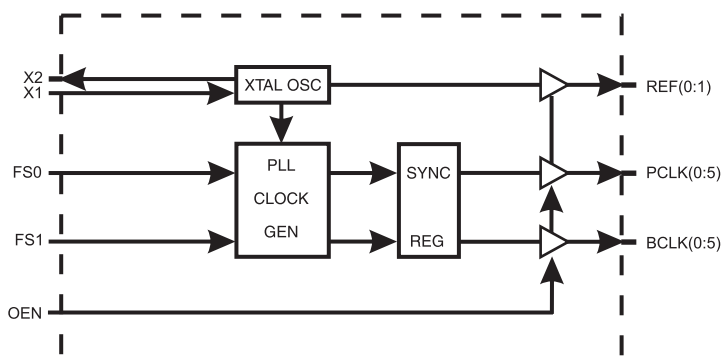
The ICS9159-13 generates all clocks required for high speed RISC or CISC microprocessor systems such as 486, Pentium, PowerPC,™ etc. Four different reference frequency multiplying factors are externally selectable with smooth frequency transitions. A test mode is provided to drive all clocks directly.

High drive BCLK outputs provide typically greater than 1V/ns slew rate into 30pF loads. PCLK outputs provide typically better than 1V/ns slew rate into 20pF loads while maintaining 50±5% duty cycle.

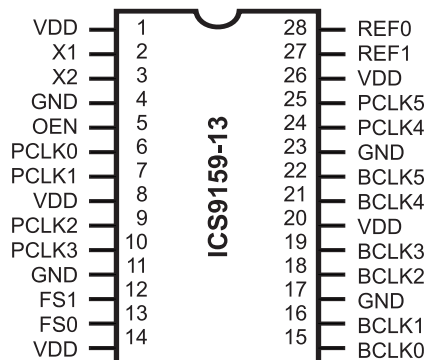
### Features

- Generates up to six processor and six bus clocks, plus two reference clocks
- Synchronous clocks skew matched to 250ps window on PCLKs and 500ps window on BCLKs
- Processor and bus clocks synchronized to each other, PCLK to BCLK skew window 600ps max
- Test clock mode eases system design
- 3.0V - 5.5V supply range
- 28-pin SOIC package

### Block Diagram



### Pin Configuration



### 28-Pin SOIC

### Functionality

| OEN | FS1 | FS0 | PCLK     | BCLK     | REF        |
|-----|-----|-----|----------|----------|------------|
| 1   | 0   | 0   | 50MHz    | 25 MHz   | 14.318 MHz |
| 1   | 0   | 1   | 66.6 MHz | 33.3 MHz | 14.318 MHz |
| 1   | 1   | 0   | 60 MHz   | 30 MHz   | 14.318 MHz |
| 1   | 1   | 1   | TCLK/2   | TCLK/4   | TCLK       |
| 0   | X   | X   | Tristate | Tristate | Tristate   |



# ICS9159-13

## Pin Descriptions

| PIN NUMBER                | PIN NAME  | TYPE | DESCRIPTION                                                                                                                                                |
|---------------------------|-----------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 8, 14, 20, 26          | VDD       | PWR  | Power for logic, CPU and fixed frequency output buffers.                                                                                                   |
| 2                         | X1        | IN   | XTAL or external reference frequency input. This input includes XTAL load capacitance and feedback bias for a 12 - 16 MHz crystal, nominally 14.31818 MHz. |
| 3                         | X2        | OUT  | XTAL output which includes XTAL load capacitance.                                                                                                          |
| 4, 11, 17, 23             | GND       | PWR  | Ground for logic, CPU and fixed frequency output buffers.                                                                                                  |
| 6, 7, 9, 10,<br>24, 25    | PCLK(0:3) | OUT  | Processor clock outputs which are a multiple of the input reference frequency as shown in the table above.                                                 |
| 13, 12                    | FS(0:1)   | IN   | Frequency multiplier select pins. See table above. These inputs have internal pull-up devices.                                                             |
| 15, 16, 18, 19,<br>21, 22 | BCLK(0:5) | OUT  | Bus clock outputs are fixed at one half the PCLK frequency.                                                                                                |
| 5                         | OEN       | IN   | OEN tristates all outputs when low. This input has an internal pull-up device.                                                                             |
| 28, 27                    | REF(0:1)  | OUT  | REF is a buffered copy of the crystal oscillator or reference input clock, nominally 14.31818 MHz.                                                         |



## Absolute Maximum Ratings

|                                     |                                |
|-------------------------------------|--------------------------------|
| Supply Voltage .....                | 7.0 V                          |
| Logic Inputs .....                  | GND –0.5 V to $V_{DD} + 0.5$ V |
| Ambient Operating Temperature ..... | 0°C to +70°C                   |
| Storage Temperature .....           | –65°C to +150°C                |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## Electrical Characteristics at 3.3V

$V_{DD} = 3.0 - 3.7$  V,  $T_A = 0 - 70^\circ\text{C}$  unless otherwise stated

| DC Characteristics               |          |                                           |             |       |             |               |
|----------------------------------|----------|-------------------------------------------|-------------|-------|-------------|---------------|
| PARAMETER                        | SYMBOL   | TEST CONDITIONS                           | MIN         | TYP   | MAX         | UNITS         |
| Input Low Voltage                | $V_{IL}$ |                                           | -           | -     | $0.2V_{DD}$ | V             |
| Input High Voltage               | $V_{IH}$ |                                           | $0.7V_{DD}$ | -     | -           | V             |
| Input Low Current                | $I_{IL}$ | $V_{IN}=0\text{V}$                        | -28.0       | -10.5 | -           | $\mu\text{A}$ |
| Input High Current               | $I_{IH}$ | $V_{IN}=V_{DD}$                           | -5.0        | -     | 5.0         | $\mu\text{A}$ |
| Output Low Current <sup>1</sup>  | $I_{OL}$ | $V_{OL}=0.8\text{V}$ ; for PCLKS & BCLKS  | 30.0        | 47.0  | -           | mA            |
| Output High Current <sup>1</sup> | $I_{OH}$ | $V_{OL}=2.0\text{V}$ ; for PCLKS & BCLKS  | -           | -66.0 | -42.0       | mA            |
| Output Low Current <sup>1</sup>  | $I_{OL}$ | $V_{OL}=0.8\text{V}$ ; for REF CLKs       | 25.0        | 38.0  | -           | mA            |
| Output High Current <sup>1</sup> | $I_{OH}$ | $V_{OL}=2.0\text{V}$ ; for REF CLKs       | -           | -47.0 | -30.0       | mA            |
| Output Low Voltage <sup>1</sup>  | $V_{OL}$ | $I_{OL}=15\text{mA}$ ; for PCLKS & BCLKS  | -           | 0.3   | 0.4         | V             |
| Output High Voltage <sup>1</sup> | $V_{OH}$ | $I_{OH}=-30\text{mA}$ ; for PCLKS & BCLKS | 2.4         | 2.8   | -           | V             |
| Output Low Voltage <sup>1</sup>  | $V_{OL}$ | $I_{OL}=12.5\text{mA}$ ; for REF CLKs     | -           | 0.3   | 0.4         | V             |
| Output High Voltage <sup>1</sup> | $V_{OH}$ | $I_{OH}=-20\text{mA}$ ; for REF CLKs      | 2.4         | 2.8   | -           | V             |
| Supply Current                   | $I_{DD}$ | @66.5 MHz; all outputs unloaded           | -           | 55    | 110         | mA            |

**Note 1:** Parameter is guaranteed by design and characterization. Not 100% tested in production.



# ICS9159-13

## Electrical Characteristics at 3.3V

$V_{DD} = 3.1 - 3.7\text{ V}$ ,  $T_A = 0 - 70^\circ\text{C}$

| AC Characteristics                          |            |                                                                                       |      |        |      |       |
|---------------------------------------------|------------|---------------------------------------------------------------------------------------|------|--------|------|-------|
| PARAMETER                                   | SYMBOL     | TEST CONDITIONS                                                                       | MIN  | TYP    | MAX  | UNITS |
| Rise Time <sup>1</sup>                      | $T_{r1}$   | 20pF load, 0.8 to 2.0V PCLK & BCLK                                                    | -    | 0.9    | 1.5  | ns    |
| Fall Time <sup>1</sup>                      | $T_{f1}$   | 20pF load, 2.0 to 0.8V PCLK & BCLK                                                    | -    | 0.8    | 1.4  | ns    |
| Rise Time <sup>1</sup>                      | $T_{r2}$   | 20pF load, 20% to 80% PCLK & BCLK                                                     | -    | 1.5    | 2.5  | ns    |
| Fall Time <sup>1</sup>                      | $T_{f2}$   | 20pF load, 80% to 20% PCLK & BCLK                                                     | -    | 1.4    | 2.4  | ns    |
| Duty Cycle <sup>1</sup>                     | $D_t$      | 20pF load @ $V_{OUT}=1.4\text{V}$                                                     | 45   | 50     | 55   | %     |
| Jitter, One Sigma <sup>1</sup>              | $T_{j1s1}$ | PCLK & BCLK Clocks;<br>Load=20pF, $F_{OUT}>25\text{ MHz}$                             | -    | 50     | 150  | ps    |
| Jitter, Absolute <sup>1</sup>               | $T_{jab1}$ | PCLK & BCLK Clocks;<br>Load=20pF, $F_{OUT}>25\text{ MHz}$                             | -250 | -      | 250  | ps    |
| Jitter, One Sigma <sup>1</sup>              | $T_{j1s2}$ | REF CLK; Load=20pF                                                                    | -    | 1      | 3    | %     |
| Jitter, Absolute <sup>1</sup>               | $T_{jab2}$ | REF CLK; Load=20pF                                                                    | -5   | 2      | 5    | %     |
| Input Frequency <sup>1</sup>                | $F_i$      |                                                                                       | 12.0 | 14.318 | 16.0 | MHz   |
| Logic Input Capacitance <sup>1</sup>        | $C_{IN}$   | Logic input pins                                                                      | -    | 5      | -    | pF    |
| Crystal Oscillator Capacitance <sup>1</sup> | $C_{INX}$  | X1, X2 pins                                                                           | -    | 18     | -    | pF    |
| Power-on Time <sup>1</sup>                  | $t_{on}$   | From $V_{DD}=1.6\text{V}$ to 1 st crossing of 66.5 MHz<br>$V_{DD}$ supply ramp < 40ms | -    | 2.5    | 4.5  | ms    |
| Frequency Settling Time <sup>1</sup>        | $t_s$      | From 1st crossing of acquisition to <<br>1% settling                                  | -    | 2.0    | 4.0  | ms    |
| Clock Skew Window <sup>1</sup>              | $T_{sk1}$  | PCLK to PCLK; Load=20pF; @1.4V                                                        | -    | 150    | 250  | ps    |
| Clock Skew Window <sup>1</sup>              | $T_{sk2}$  | BCLK to BCLK; Load=20pF; @1.4V                                                        | -    | 300    | 500  | ps    |
| Clock Skew Window <sup>1</sup>              | $T_{sk3}$  | PCLK to BCLK; Load=20pF; @1.4V                                                        | -    | 400    | 600  | ps    |

**Note 1:** Parameter is guaranteed by design and characterization. Not 100% tested in production.



## Electrical Characteristics at 5.0V

$V_{DD} = 4.5 - 5.5 \text{ V}$ ,  $T_A = 0 - 70^\circ \text{ C}$

| DC Characteristics               |          |                                           |      |        |       |               |
|----------------------------------|----------|-------------------------------------------|------|--------|-------|---------------|
| PARAMETER                        | SYMBOL   | TEST CONDITIONS                           | MIN  | TYP    | MAX   | UNITS         |
| Input Low Voltage                | $V_{IL}$ |                                           | -    | -      | 0.8   | V             |
| Input High Voltage               | $V_{IH}$ |                                           | 2.4  | -      | -     | V             |
| Input Low Current                | $I_{IL}$ | $V_{IN}=0\text{V}$                        | -45  | -15    | -     | $\mu\text{A}$ |
| Input High Current               | $I_{IH}$ | $V_{IN}=V_{DD}$                           | -5.0 | -      | 5.0   | $\mu\text{A}$ |
| Output Low Current <sup>1</sup>  | $I_{OL}$ | $V_{OL}=0.8\text{V}$ ; for PCLKS & BCLKS  | 36.0 | 62.0   | -     | mA            |
| Output High Current <sup>1</sup> | $I_{OH}$ | $V_{OL}=2.0\text{V}$ ; for PCLKS & BCLKS  | -    | -152   | -90.0 | mA            |
| Output Low Current <sup>1</sup>  | $I_{OL}$ | $V_{OL}=0.8\text{V}$ ; for REF CLKs       | 30.0 | 50.0   | -     | mA            |
| Output High Current <sup>1</sup> | $I_{OH}$ | $V_{OL}=2.0\text{V}$ ; for REF CLKs       | -    | -110.0 | -65.0 | mA            |
| Output Low Voltage <sup>1</sup>  | $V_{OL}$ | $I_{OL}=20\text{mA}$ ; for PCLKS & BCLKS  | -    | 0.25   | 0.4   | V             |
| Output High Voltage <sup>1</sup> | $V_{OH}$ | $I_{OH}=-70\text{mA}$ ; for PCLKS & BCLKS | 2.4  | 4.0    | -     | V             |
| Output Low Voltage <sup>1</sup>  | $V_{OL}$ | $I_{OL}=15\text{mA}$ ; for REF CLKs       | -    | 0.2    | 0.4   | V             |
| Output High Voltage <sup>1</sup> | $V_{OH}$ | $I_{OH}=-50\text{mA}$ ; for REF CLKs      | 2.4  | 4.7    | -     | V             |
| Supply Current                   | $I_{DD}$ | @66.5 MHz; all outputs unloaded           | -    | 80.0   | 160.0 | mA            |

**Note 1:** Parameter is guaranteed by design and characterization. Not 100% tested in production.



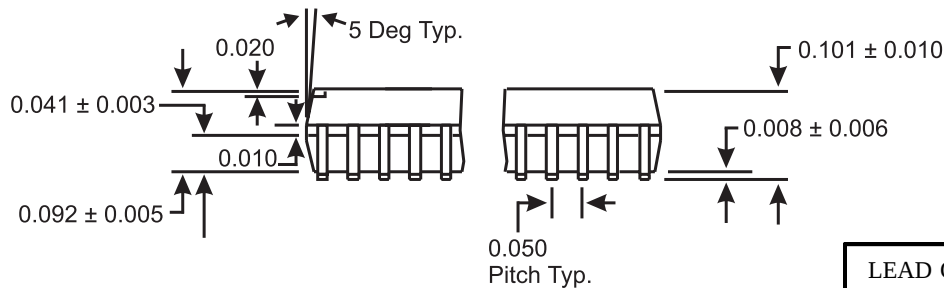
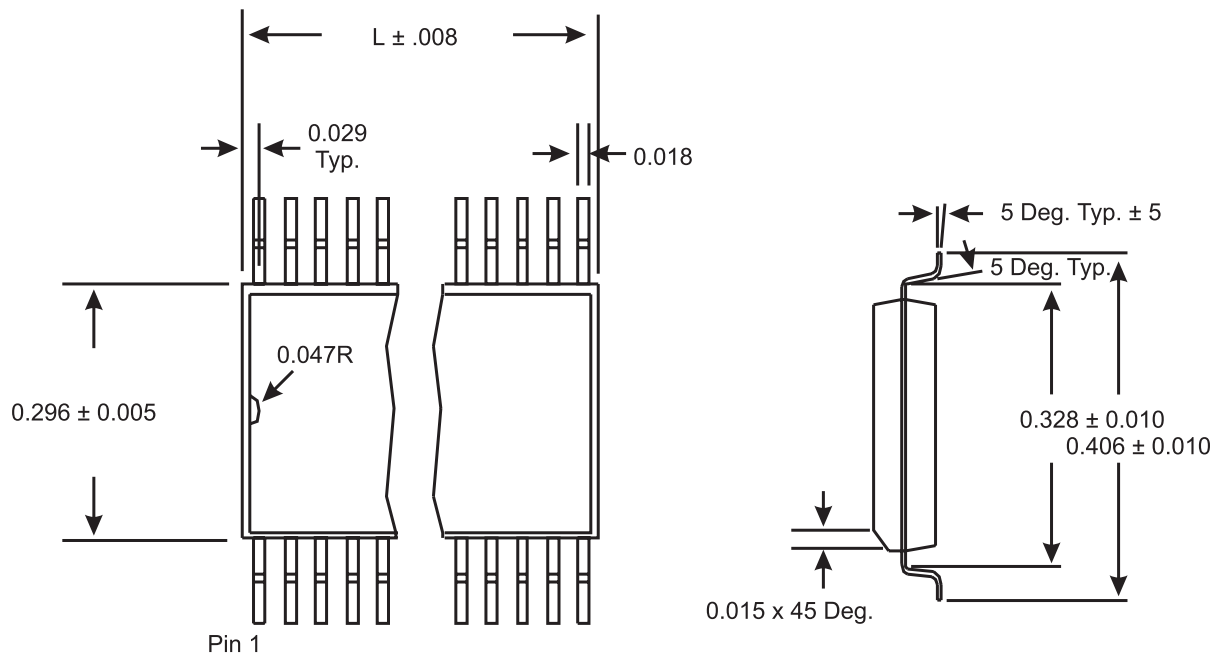
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## Electrical Characteristics at 5.5V

$V_{DD} = 4.5 - 5.5 \text{ V}$ ,  $T_A = 0 - 70^\circ \text{ C}$

| AC Characteristics                         |            |                                                                                    |      |        |      |       |
|--------------------------------------------|------------|------------------------------------------------------------------------------------|------|--------|------|-------|
| PARAMETER                                  | SYMBOL     | TEST CONDITIONS                                                                    | MIN  | TYP    | MAX  | UNITS |
| Rise Time <sup>1</sup>                     | $T_{r1}$   | 20pF load, 0.8 to 2.0V PCLK & BCLK                                                 | -    | 0.55   | 0.95 | ns    |
| Fall Time <sup>1</sup>                     | $T_{f1}$   | 20pF load, 2.0 to 0.8V PCLK & BCLK                                                 | -    | 0.52   | 0.90 | ns    |
| Rise Time <sup>1</sup>                     | $T_{r2}$   | 20pF load, 20% to 80% PCLK & BCLK                                                  | -    | 1.2    | 2.1  | ns    |
| Fall Time <sup>1</sup>                     | $T_{f2}$   | 20pF load, 80% to 20% PCLK & BCLK                                                  | -    | 1.1    | 2.0  | ns    |
| Duty Cycle <sup>1</sup>                    | $D_{t1}$   | 20pF load @ $V_{OUT}=1.4\text{V}$                                                  | 52   | 57     | 62   | %     |
| Duty Cycle <sup>1</sup>                    | $D_{t2}$   | 20pF load @ $V_{OUT}=50\%$                                                         | 45   | 50     | 55   | %     |
| Jitter, One Sigma <sup>1</sup>             | $T_{j1s1}$ | PCLK & BCLK Clocks; Load=20pF, RS=33W FOUT>25 MHz                                  | -    | 50     | 150  | ps    |
| Jitter, Absolute <sup>1</sup>              | $T_{jab1}$ | PCLK & BCLK Clocks; Load=20pF, RS=33W FOUT>25 MHz                                  | -250 | -      | 250  | ps    |
| Jitter, One Sigma <sup>1</sup>             | $T_{j1s2}$ | REF CLKs; Load=20pF RS=33W                                                         | -    | 1      | 3    | %     |
| Jitter, Absolute <sup>1</sup>              | $T_{jab2}$ | REF CLKs; Load=20pF RS=33W                                                         | -5   | 2      | 5    | %     |
| Input Frequency <sup>1</sup>               | $F_i$      |                                                                                    | 12.0 | 14.318 | 16.0 | MHz   |
| Logic Input Capacitance <sup>1</sup>       | $C_{IN}$   | Logic input pins                                                                   | -    | 5      | -    | pF    |
| Crystal OscillatorCapacitance <sup>1</sup> | $C_{INX}$  | X1, X2 pins                                                                        | -    | 18     | -    | pF    |
| Power-on Time <sup>1</sup>                 | $t_{on}$   | From $V_{DD}=1.6\text{V}$ to 1 st crossing of 66.5 MHz $V_{DD}$ supply ramp < 40ms | -    | 2.5    | 4.5  | ms    |
| Frequency Settling Time <sup>1</sup>       | $t_s$      | From 1st crossing of acquisition to < 1% settling                                  | -    | 2.0    | 4.0  | ms    |
| Clock Skew Window <sup>1</sup>             | $T_{sk1}$  | PCLK to PCLK; Load=20pF; @1.4V                                                     | -    | 150    | 250  | ps    |
| Clock Skew Window <sup>1</sup>             | $T_{sk2}$  | BCLK to BCLK; Load=20pF; @1.4V                                                     | -    | 300    | 500  | ps    |
| Clock Skew Window <sup>1</sup>             | $T_{sk3}$  | PCLK to BCLK; Load=20pF; @1.4V                                                     | -    | 400    | 600  | ps    |

**Note 1:** Parameter is guaranteed by design and characterization. Not 100% tested in production.



## SOIC Package

|            |       |
|------------|-------|
| LEAD COUNT | 28L   |
| DIMENSIONL | 0.704 |

## Ordering Information

### ICS9159M-13

Example:

**ICS XXXX M-PPP**

