

DESCRIPTION

The HYM594000A is a 4M x 9-bit Fast page mode CMOS DRAM module consisting of nine HY5114100A in 20/26 pin SOJ on a 30 pin glass-epoxy printed circuit board. 0.22 μ F decoupling capacitor is mounted for each DRAM. The HYM594000AM/ALM are Tin-Lead plated socket type Single In-line Memory Modules suitable for easy interchange and addition of 4M byte memory.

FEATURES

- Low power dissipation

Max. battery back-up 19.8mW (L-part)

Max. CMOS standby 9.9mW (L-part)

49.5mW

Max. TTL standby 99.0mW

Max. operating

Speed	Power
50	6.19W
60	5.45W
70	4.70W

- Single power supply of 5V $\pm$ 10%

- TTL compatible inputs and outputs

- Fast access time

Speed	tRAC	tCAC	tPC
50	50ns	15ns	35ns
60	60ns	15ns	40ns
70	70ns	20ns	45ns

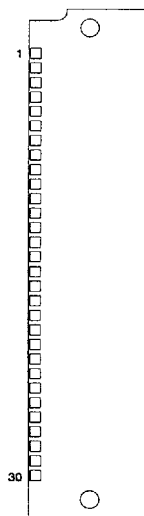
- Fast page mode operation

- CAS-before-RAS, RAS-only, Hidden refresh

- 1024 refresh cycles / 128ms (L-part)

1024 refresh cycles / 16ms

PIN CONNECTION



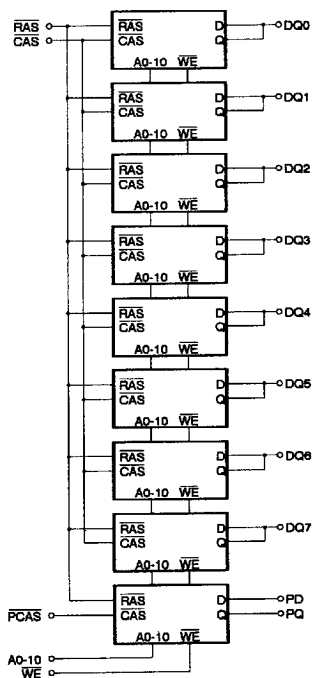
PIN DESCRIPTION

RAS	Row Address Strobe
CAS	Column Address Strobe
PCAS	CAS for Parity
WE	Write Enable
A0-A10	Address Input
DQ0-DQ7	Data Input/Output
PD	Data In for Parity
PQ	Data Out for Parity
VCC	Power (+5V)
VSS	Ground

PIN NAME

#	NAME
1	VCC
2	CAS
3	DQ0
4	A0
5	A1
6	DQ1
7	A2
8	A3
9	VSS
10	DQ2
11	A4
12	A5
13	DQ3
14	A6
15	A7
16	DQ4
17	A8
18	A9
19	A10
20	DQ5
21	WE
22	VSS
23	DQ6
24	NC
25	DQ7
26	PQ
27	RAS
28	PCAS
29	PD
30	VCC

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to VSS	-1.0 to 7.0	V
VCC	Voltage on VCC Relative to VSS	-1.0 to 7.0	V
IOS	Short Circuit Output Current	50	mA
PD	Power Dissipation	8.1	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	VCC + 1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to VSS.

DC CHARACTERISTICS

(TA=0°C to 70°C, VCC=5V±10%, VSS=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pin)	VSS≤VIN≤VCC+1.0, All other pins not under test = VSS		-90	90	μA	
ILO	Output Leakage Current (High Impedance State)	VSS≤VOUT≤VCC, RAS & CAS at VIH		-10	10	μA	
ICC1	VCC Supply Current, Operating	trc = trc (min.)	50 60 70	- - -	1125 990 855	mA	1,2,3
ICC2	VCC Supply Current, TTL Standby	RAS & CAS at VIH, other inputs≥VSS		-	18	mA	
ICC3	VCC Supply Current, RAS-only refresh	trc = trc (min.)	50 60 70	- - -	1125 990 855	mA	1,3
ICC4	VCC Supply Current, Fast Page mode	tpc = tpc (min.)	50 60 70	- - -	675 585 495	mA	1,2,3
ICC5	VCC Supply Current, CMOS Standby	RAS & CAS ≥ VCC-0.2V	L-part	- -	9 1.8	mA	5
ICC6	VCC Supply Current, CAS-before-RAS refresh	trc = trc (min.)	50 60 70	- - -	1125 990 855	mA	1,3
ICC7	VCC Supply Current, Battery Back Up (L-part only)	trc = 125μs, CAS = CBR cycling or 0.2V WE = VCC-0.2V A0-A10 = VCC-0.2V or 0.2V DQ0-DQ7 = VCC-0.2V, 0.2V, or open	tras ≤ 300ns tras ≤ 1μs	- - -	2.7 3.6	mA	1,4,5
VOL	Output Low Voltage	IOL = 4.2mA		-	0.4	V	
VOH	Output High Voltage	IOH = -5mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4, ICC6 and ICC7 depend on cycle rate.
2. ICC1 and ICC4 depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while RAS = VIL and CAS = VIH.
4. Only tras(max.) = 1μs is applied to refresh of battery backup but tras(max.) = 10μs is applied to normal functional operation.
5. ICC5(max.) = 1.8mA and ICC7 are applied to L-part only (HYM594000ALM).

AC CHARACTERISTICS

(TA = 0°C to 70°C, VCC = 5V ± 10%, VSS = 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM594000AM/ALM						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	90	-	110	-	130	-	ns	
2	tRPC	RAS to CAS Precharge Time	0	-	0	-	0	-	ns	
3	tPC	Fast Page Mode Cycle Time	35	-	40	-	45	-	ns	
4	tRHCP	RAS Hold Time from CAS Precharge	30	-	35	-	40	-	ns	
5	tRAC	Access Time from RAS	-	50	-	60	-	70	ns	4,9,10
6	tCAC	Access Time from CAS	-	15	-	15	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	25	-	30	-	35	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	30	-	35	-	40	ns	4
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	15	0	15	0	20	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3
12	tRP	RAS Precharge Time	30	-	40	-	50	-	ns	
13	tRAS	RAS Pulse Width	50	10K	60	10K	70	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	50	200K	60	200K	70	200K	ns	
15	tRSH	RAS Hold Time	15	-	15	-	20	-	ns	
16	tCSH	CAS Hold Time	50	-	60	-	70	-	ns	
17	tCAS	CAS Pulse Width	15	10K	15	10K	20	10K	ns	
18	tRCD	RAS to CAS Delay	15	35	20	45	20	50	ns	9
19	tRAD	RAS to Column Address Delay Time	10	25	15	30	15	35	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	
21	tCP	CAS Precharge Time	10	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	5	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	15	-	15	-	15	-	ns	
26	tAR	Column Address Hold Time from RAS	45	-	50	-	55	-	ns	
27	tRAL	Column Address to RAS Lead Time	25	-	30	-	35	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	10	-	15	-	15	-	ns	
32	tWCR	Write Command Hold Time from RAS	40	-	50	-	55	-	ns	
33	tWP	Write Command Pulse Width	10	-	15	-	15	-	ns	
34	tRWL	Write Command to RAS Lead Time	15	-	15	-	20	-	ns	
35	tCWL	Write Command to CAS Lead Time	15	-	15	-	20	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	10	-	15	-	15	-	ns	7
38	tDHR	Data-In Hold Time Referenced to RAS	40	-	50	-	55	-	ns	
39	tREF	Refresh Period (1024 cycles)	-	16	-	16	-	16	ms	
		L-part	-	128	-	128	-	128		11
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

AC CHARACTERISTICS

(continued)

(continued)

#	SYMBOL	PARAMETER	HYM594000AM/ALM						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCSR	CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
42	tCHR	CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
43	tCPT	CAS Precharge Time (CBR Counter Test)	25	-	30	-	35	-	ns	
44	tWRP	WE to RAS Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
45	tWRH	WE to RAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	

NOTE :

1. An initial pause of 200 μ s is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ -only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$ are reference levels for measuring timing of input signals. Transition time is measured between V_{IH} and V_{IL} and assumed to be 5ns for all inputs.
3. Refer to the HY514100A data sheet for detailed information.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. $t_{OFF}(\text{max.})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RAH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles.
8. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
9. Operation within the $t_{RCD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
10. Operation within the $t_{RAD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .
11. $t_{REF}(\text{max.}) = 128\text{ms}$ is applied to L-part only (HYM594000ALM).

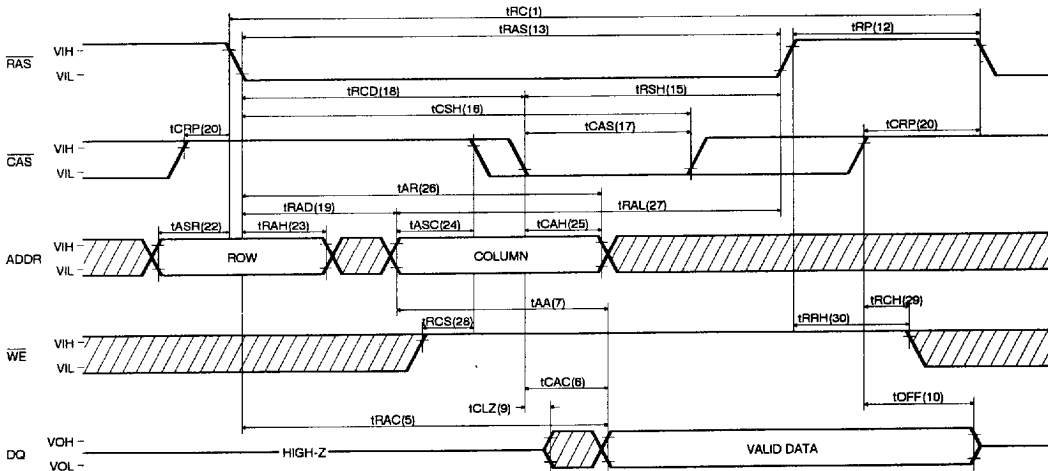
CAPACITANCE

($T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, $f = 1\text{MHz}$, unless otherwise noted.)

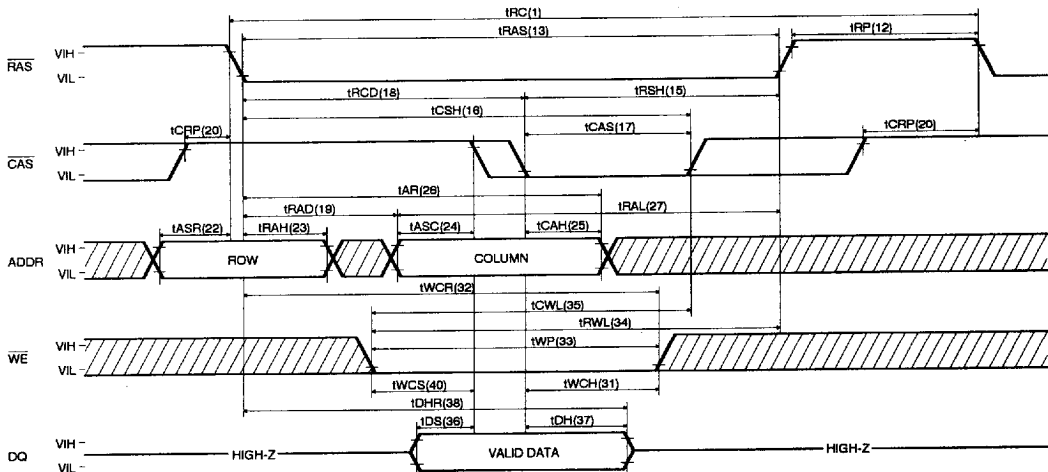
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A10, WE, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$)	-	60	pF
C_{IN2}	Input Capacitance (PD, $\overline{\text{PCAS}}$)	-	10	pF
C_{DQ}	I/O Capacitance (DQ0-DQ7)	-	15	pF
C_{PQ}	Output Capacitance (PQ)	-	10	pF

TIMING DIAGRAM

READ CYCLE

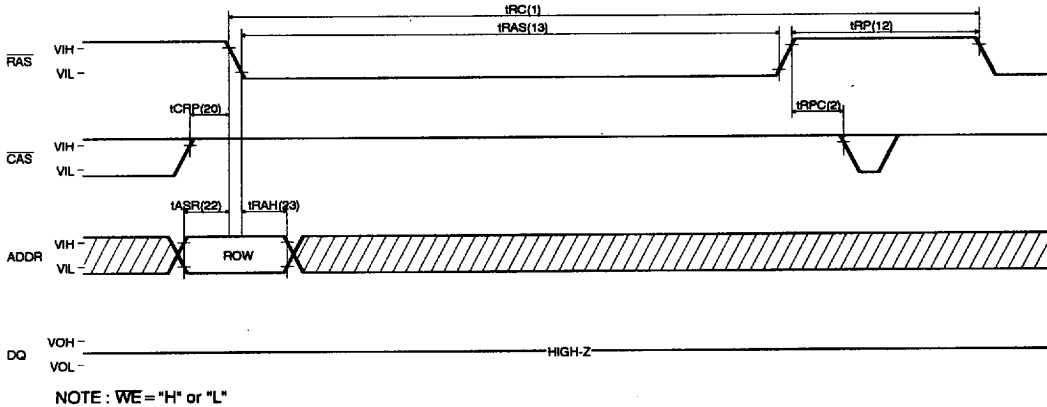


EARLY WRITE CYCLE

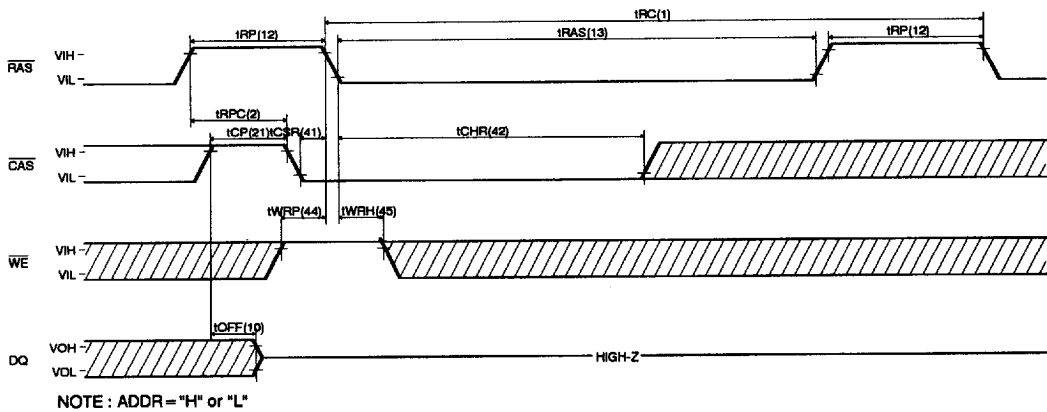


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RAS-ONLY REFRESH CYCLE



CAS-BEFORE-RAS REFRESH CYCLE



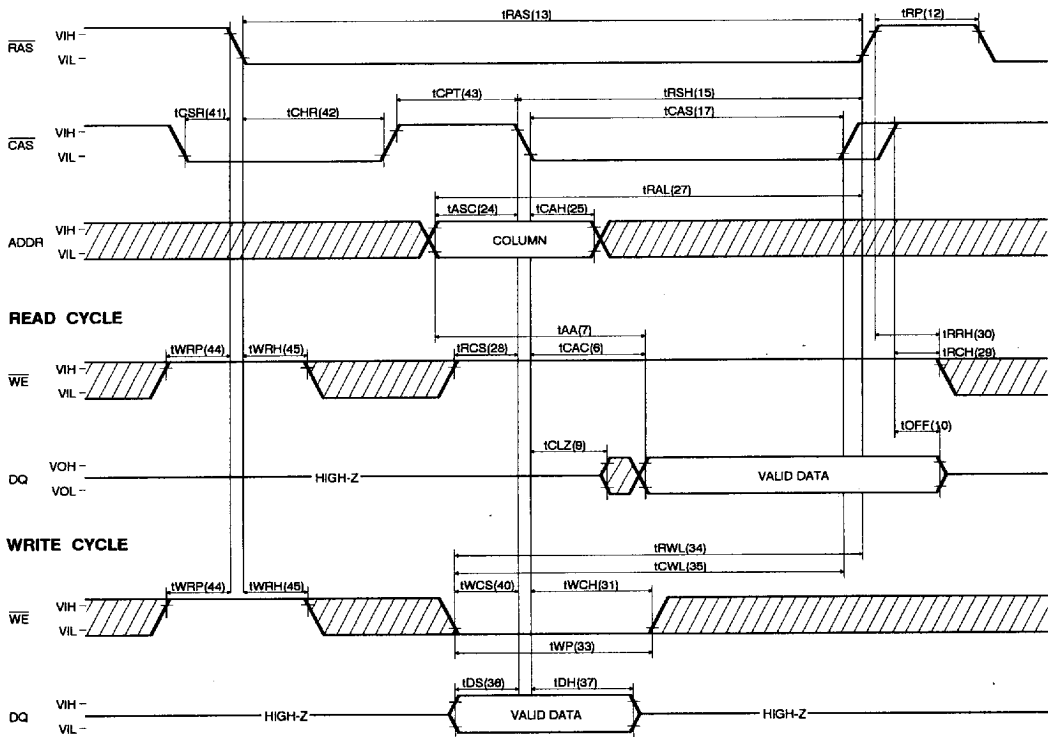
The timing diagram illustrates the relationship between several signals and their timing parameters:

- RAS:** Shows two pulses. Timing parameters include $t_{RC}(1)$, $t_{RAS}(13)$, $t_{RP}(12)$, $t_{CRP}(20)$, $t_{RCD}(18)$, $t_{RSH}(15)$, $t_{CHR}(42)$, and $t_{CRP}(20)$.
- CAS:** Shows two pulses. Timing parameters include $t_{AR}(28)$, $t_{RAD}(19)$, $t_{RAH}(23)$, $t_{ASC}(24)$, $t_{RAL}(27)$, $t_{CAH}(25)$, and $t_{ASR}(22)$.
- ADDR:** Shows two pulses labeled ROW and COLUMN. Timing parameters include $t_{RCS}(28)$, $t_{RRH}(30)$, $t_{WRF}(44)$, and $t_{WRF}(45)$.
- WE:** Shows two pulses. Timing parameters include $t_{AA}(7)$, $t_{CAC}(8)$, $t_{RAC}(5)$, $t_{ICLZ}(9)$, and $t_{OFF}(10)$.
- DQ:** Shows a signal that transitions from HIGH-Z to VALID DATA and back to HIGH-Z. Timing parameters include $t_{CLZ}(9)$ and $t_{OFF}(10)$.

The timing diagram illustrates the relationship between the RAS, CAS, ADDR, WE, and DQ signals. Key timing parameters are defined as follows:

- RAS:** $t_{RAS}(13)$, $t_{RC}(11)$, $t_{RP}(12)$
- CAS:** $t_{CRP}(20)$, $t_{RCD}(18)$, $t_{RSH}(15)$, $t_{CHR}(42)$
- ADDR:** $t_{ASR}(22)$, $t_{AR}(26)$, $t_{RAD}(19)$, $t_{RAH}(23)$, $t_{SC}(24)$, $t_{CAH}(25)$
- WE:** $t_{WCS}(40)$, $t_{RWL}(34)$, $t_{WCH}(31)$, $t_{WP}(33)$, $t_{WRP}(44)$, $t_{WRH}(45)$
- DQ:** $t_{WCR}(32)$, $t_{DHR}(38)$, $t_{DS}(36)$, $t_{DH}(37)$

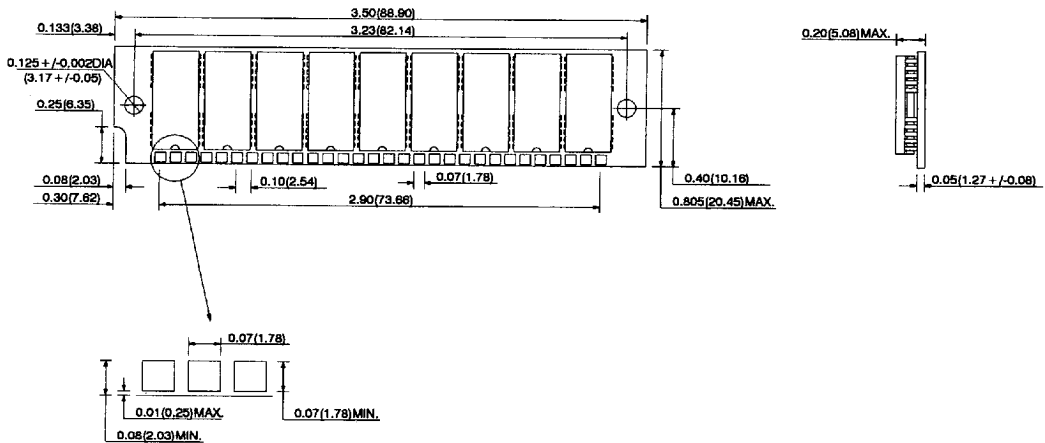
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



PACKAGE INFORMATION

30 pin Single In-line Memory Module (M ; Tin-Lead plated)

UNIT : INCH(mm)
TOLERANCE : +/-0.005(0.13)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM594000AM	50/60/70		SIMM	Tin-Lead
HYM594000ALM	50/60/70	L-part	SIMM	Tin-Lead