STANDARD MICROSYSTEMS CORPORATION

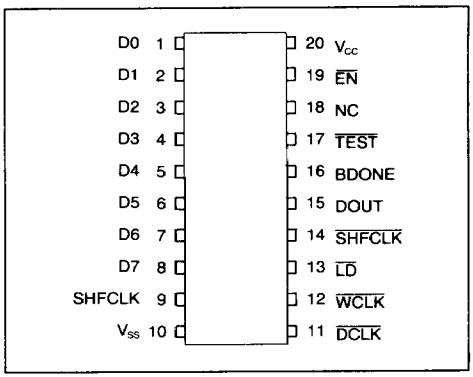
HDC 1100-05
PRELIMINARY

Hard Disk Parallel to Serial Converter

FEATURES

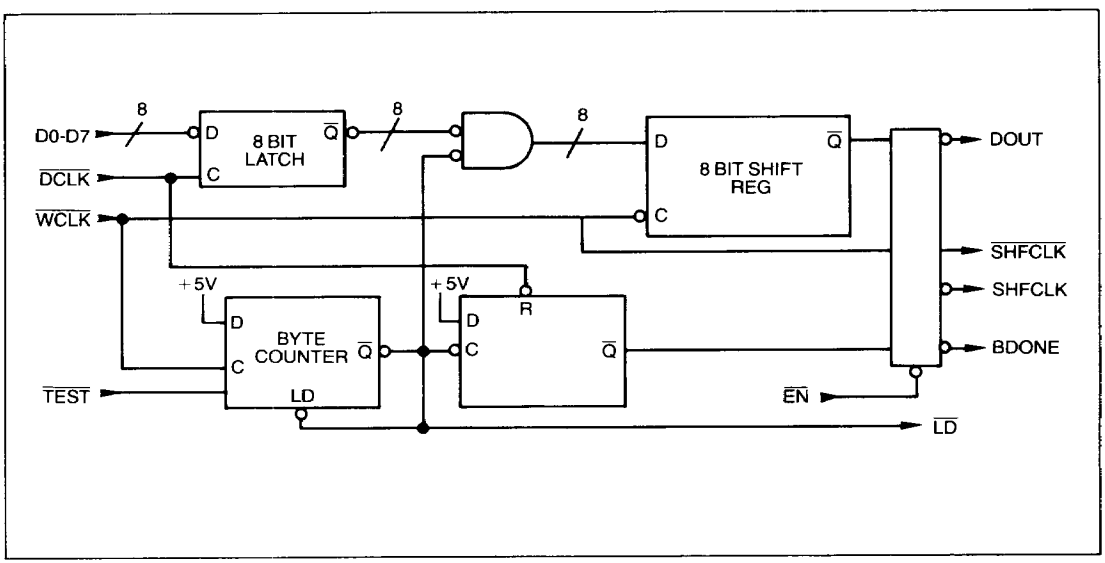
- ☐ Single +5 Volt Power Supply
- ☐ Double Buffered
- ☐ Byte Strobe Outputs
- ☐ 5 Mbit Data Rate
- ☐ Parallel In/Serial Out
- ☐ 20 Pin DIP
- ☐ n-Channel COPLAMOS® Silicon Gate Technology

PIN CONFIGURATION



GENERAL DESCRIPTION

The HDC 1100-05 converts bytes of parallel data to a serial data stream for writing to disk memories or other serial devices. Parallel data is entered via the D0-D7 lines. A synchronous byte counter is used to signify that 8 bits of data have been shifted out and that the 8 bit latch is ready to be reloaded. The double buffering of the data permits another byte to be loaded while the previous byte is in the process of being shifted.



SECTION VI

DESCRIPTION OF PIN FUNCTIONS

PIN NUMBER	SYMBOL	NAME	FUNCTION
1-8	D0-D7	DATA 0-DATA 7	8 bit parallel data inputs (bit 7 = MSB).
9	SHFCLK	SHIFT CLOCK	Inverted copy of $\overline{WCLK}$ (pin 12) which is active when ENABLE (pin 19) is at a logic 0.
10	V_{SS}	GROUND	GROUND.
11	$\overline{DCLK}$	$\overline{DATA\ CLOCK}$	Active low input signal resets the BDONE (pin 16) latch. The low-to-high (trailing edge) clocks the input data into the internal 8 bit latch.
12	$\overline{WCLK}$	$\overline{WRITE\ CLOCK}$	The high-to-low (↓) edge of this clock signal is used to shift the data out serially. The low-to-high (↑) edge is used to update the internal byte counter (modulo 8).
13	$\overline{LD}$	$\overline{LOAD}$	This active low signal indicates that the Byte Counter is being preset to 1. Normally left open by the user.
14	$\overline{SHFCLK}$	$\overline{SHIFT\ CLOCK}$	Delayed copy of $\overline{WCLK}$ (pin 12) which is active when EN (pin 19) is at a logic 0.
15	DOUT	DATA OUT	Serial data output enabled by EN (pin 19).
16	BDONE	BYTE DONE	This output signal is forced to a logic 1 whenever 8 bits of data have been shifted out. BDONE remains in this state unless reset by the loading of another byte of data.
17	$\overline{TEST}$	$\overline{TEST\ INPUT}$	This pin must be left open by the user.
18	NC	No Connection	NO CONNECTION
19	$\overline{EN}$	$\overline{ENABLE}$	This active low signal enables DOUT, $\overline{SHFCLK}$, SHFCLK, and BDONE outputs. When high, these output signals are in a high impedance state.
20	V_{CC}	V_{CC}	+ 5 power supply input.

OPERATION

Prior to loading the HDC 1100-05, it is recommended that 00H (or FF) be loaded into the input buffers to ensure that DOUT is at a fixed level. $\overline{EN}$ (pin 19) is set to a logic 0 to enable the device outputs.

Data is entered on the D0-D7 input lines and is strobed into the data latches on the rising edge of $\overline{DCLK}$ (pin 11). $\overline{DCLK}$ also resets BCONE (pin 16). The first BDONE that comes up simply means that the HDC 1100-05 is ready to accept another byte of data and that the previous byte entered is in the process of being shifted out. If the BDONE is serviced prior to every 8th $\overline{WRITE\ CLOCK}$ pulse the output data will represent a contiguous block of the bytes entered. Due to the asynchronous nature of the HDC 1100-05, the input data will be available in serial form at the output anywhere from 8 to 16 write clock cycles later.

Data is shifted out on the high-to-low transition of the $\overline{WCLK}$ (pin 12). The low-to-high transition of $\overline{WCLK}$ increments a byte counter which in turn sets the BDONE signal high after 8 bits of data have been shifted out. The low-to-high transition of BDONE also causes the loading of the data buffer into the shift register. The data buffer is now ready to be reloaded with the next byte.

The loading of the next byte automatically clears the BDONE signal. The entire process as outlined above is repeated. BDONE always needs to be serviced within 8 WCLK cycles unless the next byte to be transmitted is the same as the previous byte.

Four signals, BDONE, DOUT, SHFCLK, and $\overline{SHFCLK}$, can be placed in a high impedance state of setting $\overline{EN}$ (pin 19) to a logic 1. Likewise, $\overline{EN}$ must be at a logic 0 in order for these signals to drive any external device.

The $\overline{TEST}$ pin is internally OR'd with the counter output to produce the $\overline{LD}$ (pin 13) signal. This is used to inhibit the bit counter by external means for test purposes. It is recommended that $\overline{TEST}$ be left open by the user. An internal pullup register is tied to this pin to satisfy the appropriate logic level required for proper device operation.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to +50°C
Storage Temperature Range	−55° to +150°C
Lead Temperature (soldering, 10 sec.)	+300°C
Positive Voltage on any I/O Pin, with respect to ground	+7.0V
Negative Voltage on any I/O Pin, with respect to ground	−0.2V
Power Dissipation	1.0 watt

*Stresses above those listed may cause permanent damage to the device. This is a stress rati... ...tion of the device at these or at any other condition above those indicated in the operational sections of this sp...

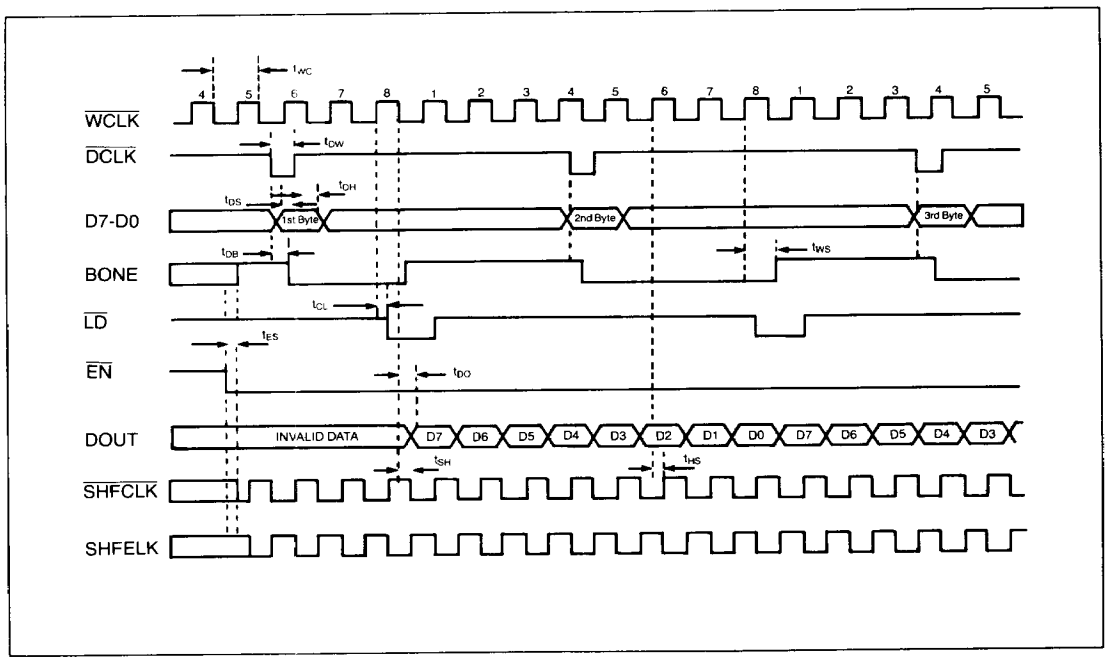
DC ELECTRICAL CHARACTERISTICS: T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
V_{IL}	Input Low Voltage	−0.2		0.8	V	
V_{OH}	Input High Voltage	2.4			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{DH}	Output High Voltage	2.4			V	I_{OH} = −200μA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			100	mA	All Outputs Open

AC ELECTRICAL CHARACTERISTICS: T_A = 0°C to 50°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITION
t_{WC}	WCLK frequency			5.25	MHZ	
t_{DW}	DCLK pulse width	50			nsec	
t_{DS}	Data set-up w.r.t. ↑ DCLK	30			nsec	
t_{DH}	Data hold time w.r.t. ↑ DCLK	30			nsec	
t_{DB}	↓ DCLK to ↓ BDONE			130	nsec	EN = 0
t_{DO}	↓ WCLK to DOUT			130	nsec	EN = 0
t_{SH}	↓ WCLK to ↓ SHFCLK			75	nsec	EN = 0
t_{HS}	↓ WCLK to ↑ SHFCLK			70	nsec	EN = 0
t_{WB}	↑ WCLK to ↑BDONE	75		180	nsec	
t_{ES}	↓ $\overline{EN}$ to BDONE, DOUT SHFCLK ACTIVE			25	nsec	
t_{CL}	↑ WCLK to ↓ $\overline{LD}$			50	nsec	

NOTES: 1. Typical Values are for T_A = 25°C and V_{CC} = +5.0V



SECTION VI