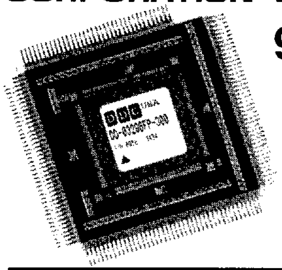
ILC DATA DEVICE CORPORATION®

DD-03296

96-CHANNEL DISCRETE-TO-DIGITAL INTERFACE "R0D3"



DESCRIPTION

The DD-03296 device is a 96-channel discrete-to-digital interface with universal HIRF-isolated inputs to handle 28 V/Open, Open/GND and 28 V/Gnd signals.

The output is an addressable 8-bit or 16-bit tri-state port, selectable for channel data, status, bounce, built-in self-test (BIST) and major fault, compatible with TTL logic.

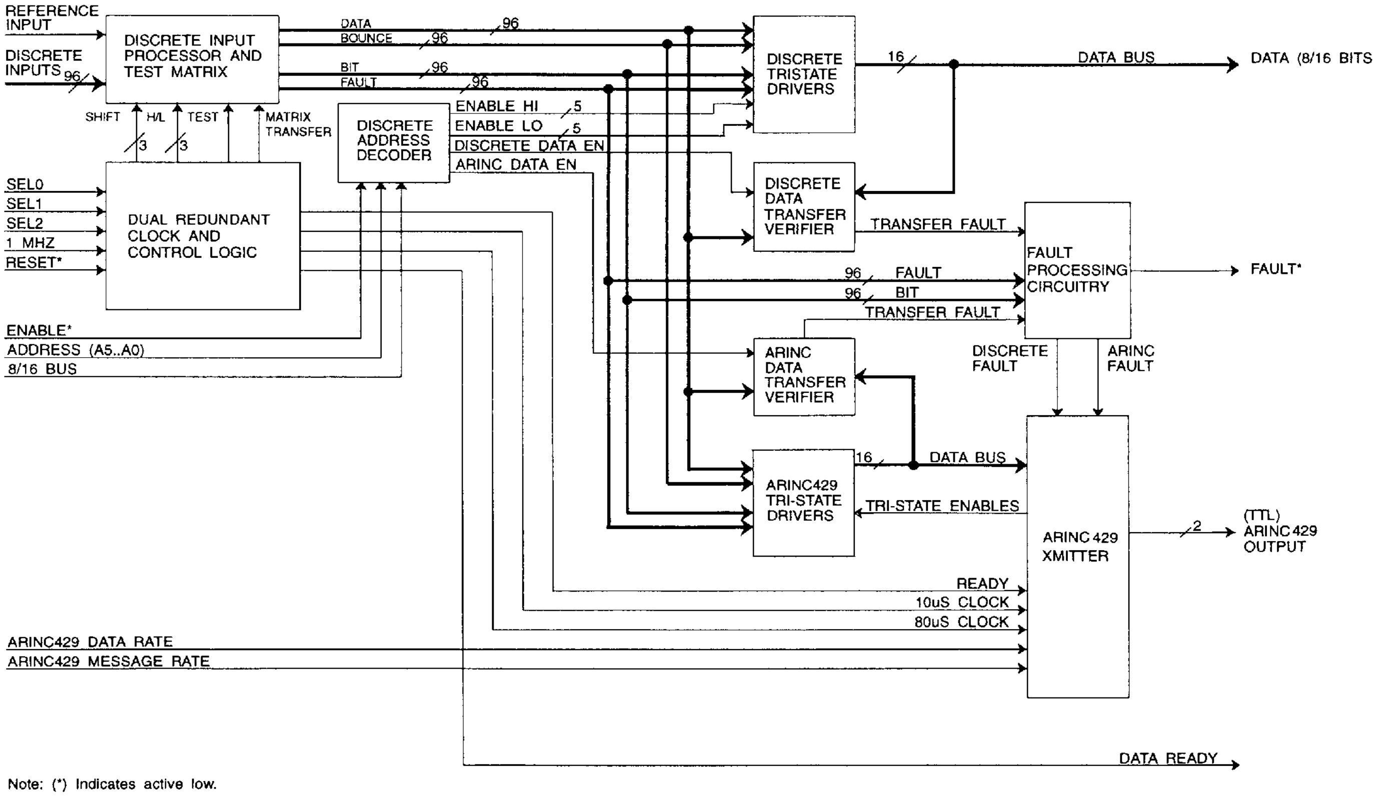
APPLICATIONS

The design specifically addresses built-in self-test autonomy, fault isolation and tolerance.

With high reliability and low cost, these features enable the devices to serve a variety of interface requirements in aerospace applications, including flight critical, essential, and nonessential functions. The optional ARINC 429 output port is particularly well-suited to data-concentrator requirements.

FEATURES

- ***HIRF Layer***
- ***Universal Inputs***
  28 V/Gnd
  Open/Gnd
  28 V/Open
- ***Built-In Self-Test***
- ***Soft Failure Reporting***
  Higher MTBUR
- ***Optional ARINC 429 Output Port***



Note: (*) Indicates active low.

FIGURE 1. DD-03296 BLOCK DIAGRAM

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TABLE 1. DD-03296 SPECIFICATION				
PARAMETER	**UNITS**	**MIN**	**TYP**	**MAX**
ABSOLUTE MAXIMUM RATINGS				
Supply Voltages (V_{CC}, V_{DD})	V	-0.3	5.0	7.0
Reference Inputs	V	-80		+80
Discrete Inputs	V	-80		+80
Digital Inputs	V	-0.3		V_{DD}+0.3
OPERATING CONDITIONS				
Supply Voltage (V_{DD})	V	4.5		5.5
DIGITAL INPUTS/OUTPUTS				
Logic Compatibility	TTL/ CMOS			
Digital Inputs				
■ V_{IH}	V	2.0		
■ V_{IL}	V			0.8
■ I_{IL} (V_{IN} = 0)	µA	-40		-400
Clock Input (See Note 1)	MHz	0.99	1.00	1.01
Digital Outputs				
■ V_{OH} (I_{OH} = -1ma)	V	V_{DD}-0.5		
■ V_{OH} (I_{OH} = -4ma)	V	2.4		
■ V_{OL} (I_{OH} = 4ma)	V			0.4
Analog Inputs	See FIGURE 3			
POWER SUPPLY REQUIREMENTS				
(Total V_{DD}, Analog & Digital) I_{DD} (V_{DD} = +5V [Digital Outputs Unloaded])	ma		25	45
POWER DISSIPATION				
P_D	mw		125.0	250.0
THERMAL				
Operating Temperature				
■ Type 1	°C	-55		125
■ Type 2	°C	-40		85
■ Type 3	°C	0		70
Storage Temp	°C	-65		150
Lead Temperature				
(localized, 1 sec. duration)	°C			280
(body, 2 sec. duration)	°C			210
Junction Temperature				
θ_{jc}	°C/W		5.0	
θ_{ca}	°C/W		20.0	
MTBF per Mil-Hbk-217 for Airborne Inhabited Cargo at 64°C		1,400,000 hrs. plastic 1,540,000 hrs. ceramic		
PHYSICAL CHARACTERISTICS				
Size	in. (cm)	2.3 x 2.3 (5.84 x 5.84)		
Weight	oz. (g)			

Note 1: For ARINC 429 option the bit rate is derived from the clock. Refer to ARINC 429 Bit Rate to avoid interference. ARINC 429-14 (January 4, 1993), paragraph 2.4 "Timing Related Elements" contains a "COMMENTARY" section following subparagraph 2.1.4.2 ("Low Speed Operation") that cautions against using "precisely" 100 kilobits per second.

WHAT IS A DISCRETE?

Advisory Circular (FAA), Airworthiness Approval of Traffic Alert and Collision Avoidance Systems (TCAS II) and Mode S Transponders, AC20-131, defines a discrete as "a separate, complete and distinct signal." In many instances these signals are binary, on or off, 28V-based signals; they are typically Open/Ground, 28V/Open, or 28V/Ground with very low bandwidth (DC to 200Hz).

While on the surface the translation of these signals to TTL-levels compatible with digital avionics may seem simple, however, RTCA DO-160C power, lightning and high-intensity-radiated-fields (HIRF) are complicating factors. Add to that the desire to have a standardized, addressable, reliable interface and the challenge is apparent.

Today's systems address the interface with tailored circuits for each interface comprised of R-C input filters, divider networks, diode isolation and comparators. Multichannel interface to a processor requires additional logic and latches. The resulting circuit generally lacks any built-in test capability and consumes considerable pc-board real estate (up to 1 square inch per channel).

FUNCTIONAL INTEGRATION

Using the aggregated signal definition and functional requirements of industry, ILC Data Device Corporation has developed a 96-channel discrete interface with universal HIRF-isolated inputs to handle 28V/Open, Open/Gnd and 28V/Gnd signals. Each channel is routed through a HIRF filter and comparator. Its output is a selectable 8-bit or 16-bit tri-state port, addressable for channel data, status, bounce, built-in self-test and major fault information.

Its design specifically addresses built-in self-test autonomy, fault isolation and tolerance; moreover, its functional integration results in significant added reliability. A comparative look at MTBF calculated in accordance with MIL-HBK-217 for airborne inhabited cargo environments at 64°C indicates an order of magnitude improvement (1,540,000 hours vs. 173,000 hours) for a ceramic packaged integrated approach vs. a similarly packaged discrete-component implementation. In addition, the real estate is reduced from as much as 64 square inches to 5 square inches.

Additional Key Features include:

BOUNCE: Relays and switches, as mechanical devices, have a characteristic "bounce" to their signal transition. It is desirable to mask this bounce by delaying the output digital transition accordingly. The sampling rate of the DD-03296 can be varied to allow for debounce of relay/switch inputs. In addition, the triple sampling of a given comparator enables a consistent reading of otherwise asynchronous signals. Bounce is an addressable status that allows the user to detect bouncing or intermittent relays/switches.

GROUND DIFFERENTIALS: When the reference inputs are connected to the 28V supply, the thresholds are designed to tolerate ±3.5V ground differences.

REGISTERS: 8-bit or 16-bit selectable data or status is available via tri-state buffers for interface to any system processor.

OPTIONAL ARINC 429 PORT: A serial ARINC 429 output is available for data-concentrator applications. This enables the transfer of data to other systems with a minimum of wiring and processor loading.

HIRF: The device incorporates passive circuitry to isolate the intelligence from both lightning effects and radiated fields as defined in DO-160C. This protection is applicable to the discrete inputs, reference inputs, and their relationship to each other and to ground.

TEST PATTERNS: Internal Test Patterns can be selected to produce alternating "1"s and "0"s data to verify that all address and data bits are operational. While these outputs are always available, *regardless* of READY state, they must be addressed by the user (A5..A0) in accordance with TABLES 3 and 4.

DISSIMILAR PATHS: Errors are reported through the registers and through the optional ARINC 429 port as cross checks.

INTELLIGENCE: The device built-in-test, status reporting scheme, and isolation significantly reduce application software requirements. FIGURE 1 illustrates the model DD-03296 functional block diagram.

ASYNCHRONOUS SAMPLING: The device takes three samples on each encode because input discrete transitions are asynchronous and reports the "majority" state.

MICROPROCESSOR INTERFACE

READ CYCLE TIMING

The DD-03296 is configured to interface between an 8- or 16-bit microprocessor. FIGURE 2 illustrates this interface.

The read cycle(s) should be preceeded by polling the device's READY bit located within the Status Register. The Status Register can be read at any time regardless of the state of the READY signal (pin) from the device.

If the READY bit is at logic 1 (this can be easily tested by a branch if negative statement) the address of the desired register, along with the negative true $\overline{\text{ENABLE}}$ signal, should be presented to the device. The addressed data will be available within 100 ns.

After the data is read the $\overline{\text{ENABLE}}$ line should be returned to the logic 1 level before the address is changed.

All of the data within the device is guaranteed to remain stable for at least 20 µs after the high-to-low transition of the READY signal (see FIGURE 3).

ANALOG INPUTS

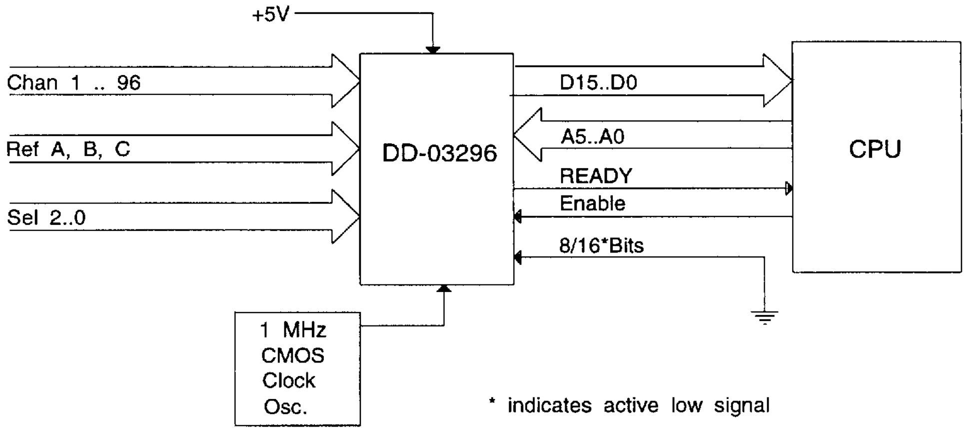
ANALOG INPUT CHANNELS: (PINS 161, 162, 1-6, 8-15 19-26, 29-36, 45-52, 55-62, 66-73, 76-83, 85-92, 95-102, 105-112, 115-122) 600KΩ input resistance, 500µs time constant, responsive to Open/Gnd (when configured with appropriate external pull-up), 28V/Open and 28V/Gnd input with HIRF/lightning immunity. Refer to FIGURE 4 for a detail of the input structure.

REFERENCE: Configured for 28V tracking discretes. User adjustable for other reference levels by connecting external resistors between corresponding TRIM and REF inputs.

FIGURE 4 also shows the reference structure. Each set of Ref/Trim inputs are configured by the user for a bank of 32-channel inputs. (See FIGURE 4 and TABLE 7.)

REF A, B, C: (Pins 37, 65, and 75) Input to the divider supplying the reference voltage to the "A," "B," and "C" group of 96 input channels.

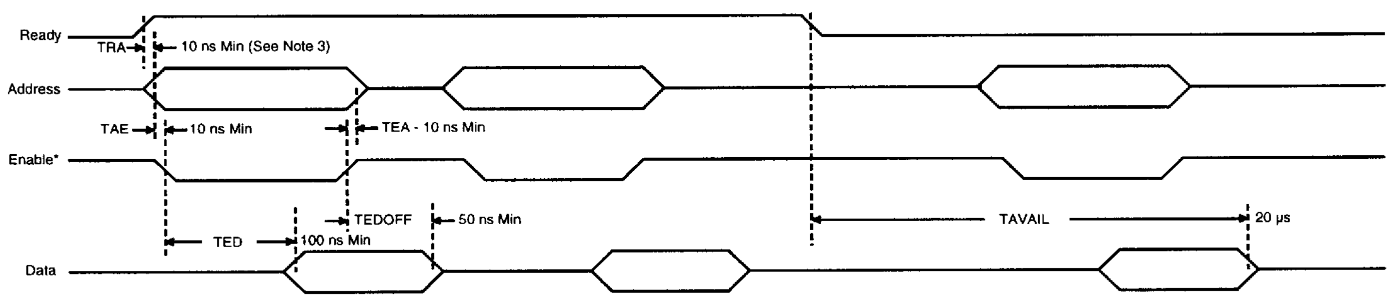
TRIM A, B, C: (Pins 38, 64, and 74) Junction of the first resistor and the rest of the reference "A," "B," and "C" divider.



NOTE: 1) If 8/16* Bits pin is tied to +5 Volts,then the DD-03296 is configured for 8-Bit Mode. The following must also be modified:
- D0 tied to D8
- D1 tied to D9
- D2 tied to D10
- D3 tied to D11
- D4 tied to D12
- D5 tied to D13
- D6 tied to D14
- D7 tied to D15

2) If the ARINC 429 option is not used, then pin 153 (429STRBI) MUST be grounded for the "bounce" circuit to operate properly.

FIGURE 2. R0D3 TO CPU INTERFACE



Note:
1) TRA = Time Ready Address
2) TAE = Time Address Enable
3) TEA = Time Enable to Address
4) TED = Time Enable Data
5) TEDOFF = Time Enable Off - Data Off
6) TAVAIL = Time Ready* - Data Available
7) (*) Indicates active low.
8) The ready "on-time" = (sample rate - 440 µs)
Sample rate is programmable via SEL0 - SEL2 (See TABLE 2)

FIGURE 3. READ CYCLE TIMING

DIGITAL INPUTS

DEBOUNCE (SEL2..SEL0): (Pins 158-160) The input discrete sampling rate (Debounce Time) is user programmable via the three select lines (SEL2..SEL0) in accordance with TABLE 2. The intent of this function is to mask the bounce of the input discrete appropriate to its characteristic performance. See "bounce" on page 3.

TABLE 2. DISCRETE SAMPLING RATE

SELECT (SEL2..SEL0)	SAMPLE RATE
000	5 ms
001	10 ms
010	20 ms
011	50 ms
100	100 ms
101	200 ms
110	500 ms
111	1000 ms

$\overline{\text{ENABLE}}$: (Pin 147) The $\overline{\text{ENABLE}}$ line controls the tri-state drivers of the 8- or 16-bit data bus outputs. The tri-state data bus drivers are enabled when this signal is at logic 0 and are tri-stated when this signal is at logic 1. $\overline{\text{ENABLE}}$ is a read signal and should only be low during reads.

8/$\overline{16}$ BITS: (Pin 104) "0" Selects 16-Bit data bus output, "1" selects 8-Bit data bus output.

ADDRESS LINES (A5..A0): (Pins 139, 140, and 143-146) The six address lines (A5..A0 where A0 is the LSB) provide for the selection of the desired 8- or 16-bit data bus information in accordance with TABLES 3 and 4 (Word/Byte Modes).

CLOCK (1 MHz CLK): (Pin 28) The user must supply a 1 MHz clock whose stability is of no importance *except* to the serial bit rate of the optional ARINC 429 port (see Note 1 of TABLE 1). The clock is brought into the internal ASIC at two widely separated points designated as CLOCK_A (primary) and CLOCK_B (secondary) path.

The primary clock path will be selected and drive the device unless a primary clock path fault is detected, in which case the operation of the device will be switched over to the secondary clock path.

Both clock paths are continually monitored for status and this information is available as separate bits in the Status Register.

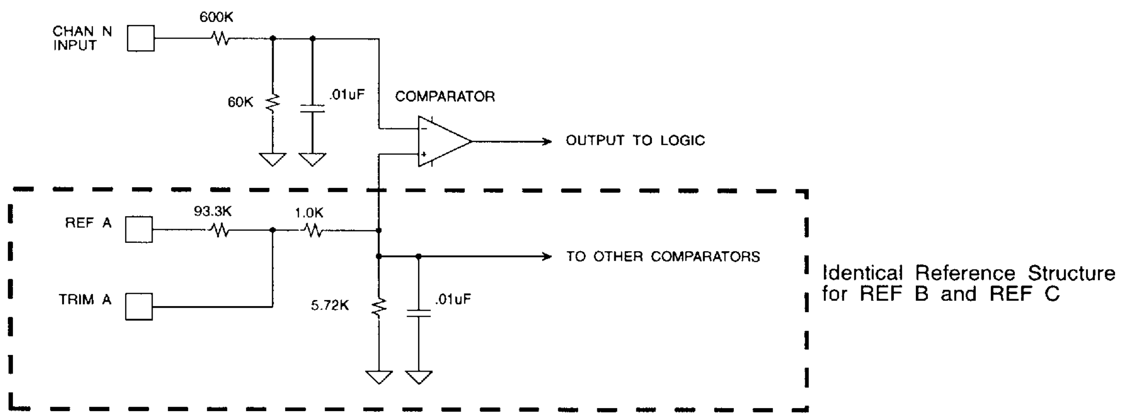


FIGURE 4. DD-03296 INPUT STRUCTURE

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TABLE 3. WORD MODE (16-BIT BUS)	
ADDRESS (A5..A0)	DATA (D7..D0)
00 000X	BOUNCE CH_16..CH_01
00 001X	BOUNCE CH_32..CH_17
00 010X	BOUNCE CH_48..CH_33
00 011X	BOUNCE CH_64..CH_49
00 100X	BOUNCE CH_80..CH_65
00 101X	BOUNCE CH_96..CH_81
00 110X	FAULT CH_16..CH_01
00 111X	FAULT CH_32..CH_17
01 000X	FAULT CH_48..CH_33
01 001X	FAULT CH_64..CH_49
01 010X	TEST PATTERN 0's and 1's
01 011X	FAULT CH_80..CH_65
01 100X	FAULT CH_96..CH_81
01 101X	DATA CH_16..CH_01
01 110X	DATA CH_32..CH_17
01 111X	DATA CH_48..CH_33
10 000X	DATA CH_64..CH_49
10 001X	DATA CH_80..CH_65
10 010X	DATA CH_96..CH_81
10 011X	NOT USED
10 100X	STATUS REGISTER
10 101X	TEST PATTERN 1's and 0's
10 110X	FACTORY TEST WORD 1
10 111X	FACTORY TEST WORD 2
11 000X	FACTORY TEST WORD 3
11 001X	FACTORY TEST WORD 4
11 010X	NOT USED
11 011X	:
11 111X	NOT USED

Notes for TABLES 3 and 4.

Note 1: A true BOUNCE bit indicates that the input signal of the associated channel changed in an alternating fashion i.e. OFF-ON-OFF or ON-OFF-ON in three successive samples at the selected sample rate.
Note 2: A FAULT bit that is true indicates that the associated channel has a major problem and the associated data should not be believed. A FAULT indication is a HARD FAULT condition indicating that the Built-In-Test has failed.
Note 3: A DATA bit indicates the input discrete state for the associated channel over the last two data samples taken.
Note 4: The two available TEST PATTERNS contain an alternating string of 1's and 0's, and 0's and 1's, which can be used to verify that all of the data bits are operational (i.e. there are no stuck bits). The two test patterns have been located at addresses of alternating address bits so that the address decoder bits are tested at the same time.

TABLE 4. BYTE MODE (8-BIT BUS)	
ADDRESS (A5..A0)	DATA (D7..D0)
00 0000	BOUNCE CH_08..CH_01
00 0001	BOUNCE CH_16..CH_09
00 0010	BOUNCE CH_24..CH_17
00 0011	BOUNCE CH_32..CH_25
00 0100	BOUNCE CH_40..CH_33
00 0101	BOUNCE_48..CH_41
00 0110	BOUNCE_56..CH_49
00 0111	BOUNCE_64..CH_57
00 1000	BOUNCE_73..CH_65
00 1001	BOUNCE_80..CH_74
00 1010	BOUNCE_88..CH_81
00 1011	BOUNCE_96..CH_89
00 1100	FAULT CH_08..CH_01
00 1101	FAULT CH_16..CH_09
00 1110	FAULT CH_24..CH_17
001111	FAULT CH_32..CH_25
01 0000	FAULT CH_40..CH_33
01 0001	FAULT CH_48..CH_41
01 0010	FAULT CH_56..CH_49
01 0011	FAULT CH_64..CH_57
01 0100	TEST PATTERN 0's and 1's
01 0101	TEST PATTERN 0's and 1's
01 0110	FAULT CH_73..CH_65
01 0111	FAULT CH_80..CH_74
01 1000	FAULT CH_88..CH_81
01 1001	FAULT CH_96..CH_89
01 1010	DATA CH_08..CH_01
01 1011	DATA CH_16..CH_09
01 1100	DATA CH_24..CH_17
01 1101	DATA CH_32..CH_25
01 1110	DATA CH_40..CH_33
01 1111	DATA CH_48..CH_41
10 0000	DATA CH_56..CH_49
10 0001	DATA CH_64..CH_57
10 0010	DATA CH_72..CH_65
10 0011	DATA CH_80..CH_73
10 0100	DATA CH_88..CH_81
10 0101	DATA CH_96..CH_89
10 0110	NOT USED
10 0111	NOT USED
10 1000	STATUS REGISTER LO
10 1001	STATUS REGISTER HI
10 1010	TEST PATTERN 1's and 0's
10 1011	TEST PATTERN 1's and 0's
10 1100	TEST WORD 1 LO
10 1101	TEST WORD 1 HI
10 1110	TEST WORD 2 LO
10 1111	TEST WORD 2 HI
11 0000	TEST WORD 3 LO
11 0001	TEST WORD 3 HI
11 0010	TEST WORD 4 LO
11 0011	TEST WORD 4 HI
11 0100	NOT USED
11 0111	:
11 1111	NOT USED

See Notes at left.

FACTORY TEST INPUTS: (Pins 39, 40, 149, and 150) The TMUX, TMODE, FMUX and FMODE input signals are used for factory testing and should be tied to logic 1 for the device to operate properly.

RESET: (Pin 41) The RESET signal is used to reset the device during factory testing. It is connected to an internal RC network to provide a power-on-reset for the device. Under normal operating conditions this pin should be a no-connect. If there is some reason to reset the device from external circuity this pin can be momentarily pulled to logic 0 through an open collector device. **Do not hard wire this pin to +5V or ground.**

OUTPUTS

DATA (D15..D0): (Pins 123-138) 8-bit byte or 16-bit word information is available on the data bus depending on the logic state of the BUS Select line described above.

In the Byte mode the upper and lower bytes are enabled separately so that bit 0 can be hard wired to bit 8, bit 1 to bit 9 etc. thereby providing an 8-bit data bus.

It is obviously important that the 8-bit mode be selected if these data bits are wired together or corrupted data will result. The available data can be found under the Address Lines section found on page 5.

FAULT: (Pin 148) The FAULT flag was designed to serve as an interrupt to the microprocessor when a HARD or SOFT error has been detected within the device (see Note 2 of TABLES 3 and 4). If this signal is asserted (logic 0) the Status Register should be read to determine the nature of the fault. Thereafter more detailed information can be found in the associated addressable registers. The Fault Flag will remain at a logic 0 for as long as the fault condition persists. FIGURE 5 illustrates the fault logic tree.

Note: Depending on the exact nature of the fault, the Fault Flag may return to logic 0 during the Built-In-Test interval (when the READY signal is at logic 0) if there is a persistent fault condition.

Fault Conditions:

FAULT is 0 for any of the following fault conditions. The reason for the fault can be obtained from the status register which is accessible *regardless* of READY state. TABLE 5 shows the contents of the status register.

A definition of each bit is as follows:

BIT FAULT: A logic 1 for this bit indicates that one of the channels has failed the Built-In-Test sequence; this BIT sequence is performed prior to every input sample taken. These signals are reset at the start of each Built-In-Test sequence, and will be set if any of the tests in the sequence fail.

DISCRETE FAULT: A logic 1 for this bit indicates that one of the channels detected a HARD failure during the Built-In-Test sequence or that the discrete input data word did not transfer to the data bus output properly when it was read. If a HARD fault was detected the offending channel can be determined by reading the associated FAULT data registers. If it was generated by a transfer error the DISCRETE TRANSFER FAULT bit in this status register will be set to logic 1.

ARINC FAULT: A logic 1 for this bit indicates that one of the channels detected a HARD failure during the Built-In-Test sequence or that the discrete input data word did not transfer to the ARINC transmitter section properly.

If a HARD fault was detected the offending channel can be determined by reading the associated FAULT data registers. If it was generated by a transfer error then no FAULT bits in the status register will be set to logic 1. †

ARINC READY: A logic 0 for this bit indicates that an ARINC transmission is currently in process. A logic 1 indicates that no ARINC transmission is currently in process. †

CLOCK_A FAULT: A logic 1 for this bit indicates that the primary 1 MHz clock circuitry is defective and that the device is running off the secondary 1 MHz clock.

CLOCK_B FAULT: A logic 1 for this bit indicates that the secondary 1 MHz clock circuitry is defective and cannot be used as a backup.

NO CLOCK: A logic 1 for this bit indicates that there is no 1 MHz clock being supplied to the device (or that both have failed).

DISCRETE TRANSFER FAULT: A logic 1 for this bit indicates that the discrete data word(s) did not transfer properly during the associated microprocessor read cycle (i.e. the word present on the data bus did not agree with the internal data). The most likely cause of this type of fault is a collision on the data bus during the read cycle.

Note: This condition is only monitored for the discrete data words, not for all of the available data.

TABLE 5. STATUS WORD BIT MAP

BIT	SIGNAL
00	BIT FAULT
01	DISCRETE FAULT
02	ARINC FAULT
03	ARINC READY
04	CLOCK_A FAULT
05	CLOCK_B FAULT
06	NO CLOCK
07	DISCRETE TRANSFER FAULT
08	LOGIC LOW (HIGH BYTE)
09	LOGIC LOW
10	LOGIC LOW
11	LOGIC LOW
12	LOGIC LOW
13	LOGIC LOW
14	LOGIC LOW
15	READY

Note: All bits available regardless of ready-state.

† This signal is only meaningful for the ARINC 429 device option.

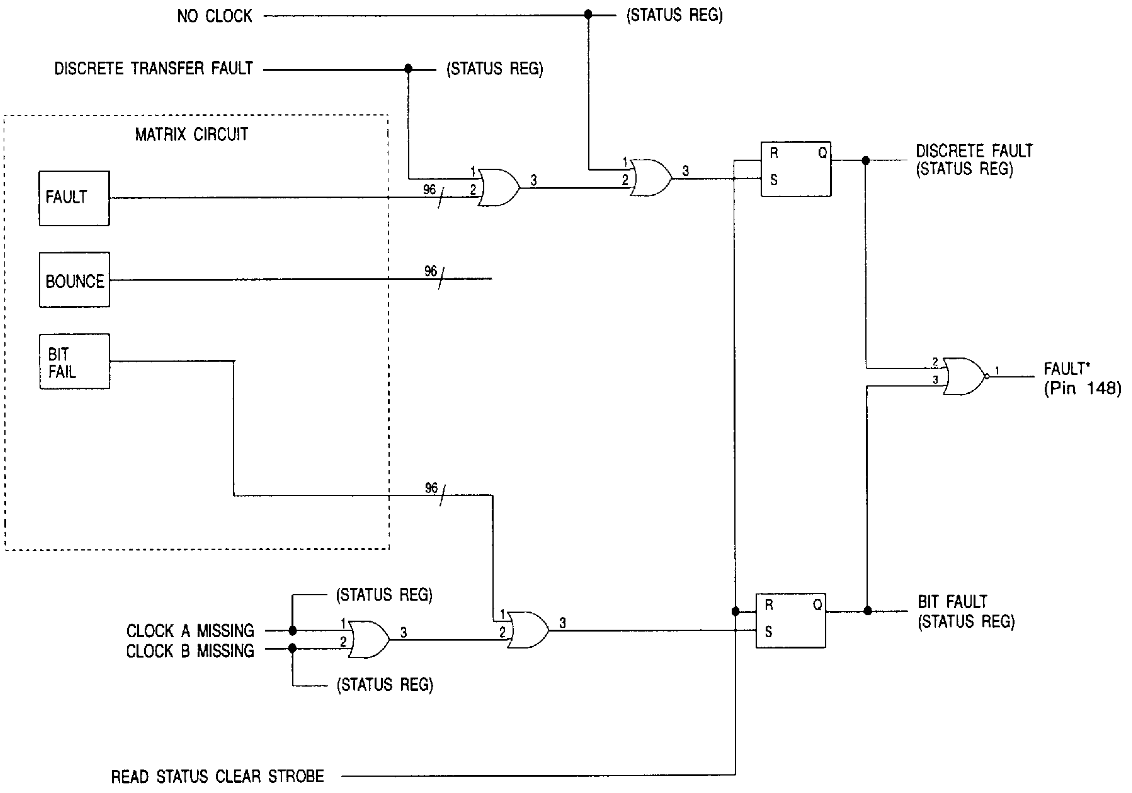


FIGURE 5. FAULT LOGIC TREE

CLKTST: (Pin 157) This signal is used for factory testing and should not be connected to any external circuitry or normal operation of the device could be affected. Specifically this signal is a low drive internal test point connected to the primary clock signal. Grounding this signal forces the device to switch to the secondary internal clock.

READY: (Pin 16) A logic 1 for this bit indicates that all of the available data is stable and can be read. A logic 0 indicates that the device is in the Built-In-Test mode, or taking a sample of the discrete input data lines.

This signal should be polled directly or by reading the status word prior to performing any read cycles. The internal data is guaranteed to be stable for 20 µs after the logic 1 to logic 0 transition (READY to NOT READY) of this signal. Therefore, it should not be necessary to repoll this signal after the read.

ARINC 429 PORT (OPTIONAL)

DD-03296XX-XX4 indicates the inclusion of the ARINC 429 data output. The option enables transmission of discrete data via a serial ARINC 429 (CMOS levels) output simultaneous with the 8/16-bit BUS output. The following features and pins apply:

ARINC 429 DATA RATE (429DRATE): (Pin 156) A logic 1 (or a no-connect) for this input selects the ARINC 429 low speed data rate of 12.5 kHz. A logic 0 selects the high speed data rate of 100 kHz. †

ARINC 429 MESSAGE RATE (429MRATE): (Pin 155) The message rate of the ARINC 429 output is selectable at either a fixed 100 ms rate or at the selected sampling rate of the input discretes. A logic 1 selects the input sampling rate as the message rate, and a logic 0 selects the fixed 100 ms message rate.†

Note: If the Low Speed ARINC 429 bit rate is selected (12.5 kHz) an entire ARINC message will take about 52 ms to complete, therefore, input discrete sampling rates of 5 ms, 10 ms, and 20 ms, and 50 ms cannot be utilized or the ARINC message will be truncated unless the fixed 100 ms message rate is selected.

429 STROBE IN (429STRBI): (Pin 153) This pin is utilized in the special case when the device is being used as a remote ARINC 429 serial port and not connected to a local microprocessor. When the device is being used in this specific configuration the associated 429 Strobe Out should be connected to this pin. In other cases this pin must be grounded.

Related Information: Because the BOUNCE data is momentarily latched within the device, this information is normally reset by a READ to the associated BOUNCE data words. In the instances when there is no microprocessor, and therefore no READS to the BOUNCE data, this connection provides a mechanism to reset the source of the BOUNCE information (just after it is transferred to the ARINC transmitter section) at the start of each ARINC message. †

† This signal is only meaningful for the ARINC 429 device option.

429 STROBE OUT (429STRB0): (Pin 154) This signal is used in conjunction with the "429 Strobe In" described above. It is basically a 500 ns positive pulse which occurs at the start of each 429 message. See the section "429 Strobe In" for further information concerning the use of this signal. †

ARINC_LO AND ARINC_HI: (Pins 151 and 152) These two signals comprise the ARINC 429 serial output transmission. Both are TTL compatible signals where the ARINC_LO signal contains the logic 0 serial transmission and the ARINC_HI signal contains the logic 1 serial transmission. These two signals must be connected to a DD-03182, 429 Line Driver, in order to obtain a single ended ARINC 429 transmission signal. FIGURE 9 illustrates this interface.

The content and word order of the ARINC 429 transmission is shown in FIGURE 6. †

As noted, these features are only guaranteed and tested if the ARINC 429 option is selected. In addition, the clock frequency (1 MHz) must be selected carefully so as not to interfere with other avionic communications as detailed in ARINC 429. The ARINC 429 option bit rate is derived from the (1 MHz) clock. Refer to ARINC 429 Bit Rate to avoid interference. ARINC 429-14 (January 4, 1993), paragraph 2.4 "Timing Related Elements" contains a "COMMENTARY" section following subparagraph 2.1.4.2 ("Low Speed Operation") that cautions against using "precisely" 100 kilobits per second.

† This signal is only meaningful for the ARINC 429 device option.

	P A R	SSM		M S B	16 BIT DATA														L S B		F	C	SDI		LABEL REVERSED OCTAL L S B							M S B	
ARINC 429 BITS:	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
FAULT 16..1	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	E	F	C	G	H	1	0	0	0	0	0	0	0	001
FAULT 32..17	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	E	F	C	G	H	0	1	0	0	0	0	0	0	002
FAULT 48..33	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	E	F	C	G	H	1	1	0	0	0	0	0	0	003
FAULT 64..49	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	E	F	C	G	H	0	0	1	0	0	0	0	0	004
FAULT 80..65	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	E	F	C	G	H	1	0	1	0	0	0	0	0	005
FAULT 96..81	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	E	F	C	G	H	0	1	1	0	0	0	0	0	006
BOUNCE 16..1	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	E	F	C	G	H	1	1	1	0	0	0	0	0	007
BOUNCE 32..17	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	E	F	C	G	H	0	0	0	1	0	0	0	0	010
BOUNCE 48..33	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	E	F	C	G	H	1	0	0	1	0	0	0	0	011
BOUNCE 64..49	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	E	F	C	G	H	0	1	0	1	0	0	0	0	012
TEST 5's	P	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	E	F	C	G	H	1	1	0	1	0	0	0	0	013
TEST A's	P	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	E	F	C	G	H	0	0	1	1	0	0	0	0	014
BOUNCE 80..65	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	E	F	C	G	H	1	0	1	1	0	0	0	0	015
BOUNCE 96..81	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	E	F	C	G	H	0	1	1	1	0	0	0'	0	016
DATA 16..1	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	E	F	C	G	H	1	1	1	1	0	0	0	0	017
DATA 32..17	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	E	F	C	G	H	0	0	0	0	1	0	0	0	020
DATA 48..33	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	E	F	C	G	H	1	0	0	0	1	0	0	0	021
DATA 64..49	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	E	F	C	G	H	0	1	0	0	1	0	0	0	022
DATA 80..65	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	E	F	C	G	H	1	1	0	0	1	0	0	0	023
DATA 96..81	P	A	B	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	E	F	C	G	H	0	0	1	0	1	0	0	0	024

Notes:

A B = 0 0 If there are no major faults.

A B = 1 1 If major faults exist (data is bad).

C = 0 When 429 data rate is 100kpbs; C=1 When data rate is 12.5 kbps.

D = Data bit.

F = 1 If the discrete interface output has any major faults (429 data may still be good).

P = ARINC 429 parity bit.

E = 1 If there is a bit fault.

G H = The value of these two locations will track channel 1 and 2 or can be hard-wired (via channel 1 and 2) to determine which R0D3 the 429 word came from.

The 20 words are transmitted in order shown from top to bottom.

FIGURE 6. ARINC BIT DESCRIPTION

OPTIONAL 429 LINE DRIVER

If you choose the 429 option for the DD-03296, you can use a line driver chip to transmit the data on the serial data bus. DDC has a device called the DD-03182 which will support ARINC 429, 571 and 575 bus standards. (See TABLE 6.)

The serial data is presented on DATA(A) and DATA(B) inputs in a dual rail format. The driver is enabled by the SYNC and CLOCK inputs. The output voltage level is programmed by the V_{REF} input and is normally tied to +5 VDC along with V_1 to produce output levels of +5 V, 0 V, and -5 V on each output for 10 V differential outputs. (See FIGURE 8.)

The output resistance is 75 Ohms ±20%: 37.5 Ohms on each output. The outputs are fused for fail-safe protection against shorts to aircraft power. The output slew rate is controlled by external timing capacitors on C_A and C_B. Typical Values are 75 pF for 100 kHz data and 500 pF for 12.5 kHz data.

DD-03182 PIN DESCRIPTION

See FIGURE 7 for reference.

Pin 1: V_{REF} (Input) - The voltage on V_{REF} sets the output voltage levels on A_{OUT} & B_{OUT}. The output logic levels swing between $+V_{REF}$ volts, 0 volts and $-V_{REF}$ volts.

Pins 2, 10, 15: N/C - No Connect

Pin 3: SYNC (Input) - Logic 0 outputs will be forced to NULL or MARK state. Logic 1 enables data transmission.

Pin 14: CLOCK (Input) - Logic 0 outputs will be forced to NULL or MARK state. Logic 1 enables data transmission.

Pins 4, 13: DATA(A)/DATA(B) (Inputs) - These signals contain the serial data to be transmitted on the ARINC 429 data bus.

Pins 5, 12: C_A/C_B (Analog) - External timing capacitors are tied from these points to ground to establish the output signal slew rate. Typically, $C_A=C_B=75$ pF for 100 kHz data and $C_A=C_B=500$ pF for 12.5 kHz data.

Pins 6, 11: A_{OUT}/B_{OUT} (Output) - These are the line driver outputs which are connected to the aircraft serial data bus.

Pin 7: -V (Input) - This is the negative supply input (-15 VDC nominal).

Pin 8: Gnd - Ground

Pin 9: +V (Input) This is the positive supply input (+15 VDC nominal).

Pin 16: V_1(Input) This is the logic supply input (+5 VDC nominal).

TABLE 6. DD-03182 SPECIFICATIONS

PARAMETER	UNITS	MIN	TYP	MAX
ABSOLUTE MAXIMUM RATINGS				
VOLTAGE BETWEEN PINS				
■ +V & -V	V			40
■ V_1 & GND	V			7
■ V_{REF} & GND	V			6
POWER SUPPLY REQUIREMENTS				
■ +V	VDC	10.5	15	16.5
■ -V	VDC	-10.5	-15	-16.5
■ V_1	VDC	4.75	5	5.25
■ V_{REF}	VDC	4.75	5	5.25
THERMAL				
Operating Temperature	°C	-55		+125
Storage Temperature	°C	-65		+150
Lead Temperature (localized, 10 sec duration)	°C			+300
Thermal Resistance:				
Junction to Case θ_{jc}	°C/W			35
Junction to Ambient θ_{ja}	°C/W			75

Note: Refer to DD-03182 data sheet for more information.

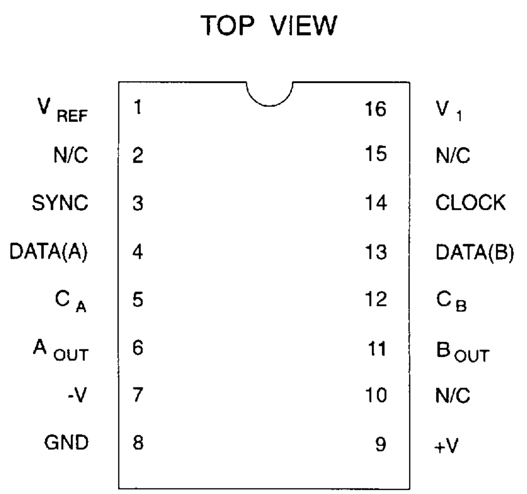


FIGURE 7. DD-03182 PIN OUT

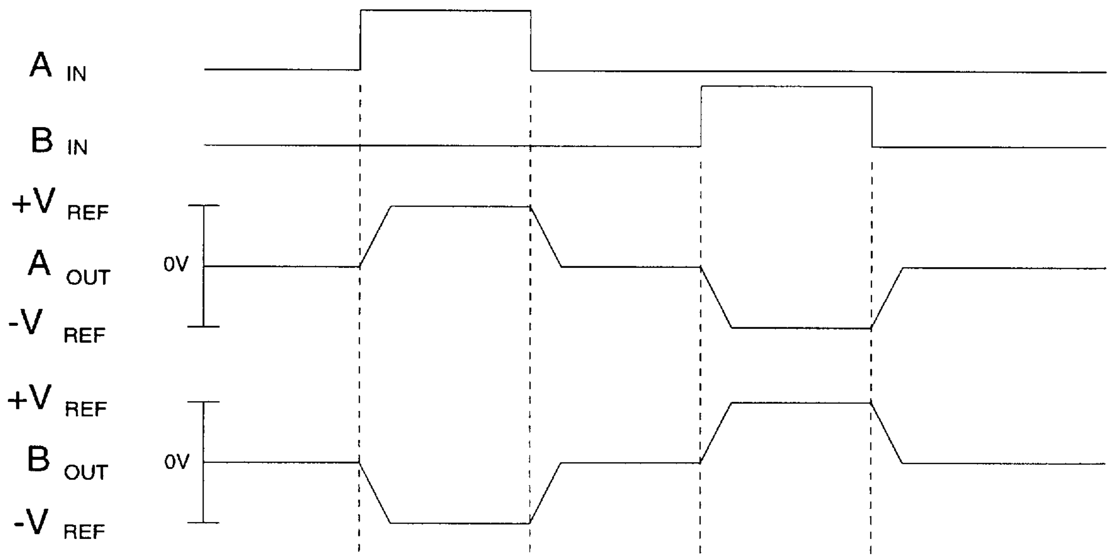
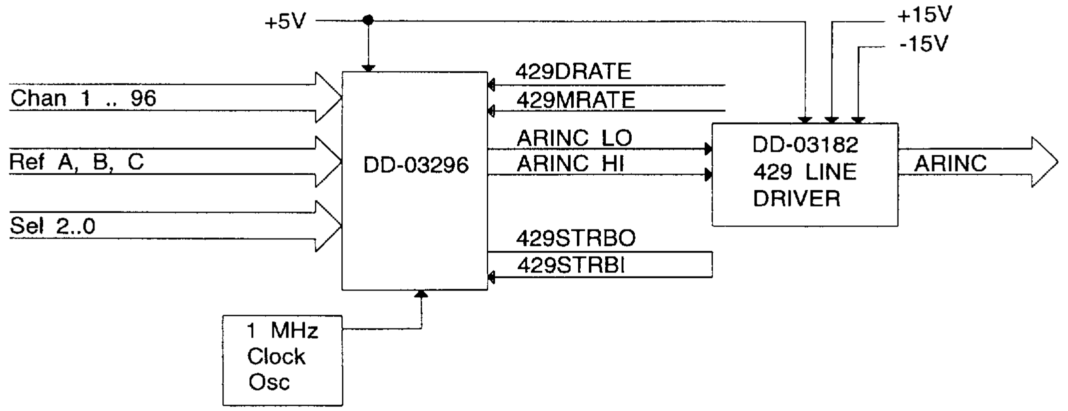


FIGURE 8. ARINC 429 WAVEFORM



NOTE:
1) 429 MRATE and DRATE can either be tied to GND or +5V (Refer to Page 8).
2) If the ARINC 429 option is not used, then pin 153 (429STRBI) MUST be grounded for the "bounce" circuit to operate properly.

FIGURE 9. DD-03296 TO ARINC 429 INTERFACE

4678769 0010813 611

TABLE 7. DD-03296 PIN FUNCTION					
PIN NUMBER	FUNCTION	PIN NUMBER	FUNCTION	PIN NUMBER	FUNCTION
1	CH_ 03	55	CH_ 41	109	CH_76
2	CH_ 04	56	CH_ 42	110	CH_75
3	CH_ 05	57	CH_ 43	111	CH_74
4	CH_ 06	58	CH_ 44	112	CH_73
5	CH_ 07	59	CH_ 45	113	N/C
6	CH_ 08	60	CH_ 46	114	N/C
7	N/C	61	CH_ 47	115	CH_72
8	CH_ 09	62	CH_ 48	116	CH_71
9	CH_ 10	63	N/C	117	CH._70
10	CH_ 11	64	TRIM: CH_ 65-96	118	CH_69
11	CH_ 12	65	REF.: CH 65-96	119	CH_68
12	CH_ 13	66	CH_ 49	120	CH_67
13	CH_ 14	67	CH_ 50	121	CH._66
14	CH_ 15	68	CH_ 51	122	CH_65
15	CH_ 16	69	CH_ 52	123	D15
16	READY	70	CH_ 53	124	D14
17	N/C	71	CH_ 54	125	D13
18	N/C	72	CH_ 55	126	D12
19	CH_ 17	73	CH_ 56	127	D11
20	CH_ 18	74	TRIM: CH_ 33-64	128	D10
21	CH_ 19	75	REF.: CH_ 33-64	129	D09
22	CH_ 20	76	CH_ 57	130	D08
23	CH_ 21	77	CH_ 58	131	D07
24	CH_ 22	78	CH_ 59	132	D06
25	CH_ 23	79	CH_ 60	133	D05
26	CH_ 24	80	CH_ 61	134	D04
27 (Note 1)	VDD (ANALOG)	81	CH_ 62	135	D03
28	1 MHz CLK..	82	CH_ 63	136	D02
29	CH_ 25	83	CH_ 64	137	D01
30	CH_ 26	84	N/C	138	D00
31	CH_ 27	85	CH_ 96	139	A05
32	CH_ 28	86	CH_ 95	140	A04
33	CH_ 29	87	CH_ 94	141 (Note 1)	GND. (DIGITAL)
34	CH_ 30	88	CH_ 93	142 (Note 1)	VDD (DIGITAL)
35	CH_ 31	89	CH_ 92	143	A03
36	CH_ 32	90	CH_ 91	144	A02
37	REF.: CH_ 01-32	91	CH_ 90	145	A01
38	TRIM: CH_ 01-32	92	CH_ 89	146	A00
39 (Note 2)	TMODE	93	N/C	147	ENABLE
40 (Note 2)	TMUX	94	N/C	148	FAULT
41 (Note 2)	RESET	95	CH_ 88	149 (Note 2)	FMUX
42	N/C	96	CH_ 87	150 (Note 2)	FMODE
43	N/C	97	CH_ 86	151	ARINC_LO
44	N/C	98	CH_ 85	152	ARINC_HI
45	CH_ 33	99	CH_ 84	153 (Note 4)	429STRBI
46	CH_ 34	100	CH_ 83	154	429_SRBO
47	CH_ 35	101	CH_ 82	155	429MRATE
48	CH_ 36	102	CH_ 81	156	429DRATE
49	CH_ 37	103 (Note 1)	GND. (ANALOG)	157 (Note 3)	CLKTEST
50	CH_ 38	104	8/16 BITS	158	SEL0
51	CH_ 39	105	CH_80	159	SEL1
52	CH_ 40	106	CH_ 79	160	SEL2
53	N/C	107	CH_78	161	CH_01
54	N/C	108	CH_77	162	CH_02

Notes for TABLE 7:

1: V_{DD} (Digital) and V_{DD} (Analog) MUST be connected to the same power source; GND (Digital) and GND (Analog) MUST be connected to the same GND potential.

2: These signals should be tied to +5V.

3: DO NOT CONNECT.

4: **This pin must be grounded if 429 option is not implemented.**

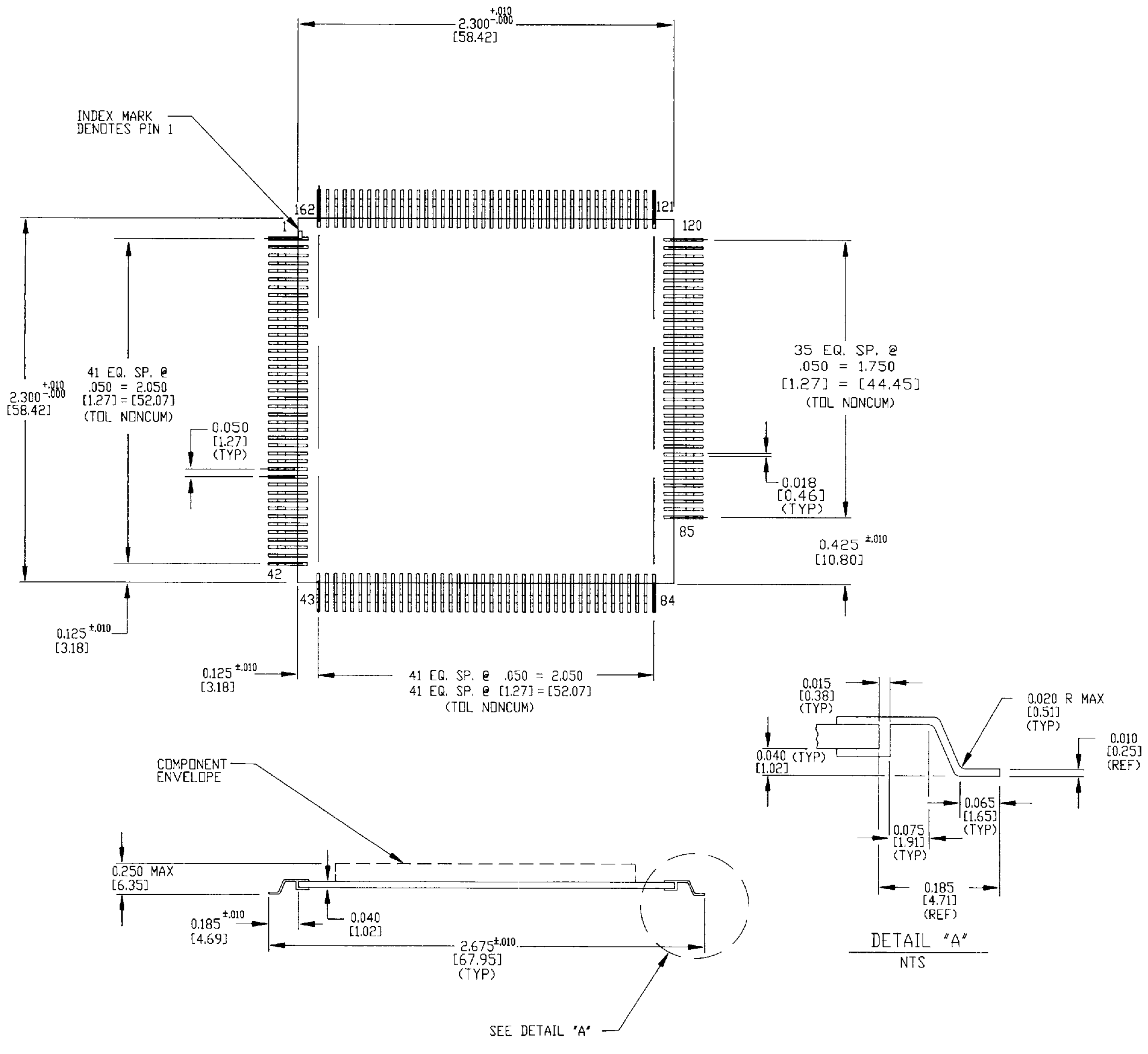


FIGURE 10. DD-03296 MECHANICAL OUTLINE

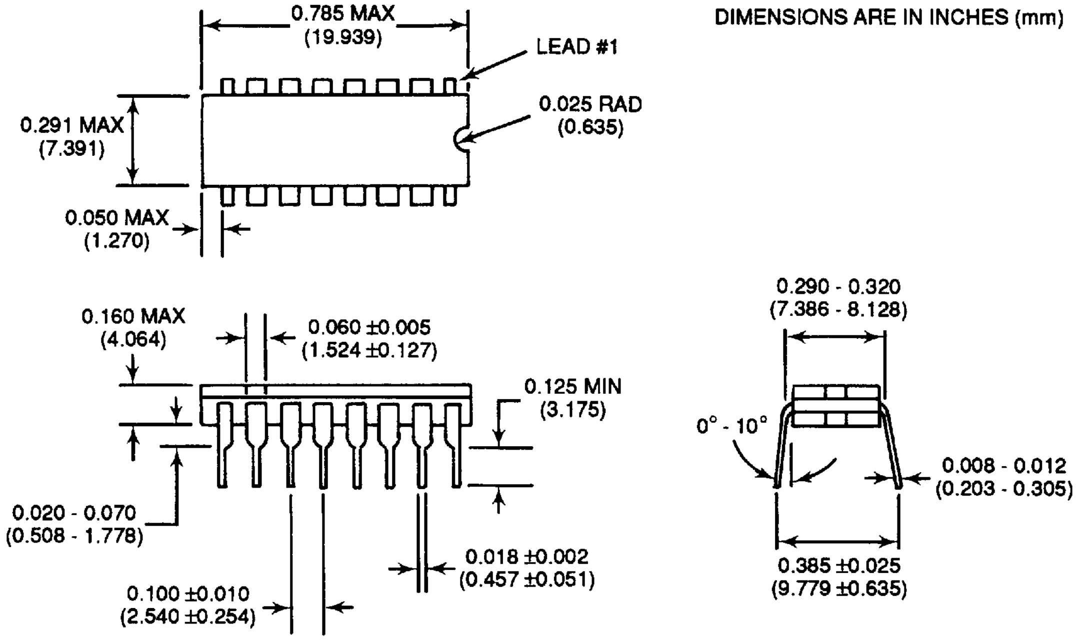


FIGURE 11. DD-03182 CERDIP (JE) MECHANICAL OUTLINE

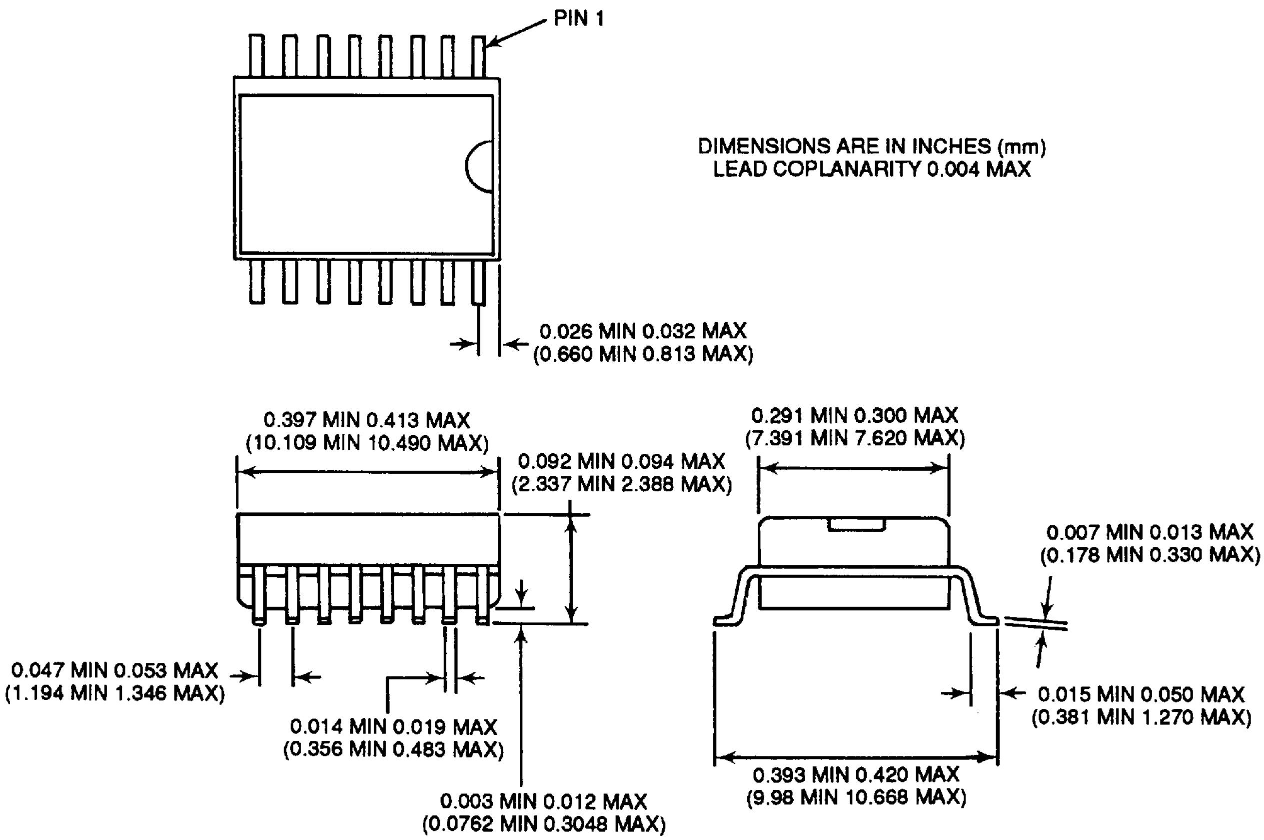


FIGURE 12. DD-03182 SURFACE MOUNT (SOIC) PACKAGE MECHANICAL OUTLINE

ORDERING INFORMATION

DD-03296FC-100

- **ARINC 429 Port Option:**
  - 0 = Without ARINC 429 output
  - 4 = With ARINC 429 output
- **Screening:**
  - 0 = Standard DDC Procedures
  - 2 = Burn-in (ceramic only)
- **Temperature Range:**
  - 1 = –55 to +125 °C (ceramic only)
  - 2 = –40 to +85 °C
  - 3 = 0 to +70 °C
- **ASIC Package Type:**
  - C = Ceramic
  - P = Plastic
- **Package Style:**
  - F = Surface Mount

OPTIONAL HARDWARE

DD-03182DC-100 — ARINC 429 Line Driver

- **Not Used**
- **Screening:**
  - 0 = Standard DDC Procedures
  - 2 = Burn-in (ceramic only)
- **Temperature Range:**
  - 1 = –55 to +125 °C (ceramic only)
  - 2 = –40 to +85 °C
- **Package Type:**
  - C = Ceramic
  - P = Plastic
- **Package Style:**
  - D = CERDIP (ceramic only)
  - G = Gull Wing (plastic only)
  - P = PLCC (plastic only)

OTHER APPLICABLE DOCUMENTS

RTCA/DO-160C: Environmental Conditions and Test Procedure for Airborne Equipment.