DRAM

4 MEG x 4 DRAM

3.3V, EDO PAGE MODE

AVAILABLE IN MILITARY SPECIFICATIONS

- MIL-STD-883
- SMD Planned

FEATURES

- Industry-standard x4 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- Low power, 1mW standby; 150mW active, typical
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) HIDDEN
- 2,048-cycle (11 row-, 11 column-addresses)
- Extended Data-Out (EDO) PAGE access cycle
- 5V-tolerant I/Os (5.5V maximum V_{IH} level)

OPTIONS — MARKING

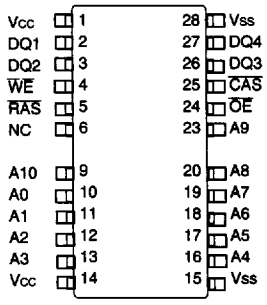
- Timing
  - 60ns access (Contact Factory) — -6
  - 70ns acess — -7
  - 80ns access — -8
- Packages
  - Ceramic SOJ — ECJ — No. 505
  - Ceramic LCC — EC — No. 212
  - Ceramic Gull Wing — ECG — No. 603

KEY TIMING PARAMETERS

SPEED	t_{RC}	t_{RAC}	t_{PC}	t_{AA}	t_{CAC}	t_{CAS}
-6	110ns	60ns	30ns	30ns	15ns	12ns
-7	130ns	70ns	35ns	35ns	18ns	15ns
-8	150ns	80ns	40ns	40ns	20ns	20ns

PIN ASSIGNMENT (Top View)

24/28-Pin



GENERAL DESCRIPTION

The AS4LC4M4 is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x4 configuration. The AS4LC4M4 $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pins remain open (High- Z) until the next $\overline{CAS}$ cycle, regardless of $\overline{OE}$.

A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. An EARLY WRITE occurs when $\overline{WE}$ is taken LOW prior to $\overline{CAS}$ falling. A LATE WRITE or READ-MODIFY-WRITE occurs when $\overline{WE}$ falls after $\overline{CAS}$ was taken LOW. During EARLY WRITE cycles, the data-outputs (Q) will remain High-Z regardless of the state of $\overline{OE}$. During LATE WRITE or READ-MODIFY-WRITE cycles, $\overline{OE}$ must be taken HIGH to disable the data-outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping $\overline{OE}$ LOW, no write will occur, and the data-outputs will drive read data from the accessed location.

The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

FAST PAGE MODE

FAST PAGE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined page boundary. The FAST PAGE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE of operation.

EDO PAGE MODE

The AS4LC4M4E8 provides EDO PAGE MODE which is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after $\overline{CAS}$ returns HIGH. EDO allows $\overline{CAS}$ precharge time (^tCP) to occur without the output data going invalid. This elimination of $\overline{CAS}$ output control allows pipeline READs.

FAST-PAGE-MODE DRAMs have traditionally turned the output buffers off (High-Z) with the rising edge of $\overline{CAS}$. EDO-PAGE-MODE DRAMs operate similarly to FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after $\overline{CAS}$ goes HIGH during READs, provided $\overline{RAS}$ and $\overline{OE}$ are held LOW. If $\overline{OE}$ is pulsed while $\overline{RAS}$ and $\overline{CAS}$ are LOW, data will toggle from valid data to High-Z and back to the same valid data. If $\overline{OE}$ is toggled or pulsed after $\overline{CAS}$ goes HIGH while $\overline{RAS}$ remains LOW, data will transition to and remain High-Z (refer to Figure 1). $\overline{WE}$ can also perform the function of disabling the output devices under certain conditions, as shown in Figure 2.

During an application, if the DQ outputs are wire OR'd, $\overline{OE}$ must be used to disable idle banks of DRAMs. Alternatively, pulsing $\overline{WE}$ to the idle banks during $\overline{CAS}$ high time will also High-Z the outputs. Independent of $\overline{OE}$ control, the outputs will disable after ^tOFF, which is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

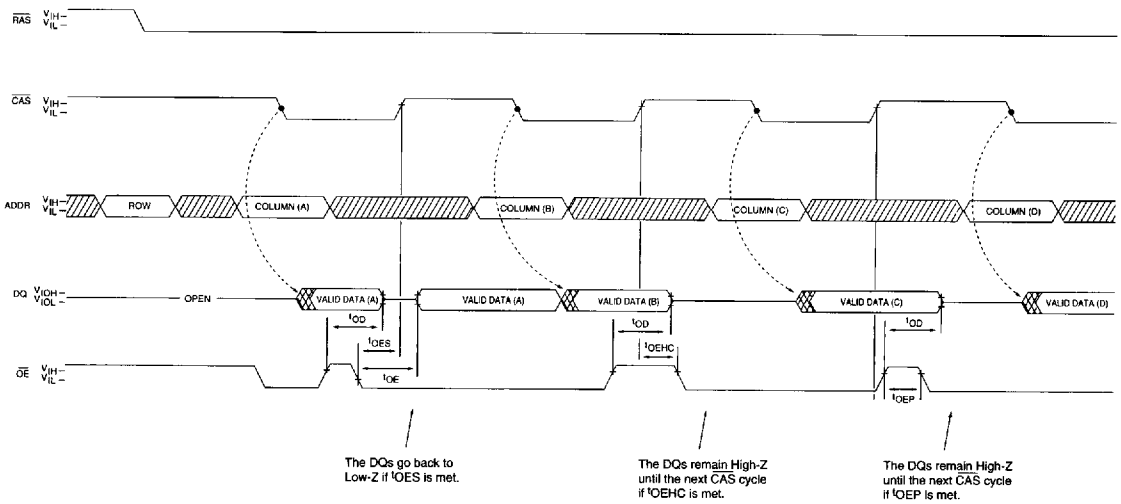


Figure 1
OUTPUT ENABLE AND DISABLE

REFRESH

Preserve correct memory cell data by maintaining power and executing a $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 2,048 combinations of $\overline{RAS}$ addresses are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic $\overline{RAS}$ addressing.

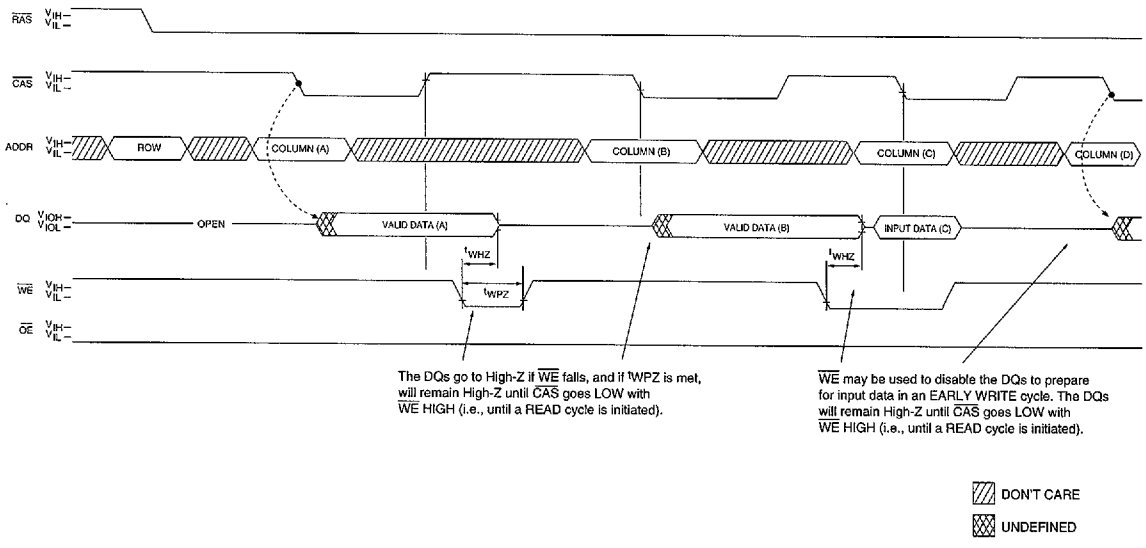


Figure 2
$\overline{WE}$ CONTROL OF DQs

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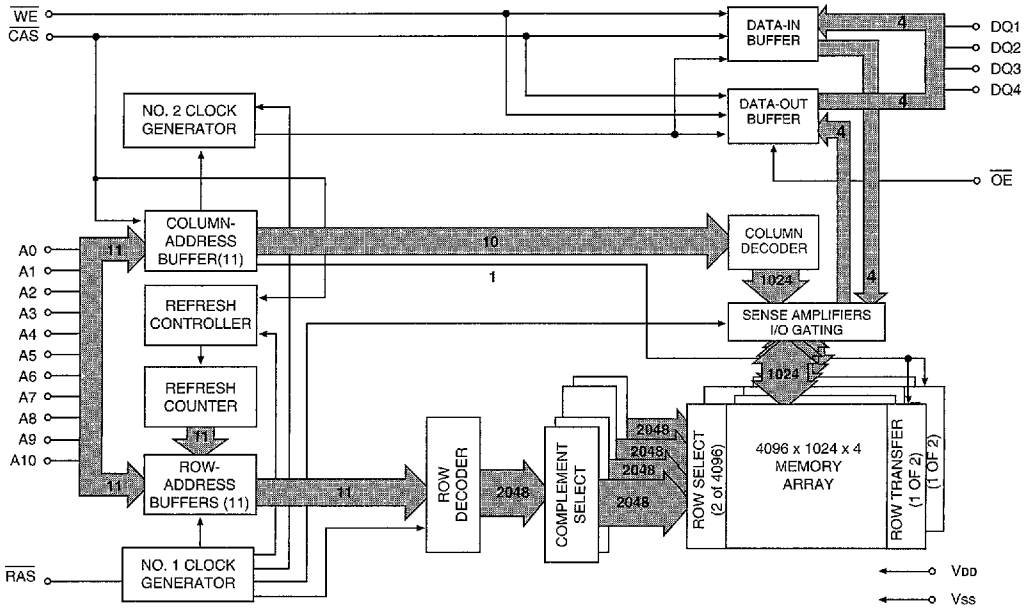
FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DATA-IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
EDO-PAGE-MODE	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
EDO-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
	Any Cycle	L	L→H	H	L	n/a	n/a	Data-Out
EDO-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data-Out
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
CBR REFRESH		H→L	L	H	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} pin Relative to V_{SS} ..... -1V to +4.6V
Voltage on NC, Inputs or I/O pins
Relative to V_{SS} ..... -1V to +5.5V
Operating Temperature, T_A (ambient) .. TA(MIN) = -55°C
..... TC (MAX) = 125°C
Storage Temperature ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs (including NC pins)	V_{IH}	2.0	VCC+1	V	
Input Low (Logic 0) Voltage, all inputs (including NC pins)	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 5.5V Vcc = 3.6V (All other pins not under test = 0V) (NC pins not tested)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V) Vcc=3.6V	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYM	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = other inputs = Vcc -0.2V	I_{CC2}	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling: ^tRC = ^tRC [MIN])	I_{CC3}	120	110	100	mA	3, 4, 12
OPERATING CURRENT: EDO PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: ^tPC = ^tPC [MIN])	I_{CC4}	110	100	90	mA	3, 4, 12
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	120	110	100	mA	3, 12
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling: ^tRC = ^tRC [MIN])	I_{CC6}	120	110	100	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Address pins	C_{I1}	7	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	8	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		30		35		40	ns	
Column-address set-up to $\overline{CAS}$ precharge during write	^tACH	15		15		20		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	45		55		60		ns	
Column-address setup time	^tASC	0		0		0		ns	
Row-address setup time	^tASR	0		0		0		ns	
Column-address to $\overline{WE}$ delay time	^tAWD	55		65		65		ns	20
Access time from $\overline{CAS}$	^tCAC		15		20		20	ns	14
Column-address hold time	^tCAH	10		15		15		ns	
$\overline{CAS}$ pulse width	^tCAS	12	10,000	15	10,000	20	10,000	ns	
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		15		15		ns	5
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Data output hold after next $\overline{CAS}$ LOW	^tCOH	5		5		5		ns	
$\overline{CAS}$ precharge time	^tCP	10		10		10		ns	15
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		40	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
$\overline{CAS}$ hold time	^tCSH	50		55		60		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	5		5		10		ns	5
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	35		40		45		ns	20
Write command to $\overline{CAS}$ lead time	^tCWL	15		15		20		ns	
Data-in hold time	^tDH	10		12		15		ns	21
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	40		56		55		ns	
Data-in setup time	^tDS	0		0		0		ns	21
Output disable	^tOD	0	15	0	15		20	ns	
Output Enable	^tOE		15		20		20	ns	22
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	10		12		15		ns	
$\overline{OE}$ HIGH hold from $\overline{CAS}$ HIGH	^tOEHC	10		10		10		ns	
$\overline{OE}$ HIGH pulse width	^tOEP	10		10		10		ns	
$\overline{OE}$ LOW to $\overline{CAS}$ HIGH setup time	^tOES	5		5		5		ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

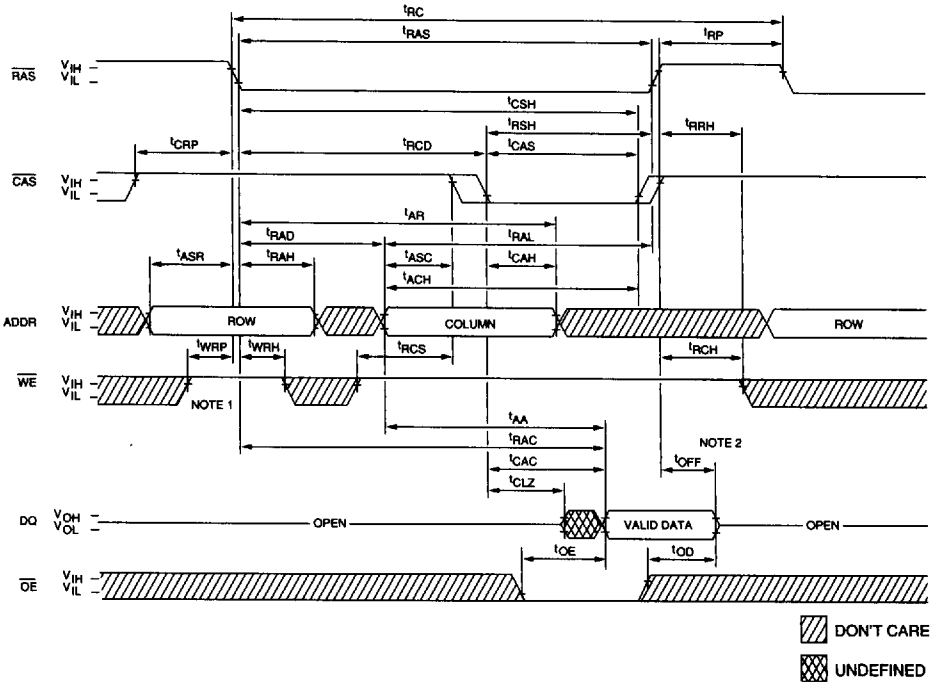
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	^tOFF	0	15	0	15	0	20	ns	
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		0		ns	19
EDO-PAGE-MODE READ or WRITE cycle time	^tPC	30		35		40		ns	
EDO-PAGE-MODE READ-WRITE cycle time	^tPRWC	75		85		90		ns	
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	13
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	15	40	ns	17
Row-address hold time	^tRAH	10		10		10		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
$\overline{RAS}$ pulse width	^tRAS	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ pulse width (EDO PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,00	ns	
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	16	45	16	50	20	60	ns	16
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	18
Read command setup time	^tRCS	0		0		0		ns	
Refresh period (2,048 cycles)	^tREF		32		32		32	ms	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	5		5		5		ns	
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	18
$\overline{RAS}$ hold time	^tRSH	13		15		15		ns	
READ WRITE cycle time	^tRWC	150		180		200		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^tRWD	80		90		105		ns	20
Write command to $\overline{RAS}$ lead time	^tRWL	15		15		20		ns	
Transition time (rise or fall)	^tT	2	30	2	30	2	30	ns	
Write command hold time	^tWCH	10		12		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	40		56		60		ns	
$\overline{WE}$ command setup time	^tWCS	0		0		0		ns	20
Output disable delay from $\overline{WE}$	^tWHZ	0	14	0	16	0	20	ns	
Write command pulse width	^tWP	10		12		15		ns	
$\overline{WE}$ pulse to disable at $\overline{CAS}$ HIGH	^tWPZ	10		12		15		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		10		ns	24
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		10		ns	24

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3.3V; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the ful temperature range is assured.
7. An initail pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any thime the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 2.5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. Column address changed once each cycle.
12. Measured with a load equivalent to two TTL gates, 100pF and V_{OL} = 0.8V and V_{OH} = 2.0V.
13. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
14. Assumes that $^tRCD \geq ^tRCD$ (MAX).
15. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
16. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC, provided ^tRAD is not exceeded.
17. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA, provided ^tRCD is not exceeded.
18. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
19. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}. It is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.
20. ^tWCS, ^tRWD, ^tAWD and ^tCWD are not restrictive operating parameters. ^tWCS applies to EARLY WRITE cycles. ^tRWD, ^tAWD and ^tCWD apply to READ-MODIFY-WRITE cycles. If $^tWCS \geq ^tWCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tWCS < ^tWCS$ (MIN) and $^tRWD \geq ^tRWD$ (MIN), $^tAWD \geq ^tAWD$ (MIN) and $^tCWD \geq ^tCWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ^tWCS, ^tRWD, ^tCWD and ^tAWD are not applicable in a LATE WRITE cycle.
21. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
22. If $\overline{OE}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted. Additionally, $\overline{WE}$ must be pulsed during $\overline{CAS}$ HIGH time in order to place I/O buffers in High-Z.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
24. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR REFRESH cycle.

READ CYCLE



NOTE:
1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.
2. ^{t}OFF is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}AA		30		35		40	ns
^{t}ACH	15		15		20		ns
^{t}AR	45		50		60		ns
^{t}ASC	0		0		0		ns
^{t}ASR	0		0		0		ns
^{t}CAC		15		20		20	ns
^{t}CAH	10		15		15		ns
^{t}CAS	12	10,000	15	10,000	20	10,000	ns
^{t}CLZ	0		0		0		ns
^{t}CRP	5		5		5		ns
^{t}CSH	50		55		60		ns
^{t}OD	0	15	0	15		20	ns
^{t}OE		15		20		20	ns
^{t}OFF	0	15	0	15	0	20	ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}RAC		60		70		80	ns
^{t}RAD	15	30	15	35	15	40	ns
^{t}RAH	10		10		10		ns
^{t}RAL	30		35		40		ns
^{t}RAS	60	10,000	70	10,000	80	10,000	ns
^{t}RC	110		130		150		ns
^{t}RCD	16	45	16	50	20	60	ns
^{t}RCH	0		0		0		ns
^{t}RCS	0		0		0		ns
^{t}RP	40		50		60		ns
^{t}RRH	0		0		0		ns
^{t}RSH	10		12		15		ns
^{t}WRH	10		10		10		ns
^{t}WRP	10		10		10		ns

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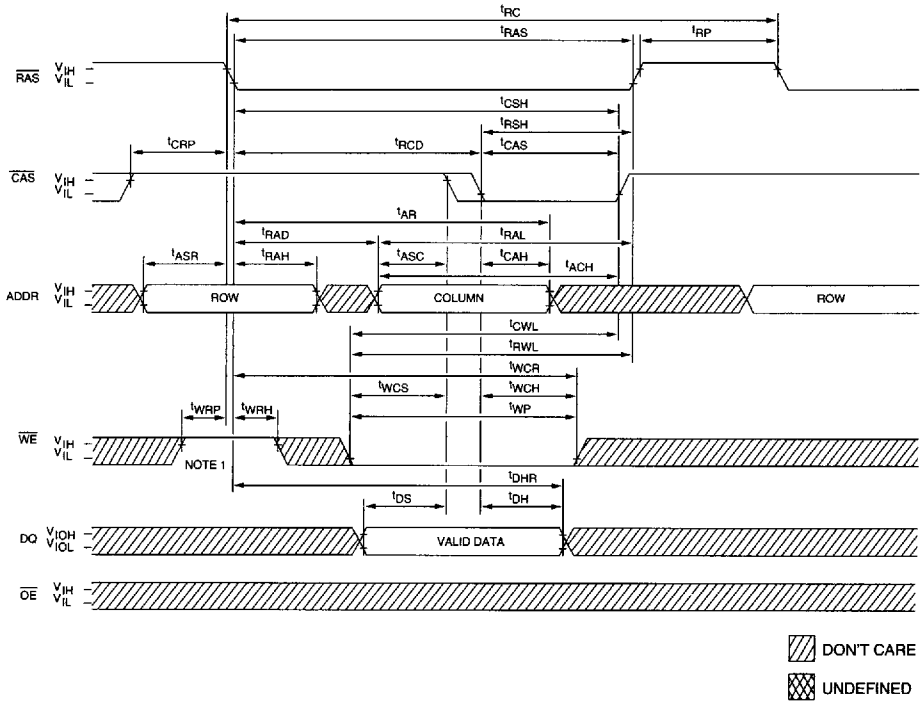
EARLY WRITE CYCLE



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

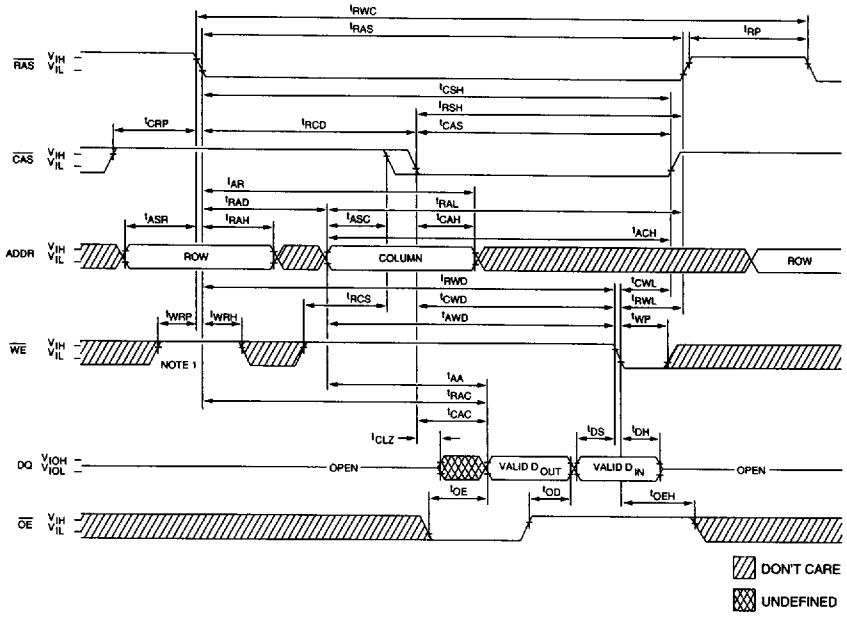
TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}ACH	15		15		20		ns
^{t}AR	45		55		60		ns
^{t}ASC	0		0		0		ns
^{t}ASR	0		0		0		ns
^{t}CAH	10		15		15		ns
^{t}CAS	12	10,000	15	10,000	20	10,000	ns
^{t}CRP	5		5		5		ns
^{t}CSH	50		55		60		ns
^{t}CWL	15		15		20		ns
^{t}DH	10		12		15		ns
^{t}DHR	40		50		55		ns
^{t}DS	0		0		0		ns
^{t}RAD	15	30	15	35	15	40	ns
^{t}RAH	10		10		10		ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}RAL	30		35		40		ns
^{t}RAS	60	10,000	70	10,000	80	10,000	ns
^{t}RC	110		130		150		ns
^{t}RCD	16	45	16	50	20	60	ns
^{t}RP	40		50		60		ns
^{t}RSH	13		15		0		ns
^{t}RWL	15		15		20		ns
^{t}WCH	10		12		15		ns
^{t}WCR	40		50		60		ns
^{t}WCS	0		0		0		ns
^{t}WP	10		12		15		ns
^{t}WRH	10		10		10		ns
^{t}WRP	10		10		10		ns

10

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



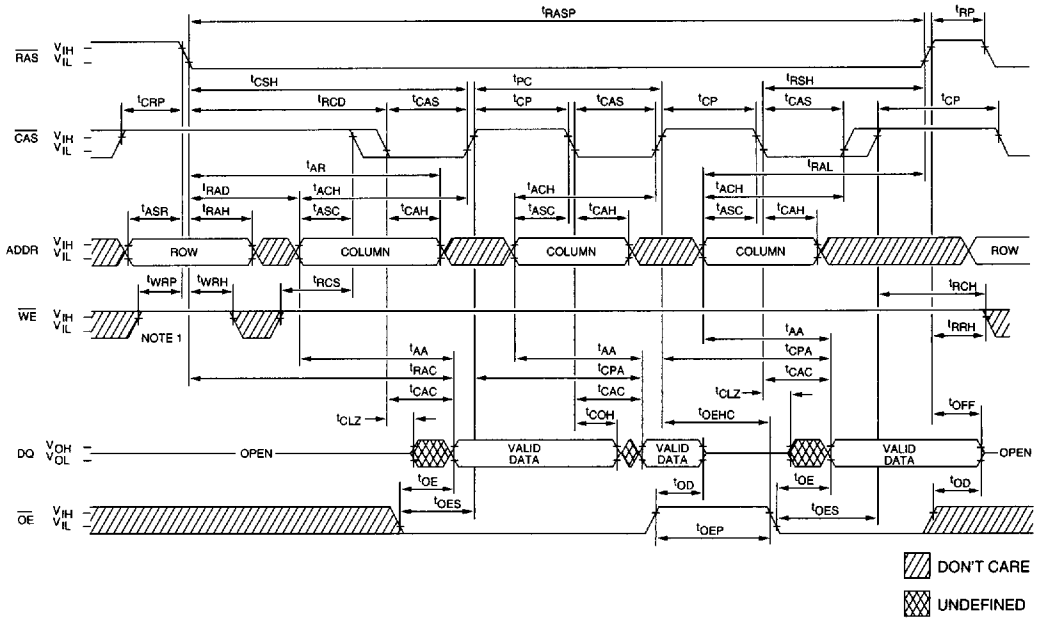
NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}AA		30		35		40	ns
^{t}ACH	15		15		20		ns
^{t}AR	45		55		60		ns
^{t}ASC	0		0		0		ns
^{t}ASR	0		0		0		ns
^{t}AWD	55		65		65		ns
^{t}CAC		15		20		20	ns
^{t}CAH	10		15		15		ns
^{t}CAS	12	10,000	15	10,000	20	10,000	ns
^{t}CLZ	0		0		0		ns
^{t}CRP	5		5		5		ns
^{t}CSH	50		55		60		ns
^{t}CWD	35		40		45		ns
^{t}CWL	15		15		20		ns
^{t}DH	10		12		15		ns
^{t}DS	0		0		0		ns
^{t}OD	0	15	0	15	0	20	ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}OE		15		20		20	ns
^{t}OEH	10		12		15		ns
^{t}RAC		60		70		80	ns
^{t}RAD	15	30	15	35	15	40	ns
^{t}RAH	10		10		10		ns
^{t}RAL	30		35		40		ns
^{t}RAS	60	10,000	70	10,000	80	10,000	ns
^{t}RCD	16	45	16	50	20	60	ns
^{t}RCS	0		0		0		ns
^{t}RP	40		50		60		ns
^{t}RSH	13		15		15		ns
^{t}RWC	150		180		200		ns
^{t}RWD	80		90		105		ns
^{t}RWL	15		15		20		ns
^{t}WP	10		12		15		ns
^{t}WRH	10		10		10		ns
^{t}WRP	10		10		10		ns

EDO-PAGE-MODE READ CYCLE



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

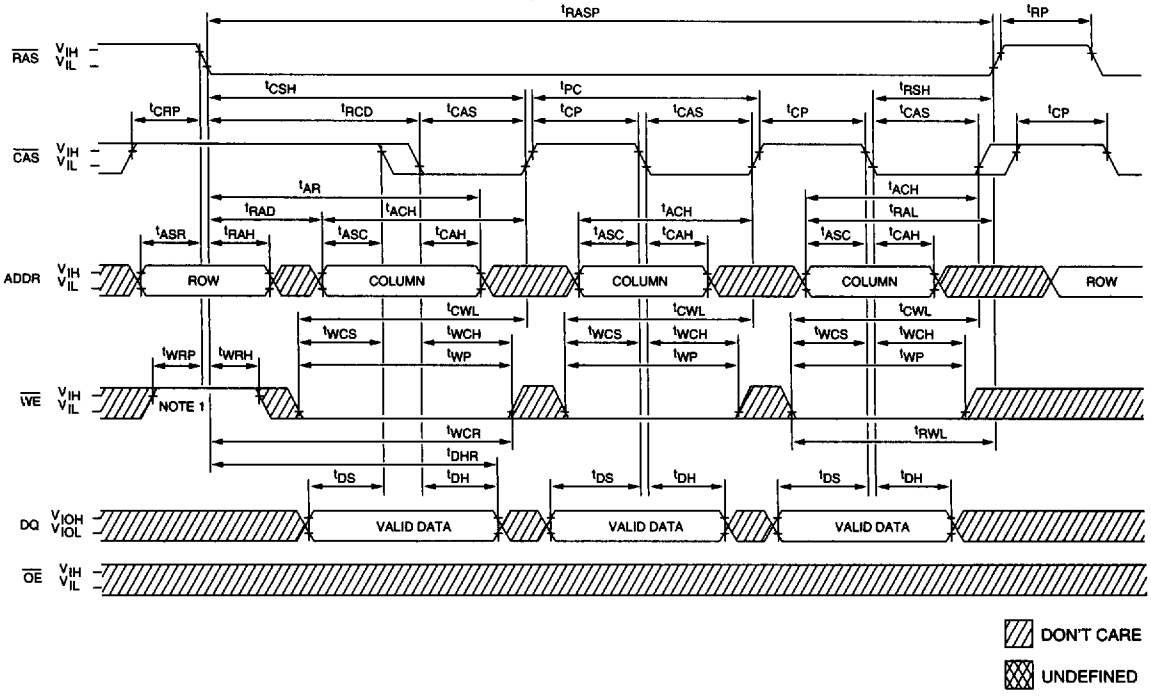
TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tAA		30		35		40	ns
tACH	15		15		20		ns
tAR	45		55		60		ns
tASC	0		0		0		ns
tASR	0		0		0		ns
tCAC		15		20		20	ns
tCAH	10		15		15		ns
tCAS	12	10,000	15	10,000	20	10,000	ns
tCLZ	0		0		0		ns
tCOH	5		5		5		ns
tCP	10		10		10		ns
tCPA		35		40		40	ns
tCRP	5		5		5		ns
tCSH	50		55		60		ns
tOD	0	15	0	15	0	20	ns
tOE		15		20		20	ns
tOEHC	10		10		10		ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tOEP	10		10		10		ns
tOES	5		5		5		ns
tOFF	0	15	0	15	0	20	ns
tPC	30		35		40		ns
tRAC		60		70		80	ns
tRAD	15	30	15	35	15	40	ns
tRAH	10		10		10		ns
tRAL	30		35		40		ns
tRASP	60	100,000	70	100,000	80	100,000	ns
tRCD	16	45	16	50	20	60	ns
tRCH	0		0		0		ns
tRCS	0		0		0		ns
tRP	40		50		60		ns
tRRH	0		0		0		ns
tRSH	13		15		15		ns
tWRH	10		10		10		ns
tWRP	10		10		10		ns

12

EDO-PAGE-MODE EARLY-WRITE CYCLE



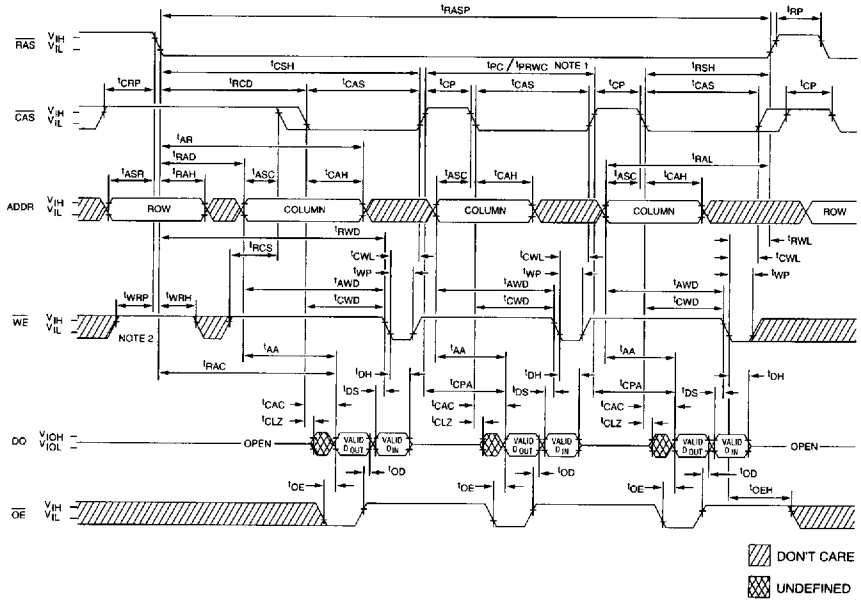
NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^tWRP and ^tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^tACH	15		15		20		ns
^tAR	45		55		60		ns
^tASC	0		0		0		ns
^tASR	0		0		0		ns
^tCAH	10		12		15		ns
^tCAS	12	10,000	15	10,000	20	10,000	ns
^tCP	10		10		10		ns
^tCRP	5		5		5		ns
^tCSH	50		55		60		ns
^tCWL	15		15		20		ns
^tDH	10		12		15		ns
^tDHR	40		50		55		ns
^tDS	0		0		0		ns
^tPC	30		35		40		ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^tRAD	15	30	15	35	15	40	ns
^tRAH	10		10		10		ns
^tRAL	30		35		40		ns
^tRASP	60	100,000	70	100,000	80	100,00	ns
^tRCD	16	45	16	50	20	60	ns
^tRP	40		50		60		ns
^tRSH	13		15		15		ns
^tRWL	15		15		20		ns
^tWCH	10		12		15		ns
^tWCR	40		50		60		ns
^tWCS	0		0		0		ns
^tWP	10		12		15		ns
^tWRH	10		10		10		ns
^tWRP	10		10		10		ns

EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



NOTE:
1. tPC is for LATE WRITE cycles only.
2. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tAA		30		35		40	ns
tAR	45		55		60		ns
tASC	0		0		0		ns
tASR	0		0		0		ns
tAWD	55		65		65		ns
tCAC		15		20		20	ns
tCAH	10		15		15		ns
tCAS	12	10,000	15	10,000	20	10,000	ns
tCLZ	0		0		0		ns
tCP	10		10		10		ns
tCPA		35		40		40	ns
tCRP	5		5		5		ns
tCSH	50		55		60		ns
tCWD	35		40		45		ns
tCWL	15		15		20		ns
tDH	10		12		15		ns
tDS	0		0		0		ns
tOD	0	15	0	15	0	20	ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tOE		15		20		20	ns
tOEH	10		12		15		ns
tPC	30		35		40		ns
tPRWC	75		85		90		ns
tRAC		60		70		80	ns
tRAD	15	30	15	35	15	40	ns
tRAH	10		10		10		ns
tRAL	30		35		40		ns
tRASP	60	100,000	70	100,000	80	100,000	ns
tRCD	16	45	16	50	20	60	ns
tRCS	0		0		0		ns
tRP	40		50		60		ns
tRSH	13		15		15		ns
tRWD	80		90		105		ns
tRWL	15		15		20		ns
tWP	10		12		15		ns
tWRH	10		10		10		ns
tWRP	10		10		10		ns

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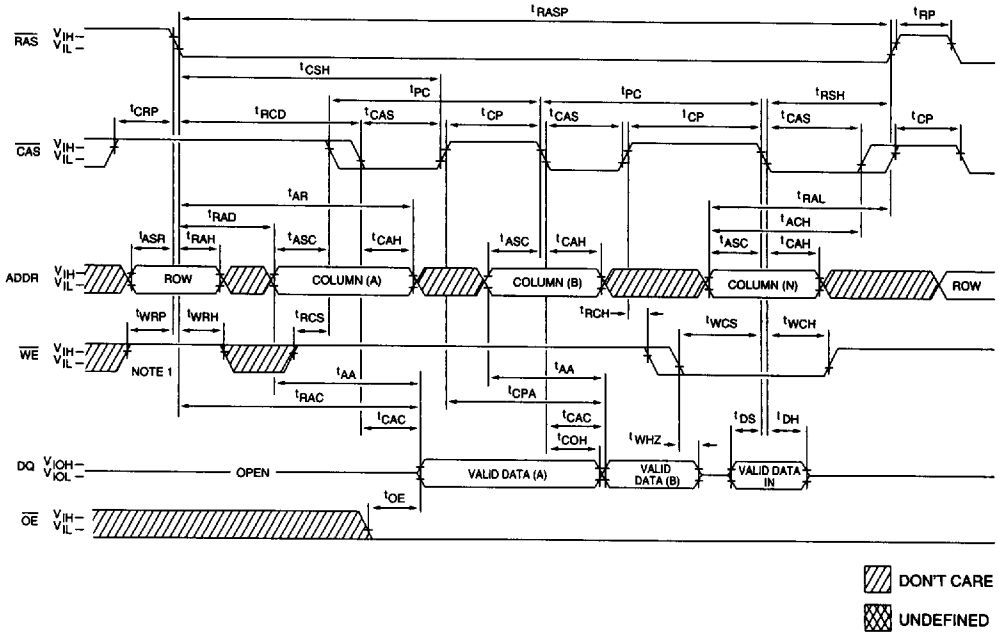
EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



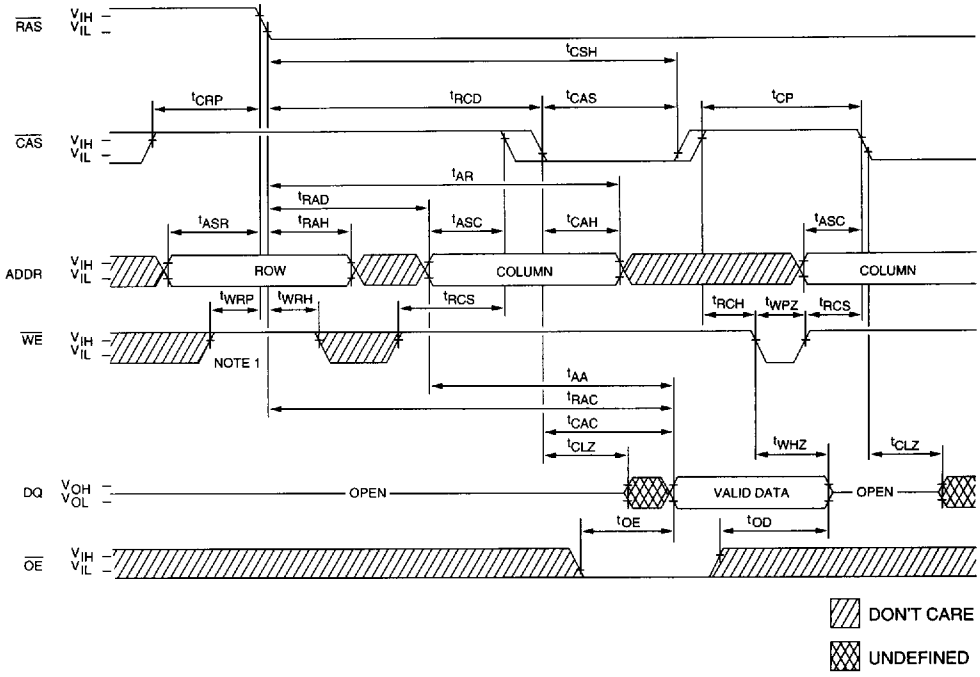
NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tAA		30		35		40	ns
tACH	15		15		20		ns
tAR	45		55		60		ns
tASC	0		0		0		ns
tASR	0		0		0		ns
tCAC		15		20		20	ns
tCAH	10		15		15		ns
tCAS	12	10,000	15	10,000	20	10,000	ns
tCOH	5		5		5		ns
tCP	10		10		10		ns
tCPA		35		40		40	ns
tCRP	5		5		5		ns
tCSH	50		55		60		ns
tDH	10		12		15		ns
tDS	0		0		0		ns
tOE		15		20		20	ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tPC	30		35		40		ns
tRAC		60		70		80	ns
tRAD	15	30	15	35	15	40	ns
tRAH	10		10		10		ns
tRAL	30		35		40		ns
tRASP	60	100,000	70	100,000	80	100,000	ns
tRCD	16	45	16	50	20	60	ns
tRCH	0		0		0		ns
tRCS	0		0		0		ns
tRP	40		50		60		ns
tRSH	13		15		15		ns
tWCH	10		12		15		ns
tWCS	0		0		0		ns
tWHZ	0	13	0	15	0	15	ns
tWRH	10		10		10		ns
tWRP	10		10		10		ns

READ CYCLE
(with $\overline{WE}$-controlled disable)



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

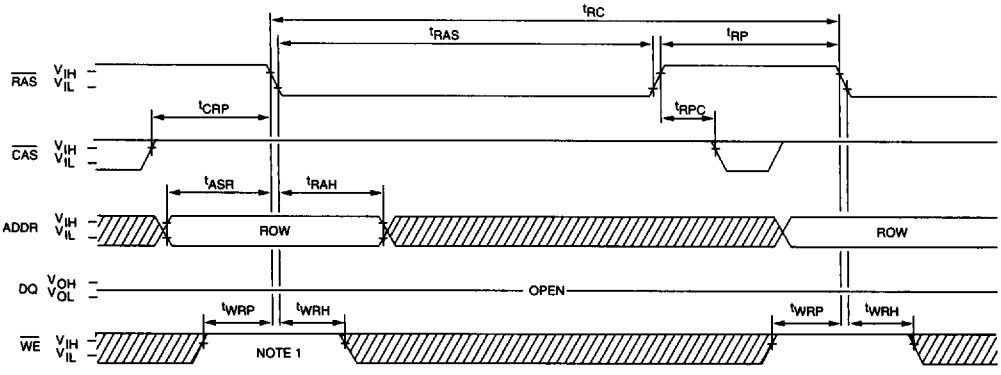
TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tAA		30		35		40	ns
tAR	45		55		60		ns
tASC	0		0		0		ns
tASR	0		0		0		ns
tCAC		15		20		20	ns
tCAH	10		15		15		ns
tCAS	12	10,000	15	10,000	20	10,000	ns
tCLZ	0		0		0		ns
tCP	10		10		10		ns
tCRP	5		5		5		ns
tCSH	50		55		60		ns
tOD	0	15	0	15	0	20	ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tOE		15		20		20	ns
tRAC		60		70		80	ns
tRAD	15	30	15	35	15	40	ns
tRAH	10		10		10		ns
tRCD	16	45	16	50	20	60	ns
tRCH	0		0		0		ns
tRCS	0		0		0		ns
tWHZ	0	14	0	16	0	20	ns
tWPZ	10		12		15		ns
tWRH	10		10		10		ns
tWRP	10		10		10		ns

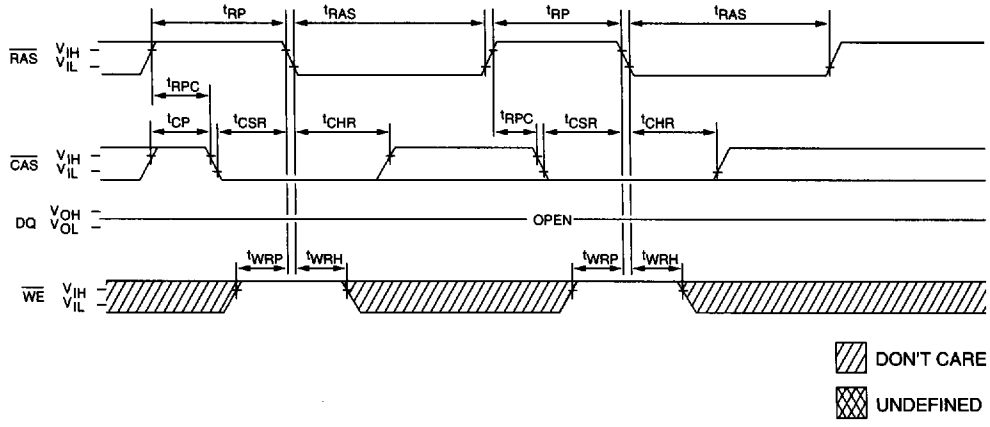
16

$\overline{RAS}$-ONLY REFRESH CYCLE



CBR REFRESH CYCLE

(Addresses and $\overline{OE}$ = DON'T CARE)



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

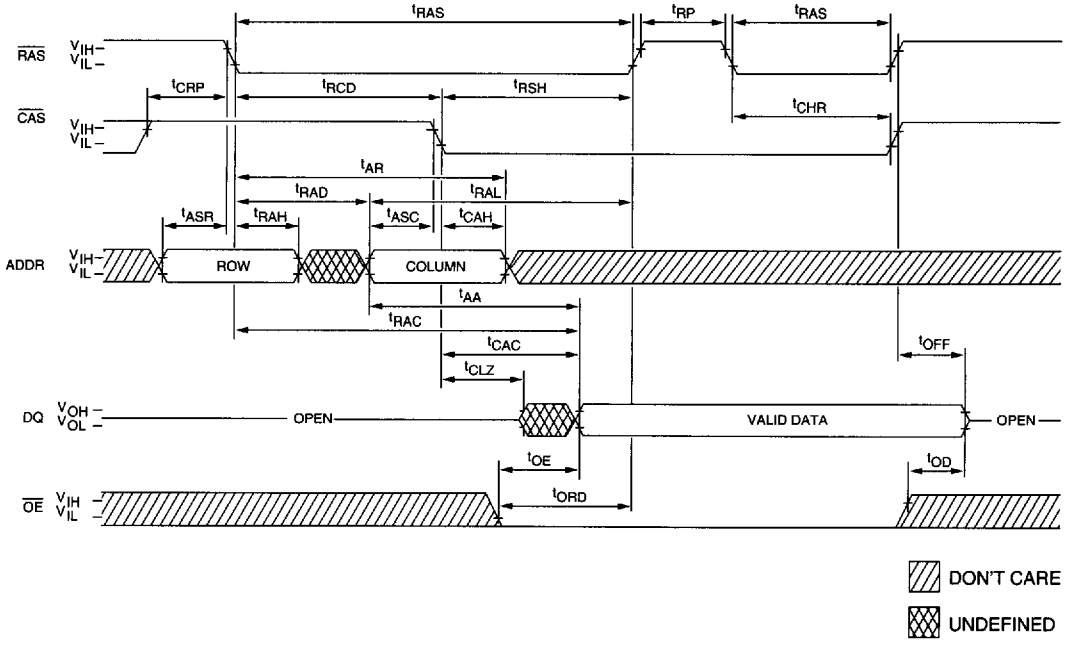
TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}ASR	0		0		0		ns
^{t}CHR	10		15		15		ns
^{t}CP	10		10		10		ns
^{t}CRP	5		5		5		ns
^{t}CSR	5		5		10		ns
^{t}RAH	10		10		10		ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}RAS	60	10,000	70	10,000	80	10,000	ns
^{t}RC	110		130		150		ns
^{t}RP	40		50		60		ns
^{t}RPC	5		5		5		ns
^{t}WRH	10		10		10		ns
^{t}WRP	10		10		10		ns

17

HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



TIMING PARAMETERS

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tAA		30		35		40	ns
tAR	45		55		60		ns
tASC	0		0		0		ns
tASR	0		0		0		ns
tCAC		15		20		20	ns
tCAH	10		15		15		ns
tCHR	10		15		15		ns
tCLZ	0		0		0		ns
tCRP	5		5		5		ns
tOD	0	15	0	15	0	20	ns
tOE		15		20		20	ns

	-6		-7		-8		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tOFF	0	15	0	15	0	20	ns
tORD	0		0		0		ns
tRAC		60		70		80	ns
tRAD	15	30	15	35	15	40	ns
tRAH	10		10		10		ns
tRAL	30		35		40		ns
tRAS	60	10,000	70	10,000	80	10,000	ns
tRCD	16	45	16	50	20	60	ns
tRP	40		50		60		ns
tRSH	13		15		15		ns

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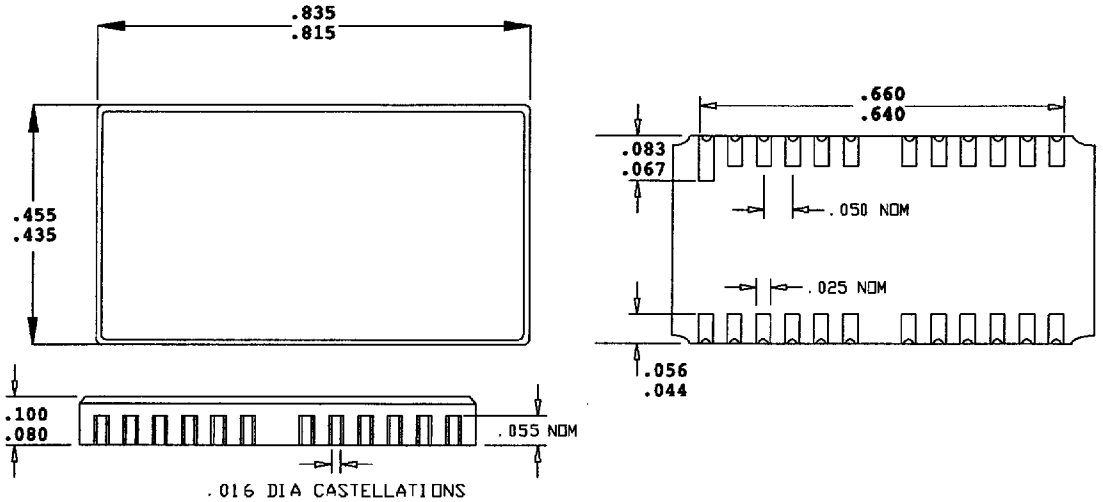
ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (per Method 5005, Table I)
INTERIM ELECTRICAL (PRE-BURN-IN) TEST PARAMETERS (Method 5004)	2, 8A, 10
FINAL ELECTRICAL TEST PARAMETERS (Method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
GROUP A TEST REQUIREMENTS (Method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
GROUP C AND D END-POINT ELECTRICAL PARAMETERS (Method 5005)	1, 2, 3, 7, 8, 9, 10, 11

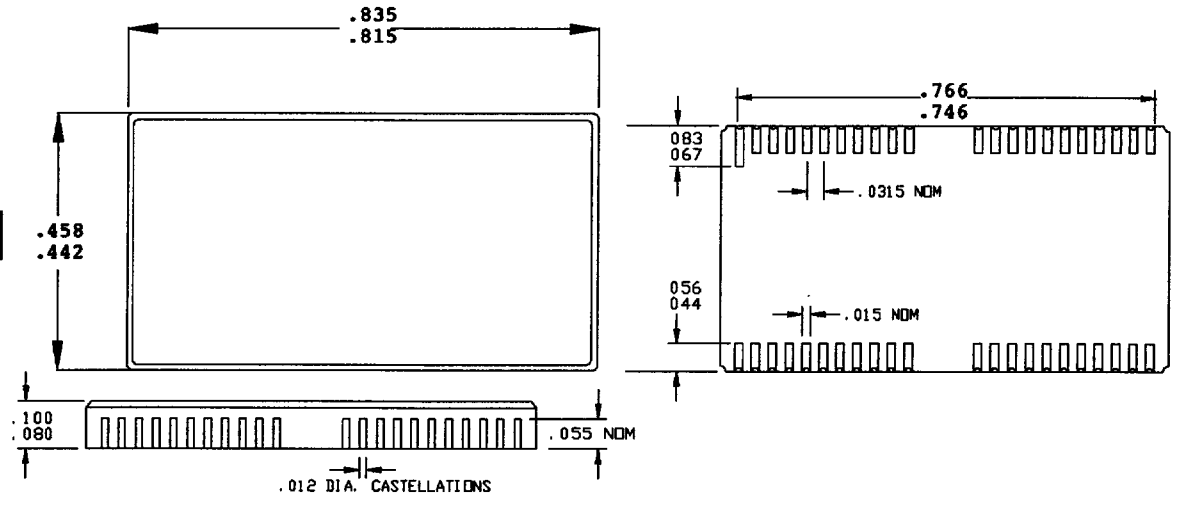
* PDA applies to subgroups 1 and 7.

** Subgroup 4 shall be measured only for initial qualification and after process or design changes, which may affect input or output capacitance.

PACKAGE NO. 212
24/28 CLCC

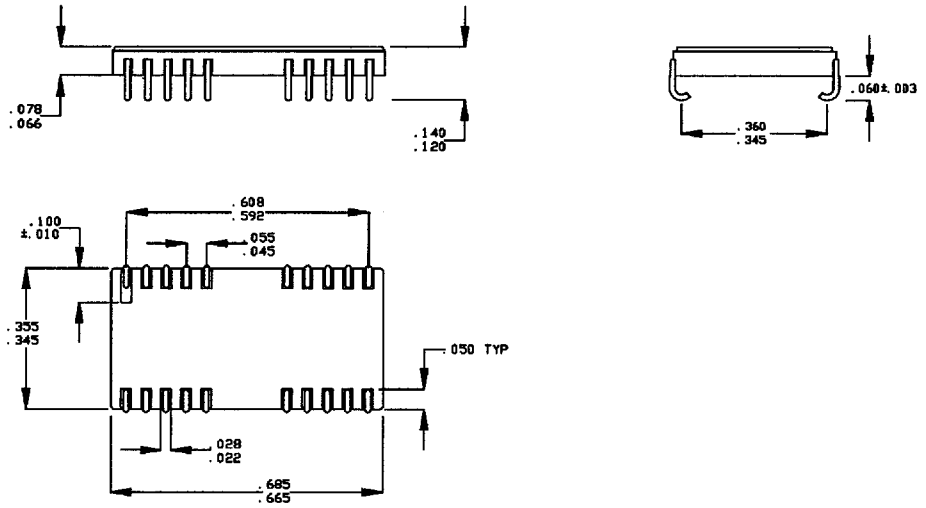


PACKAGE NO. 213
44/50 CLCC

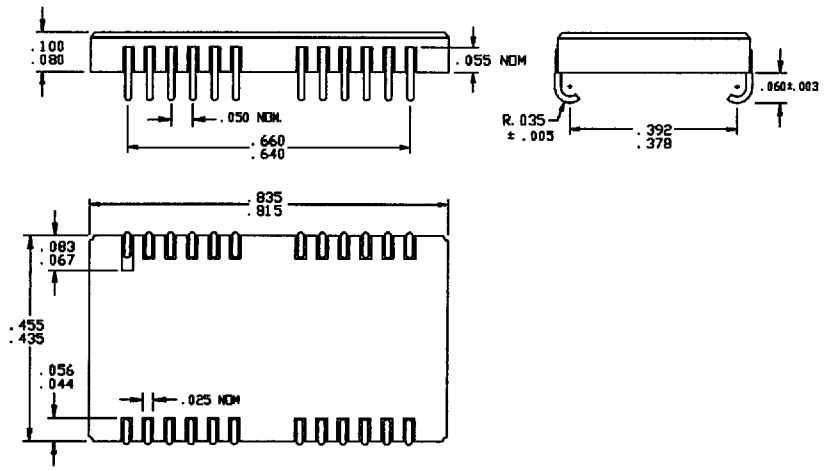


PKG-14

PACKAGE NO. 504
20 CSOJ

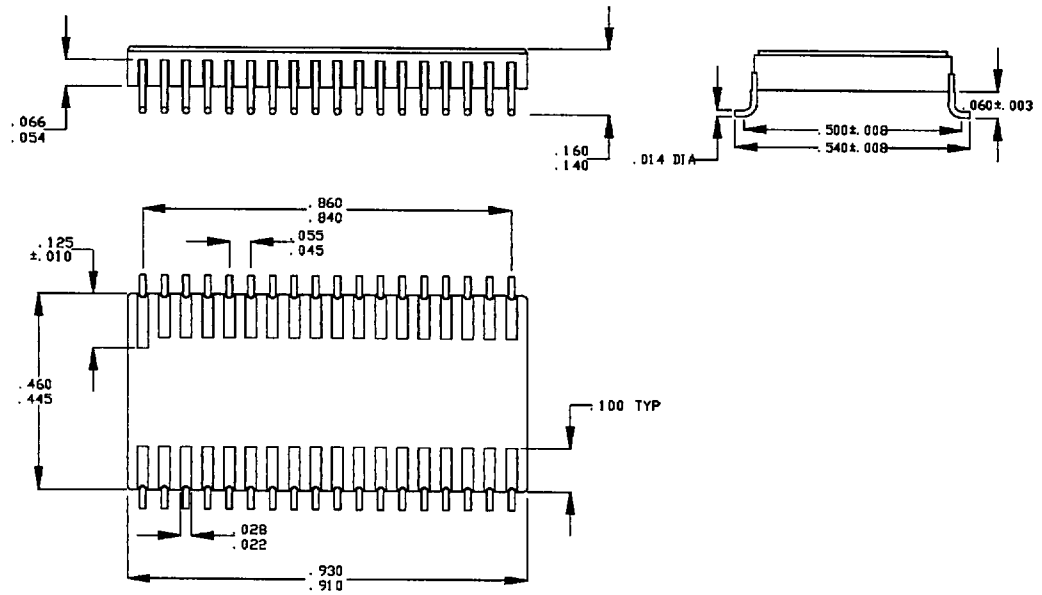


PACKAGE NO. 505
24 CSOJ

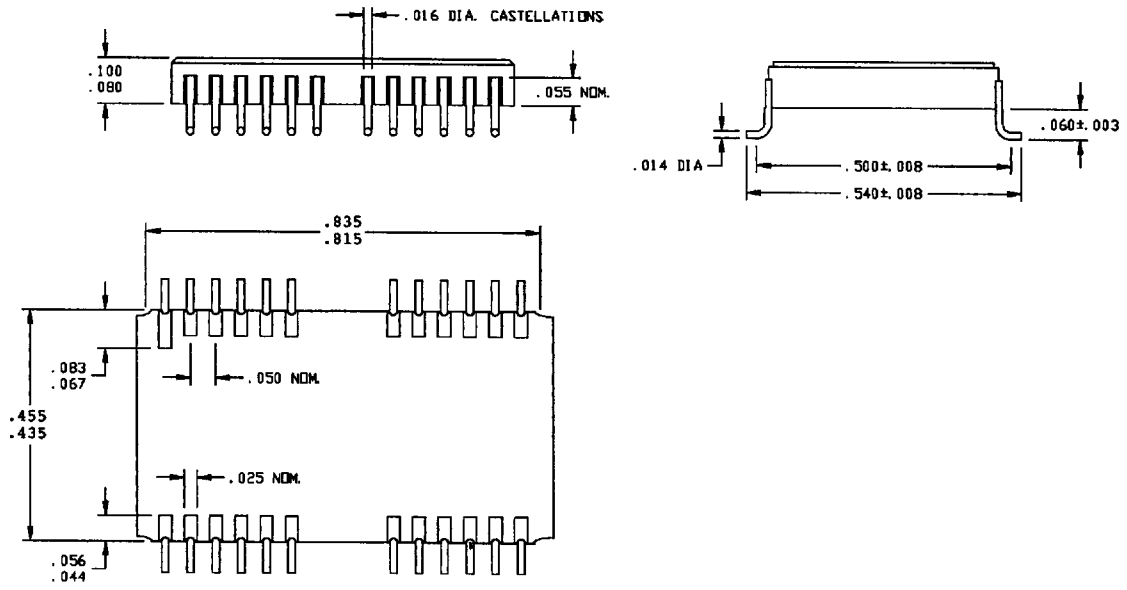


PKG-22

PACKAGE NO. 602
36 CGULL-WING



PACKAGE NO. 603
24/28 CGULL-WING



PKG-25