FEATURES

- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- 3-State outputs for bus interfacing
- Common output enable
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Power-up 3-State
- Power-up reset
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The LVT574 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates. The state of each D input (one set-up time before the Low-to-High clock transition) is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the clock operation.

When $\overline{OE}$ is Low, the stored data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "off" state, which means they will neither drive nor load the bus.

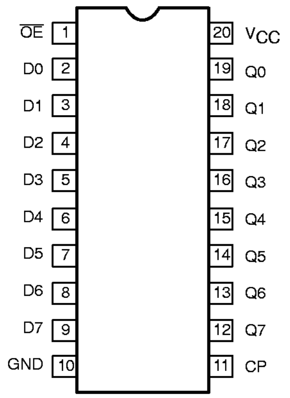
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Qn	C_L = 50pF; V_{CC} = 3.3V	3.6 4.3	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	4	pF
C_{OUT}	Output capacitance	Outputs disabled; $V_{I/O}$ = 0V or 3.0V	8	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	0.13	mA

ORDERING INFORMATION

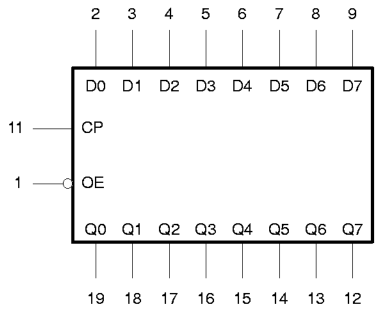
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic SOL	–40°C to +85°C	74LVT574 D	74LVT574 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74LVT574 DB	74LVT574 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVT574 PW	74LVT574PW DH	SOT360-1

PIN CONFIGURATION



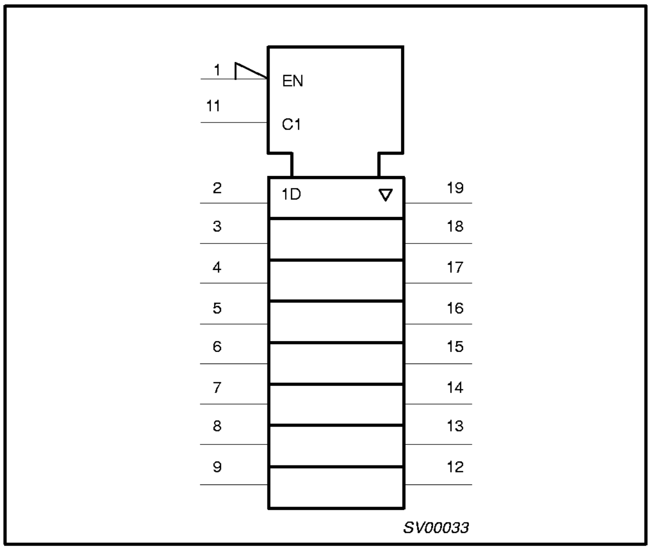
SV00041

LOGIC SYMBOL



SV00042

LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

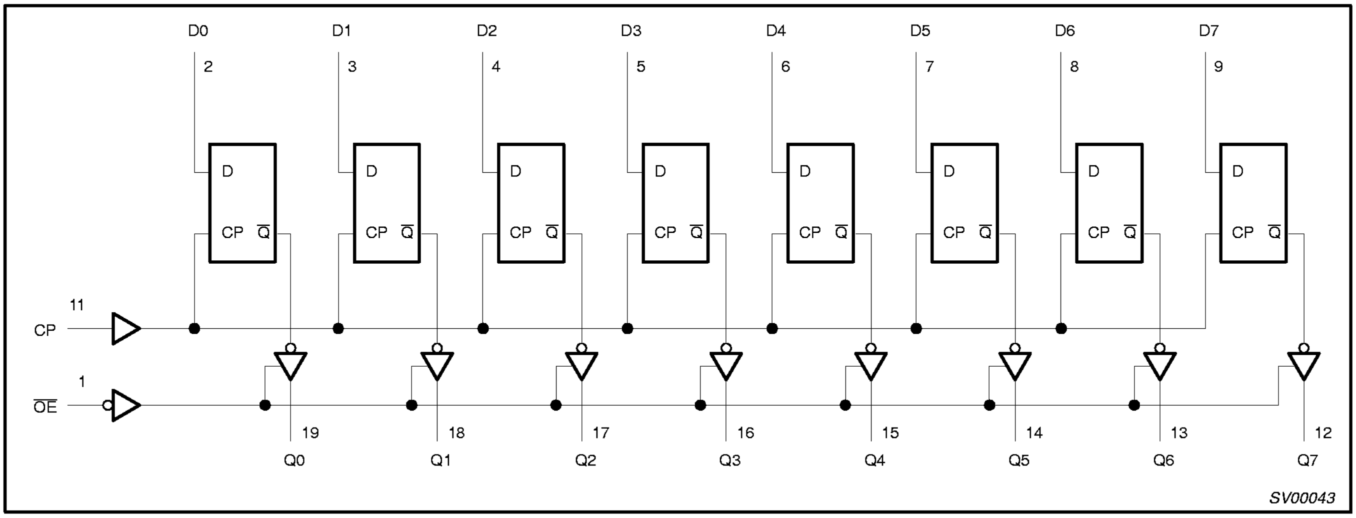
PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output enable input (active-low)
2, 3, 4, 5, 6, 7, 8, 9	D0-D7	Data inputs
19, 18, 17, 16, 15, 14, 13, 12	Q0-Q7	Data outputs
11	CP	Clock pulse input (active rising edge)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING
$\overline{OE}$	CP	Dn	REGISTER	Q0 – Q7	MODE
L L	↑ ↑	l h	L H	L H	Load and read register
L	↑̸	X	NC	NC	Hold
H	X	X	NC	Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↑̸ = not a Low-to-High clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%, f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}-0.1		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.2		
V_{OL}	Low-level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}			0.13	0.55	V
I_I	Input leakage current	V_{CC} = 0 or 3.6V; V_I = 5.5V			1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		±0.1	±1	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 3.6V; V_I = 0			–1	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus Hold current A inputs[7]	V_{CC} = 3V; V_I = 0.8V		75	150		µA
		V_{CC} = 3V; V_I = 2.0V		–75	–150		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; OE/$\overline{OE}$ = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC}= 3.6V; V_O = 3V; V_I = V_{IL} or V_{IH}			1	5	µA
I_{OZL}	3-State output Low current	V_{CC}= 3.6V; V_O = 0.5V; V_I = V_{IL} or V_{IH}			1	–5	µA
I_{CCH}	Quiescent supply current[3]	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC} -0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
6. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V, t_R = t_F = 2.5ns, C_L = 50pF, R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V		
			MIN	TYP[1]	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	NO TAG	150			150		ns
t_{PLH} t_{PHL}	Propagation delay CP to Qn	NO TAG	1.7 2.4	3.6 4.3	5.4 5.9		6.2 6.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	NO TAG NO TAG	1.0 1.3	2.9 3.4	4.8 5.1		5.9 6.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	NO TAG NO TAG	1.9 1.7	4.0 3.2	5.5 4.5		5.9 4.5	ns

NOTE:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

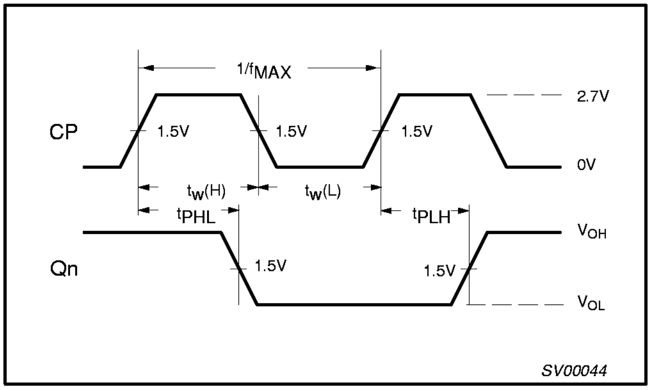
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F = 2.5ns$, $C_L = 50pF$, $R_L = 500\Omega$; $T_{amb} = -40°C$ to $+85°C$.

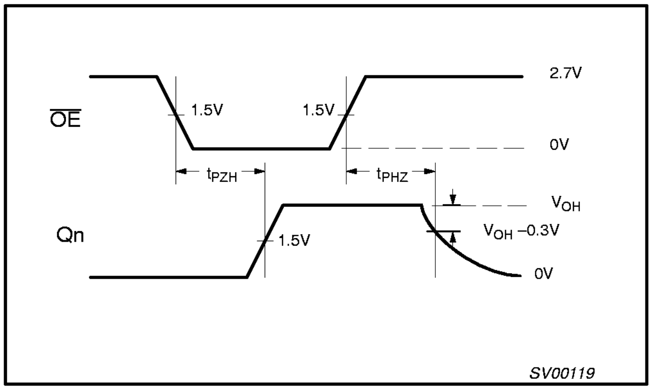
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$	
			MIN	MAX	MIN	
$t_S(H)$ $t_S(L)$	Setup time, High or Low, Dn to CP	NO TAG	2.0 2.0		2.4 2.4	ns
$T_H(H)$ $T_H(L)$	Hold time, High or Low, Dn to CP	NO TAG	0.3 0.3		0 0	ns
$T_W(H)$	CP pulse width High or Low	NO TAG	3.3 3.3		3.3 3.3	ns

AC WAVEFORMS

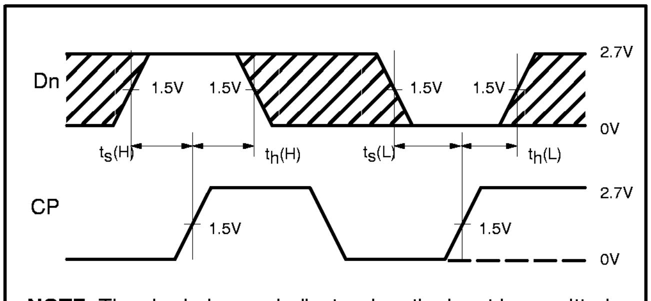
$V_M = 1.5V$, V_{IN} = GND to 2.7V



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



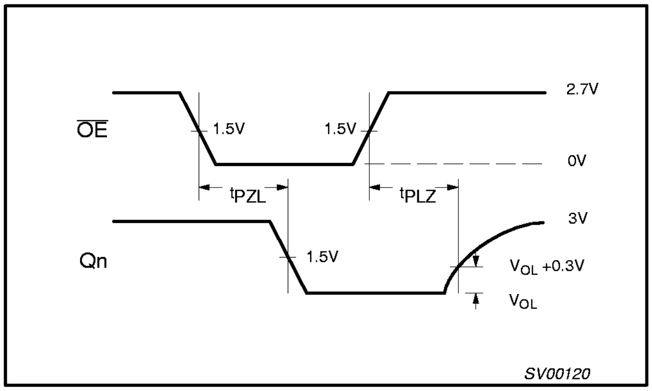
Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

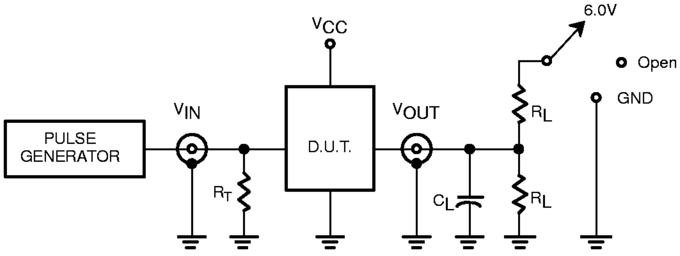
SV00108

Waveform 2. Data Setup and Hold Times

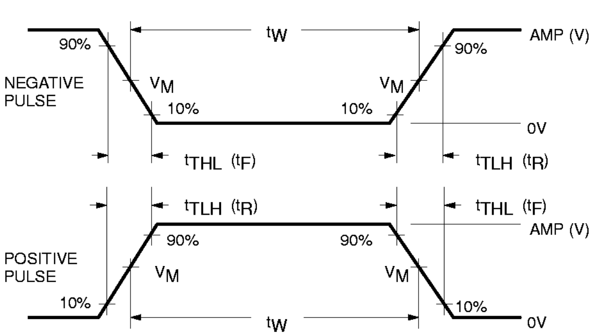


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



$V_M = 1.5V$
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

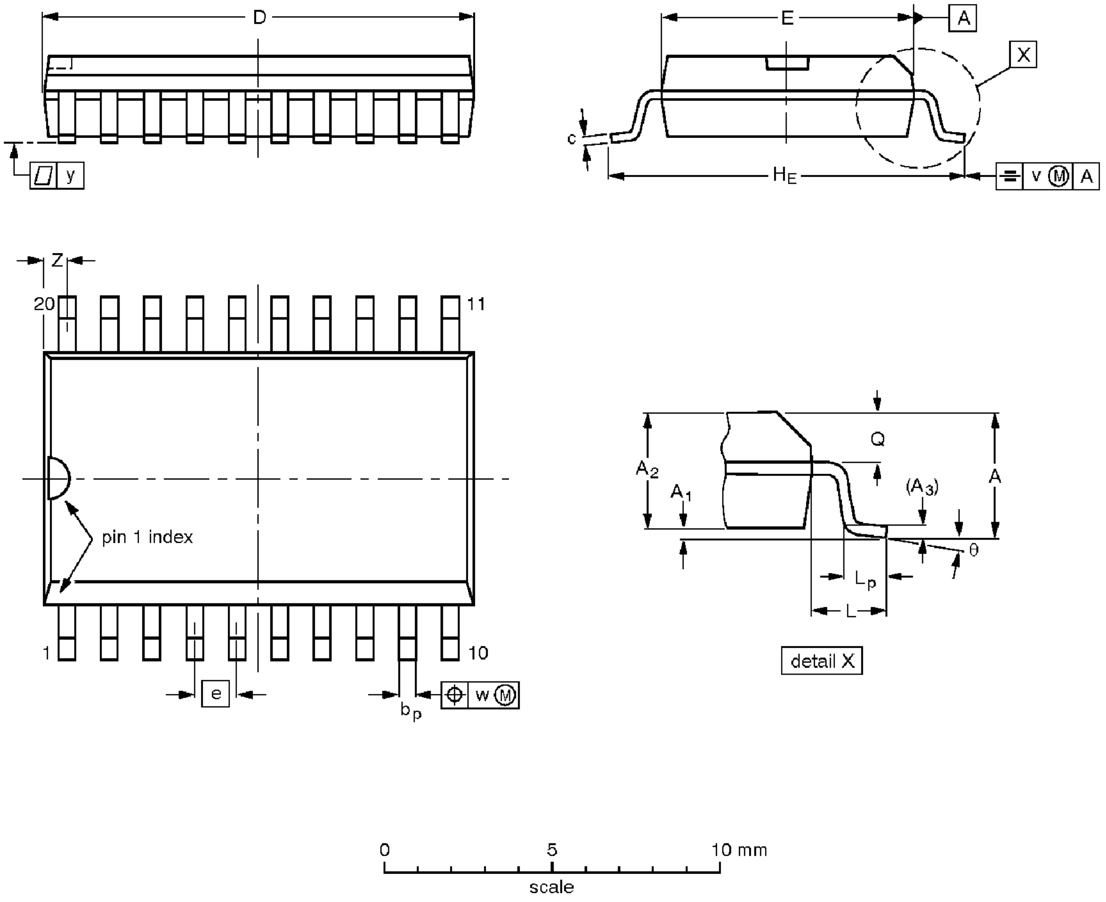
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤ 10MHz	500ns	≤ 2.5ns	≤ 2.5ns

SV00092

SO20: plastic small outline package; 20 leads; body width 7.5 mm SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

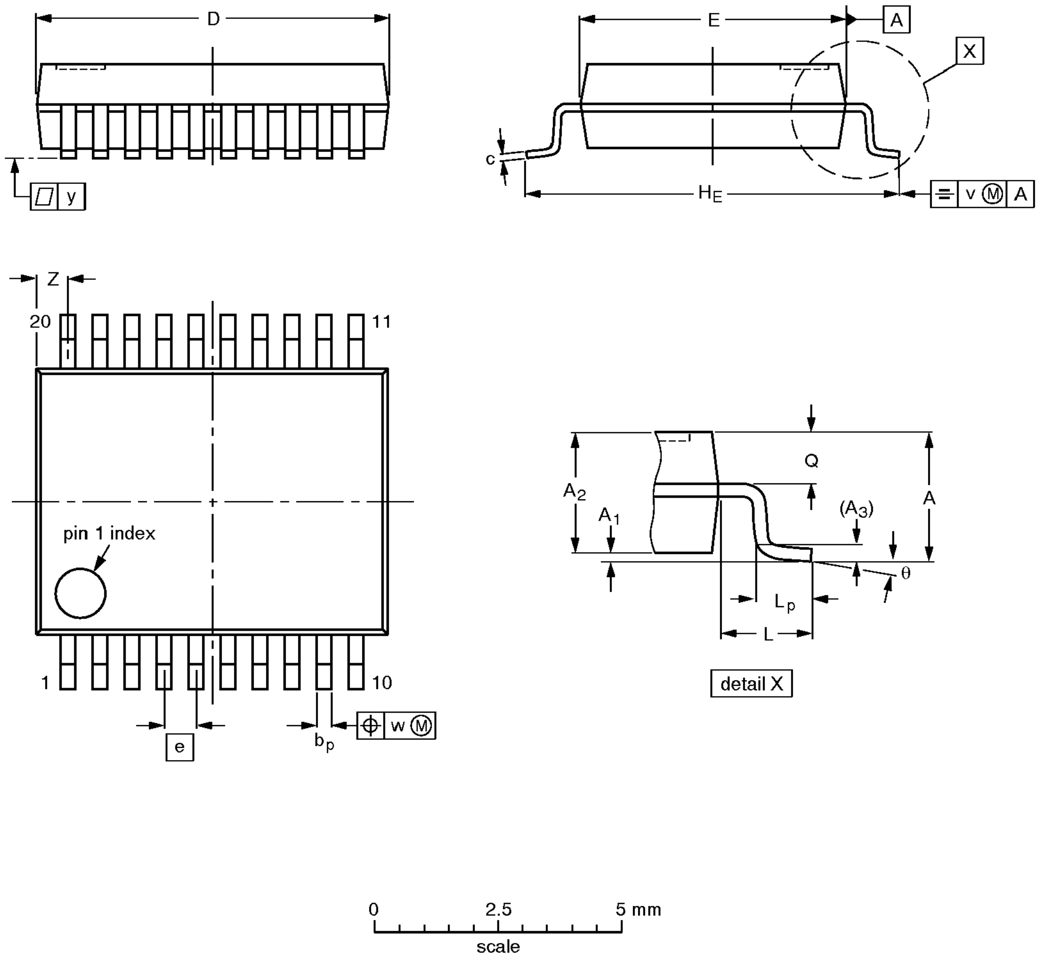
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm SOT339-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

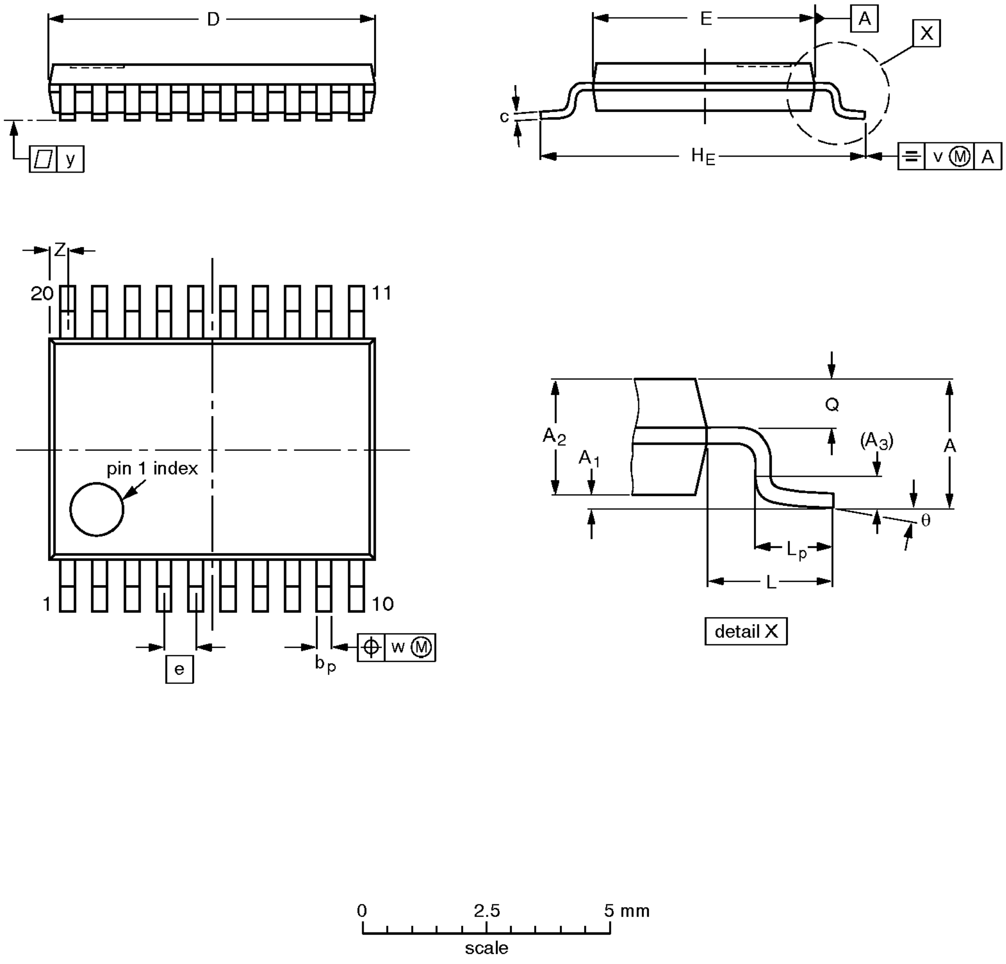
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				~~93-09-08~~ 95-02-04

3.3V Octal D-type flip-flop (3-State)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm SOT360-1

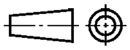


DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				~~93-06-16~~ 95-02-04