REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 04 & 05 for vendor CAGE CODE (61772). Table I: Sheet 5 for the t_{PHZ}/t_{PLZ} change from: 30 ns maximum to 35 ns maximum for device types 02 & 03. Editorial changes throughout.	92-05-14	Tim H. Noh

THE ORIGANL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV	A	A	A	A	A														
SHEET	15	16	17	18	19														

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE
AMSC N/A

PREPARED BY
Todd Creek

CHECKED BY
Ray Monnin

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
28 Apr 89

REVISION LEVEL A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS,
16 X 16 BIT MULTIPLIER
ACCUMULATOR, MONOLITHIC SILICON

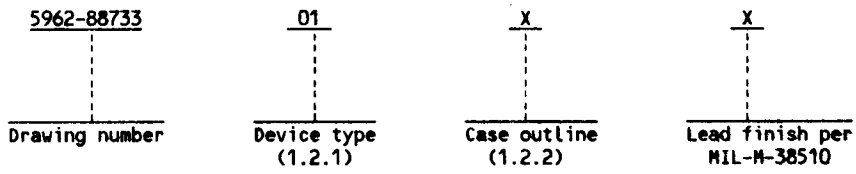
SIZE	CAGE CODE	5962-88733
A	67268	

SHEET 1 OF 19

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Multiply time
01	See 6.7	16 x 16 multiplier accumulator	55 ns
02	See 6.7	16 x 16 multiplier accumulator	65 ns
03	See 6.7	16 x 16 multiplier accumulator	75 ns
04	See 6.7	16 x 16 multiplier accumulator	30 ns
05	See 6.7	16 x 16 multiplier accumulator	40 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
T	See figure 1 (64-lead, .915" x .915" x .090"), leaded chip carrier package
X	D-13 (64-lead, 3.240" x .920" x .225"), dual-in-line package 1/
Y	C-7 (68-terminal, .962" x .962" x .120"), square chip carrier
Z	P-BC (68-pin, 1.135" x 1.135" x .345"), pin grid array

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
DC voltage applied to outputs	-0.5 V dc to +7.0 V dc
DC input voltage	-0.5 V dc to +7.0 V dc
DC output current	10 mA
Maximum power dissipation 2/	1.2 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case T	28°C/W
Cases X, Y, and Z	See MIL-M-38510, appendix C
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc
Ground voltage (GND)	0 V dc
Input high voltage (V_{IH})	2.0 V dc to 6.0 V dc
Input low voltage (V_{IL})	-0.5 V dc to +0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ This package shall be in accordance with MIL-M-38510, appendix C, except configuration 2 is allowed and as specified on figure 2 herein.
2/ Must withstand the added P_D due to short circuit test, e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein and figures 1 and 2.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 3.

3.2.3 Truth tables. The truth tables shall be as specified on figure 4.

3.2.4 Input/output data formats. The input/output data formats shall be as specified on figure 5.

3.2.5 Logic diagram. The logic diagram shall be as specified on figure 6.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

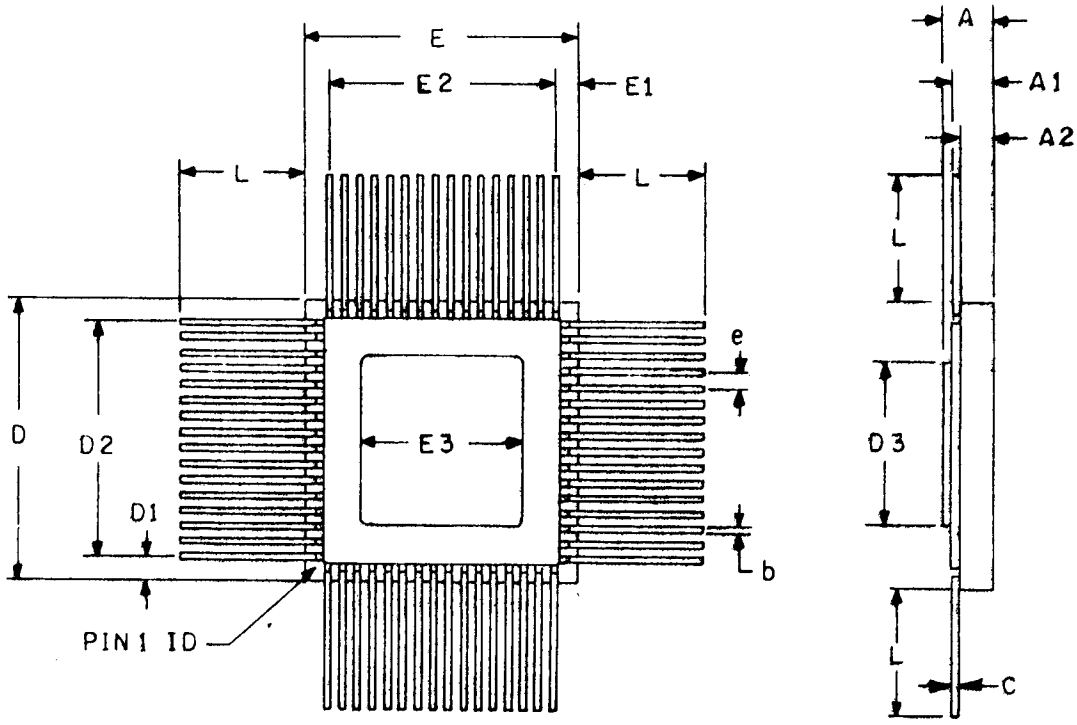
Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Device types	Group A subgroups	Limits		Unit
						Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -0.4 mA		All	1, 2, 3	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 4.0 mA			1, 2, 3		0.4	V
Input high voltage	V_{IH}				1, 2, 3	2.0		V
Input low voltage	V_{IL}				1, 2, 3		0.8	V
Input leakage current	I_{IX}	V_{CC} = 5.5 V GND $\le V_{IN} \le V_{CC}$			1, 2, 3		+20	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, $\overline{OE}$ = 2.0 V			1, 2, 3		+25	µ
Output short circuit current 2/	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = 0.5 V			1, 2, 3	-3	-30	mA
Supply current (quiescent) 3/	I_{CC1}	V_{CC} = 5.5 V, $V_{IH} \le V_{IN} \le V_{CC}$ or GND $\le V_{IN} \le V_{IL}$, $\overline{OE}$ = HIGH		01,02, 03	1, 2, 3		30	mA
				04,05			50	
Supply current (quiescent) 3/	I_{CC2}	V_{CC} = 5.5 V, $V_{CC} - 0.2 \le V_{IN} \le V_{CC}$ or GND $\le V_{IN} \le 0.2$ V, $\overline{OE}$ = HIGH		All	1, 2, 3		25	mA
Dynamic supply current 3/	I_{CC3}	V_{CC} = 5.5 V, f_{CLK} = 10 MHz, $\overline{OE}$ = HIGH V_{IN} = 0 V to 3.0 V			1, 2, 3		110	mA
Input capacitance	C_{IN}	f = 1.0 MHz V_{IN} = 0 V	V_{IN} = 0 V		4		10	pF
Output capacitance	C_{OUT}	V_{CC} = 5.0 V See 4.3.1c	V_{IN} = 0 V		4		12	pF
Bidirectional capacitance	$C_{I/O}$		$V_{I/O}$ = 0 V		4		12	pF
Functional testing		See 4.3.1d	V_{CC} = 4.5 V, 5.5 V	7,8				

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Multiply accumulate time	t_{MA}	See figure 7 V_{CC} = 4.5 V	01 02 03 04 05	9, 10, 11		55 65 75 30 40	ns
Setup time	t_S		01 02,03 04 05	9, 10, 11	20 25 12 15		ns
Hold time	t_H		All	9, 10, 11	3		ns
Clock pulse width	t_{PW}		01 02,03 04 05	9, 10, 11	25 30 10 15		ns
Output clock to P	t_{PDP}		01 02,03 04 05	9, 10, 11		30 35 20 25	ns
Output clock to Y	t_{PDY}		01 02,03 04 05	9, 10, 11		30 35 20 25	ns
$\overline{OEX}$, $\overline{OEM}$ to P; $\overline{OEL}$ to Y 4/ disable time	t_{PHZ} t_{PLZ}		01 02,03 04 05	9, 10, 11		30 35 20 25	ns
$\overline{OEX}$, $\overline{OEM}$ to P; $\overline{OEL}$ to Y enable time	t_{PZH} t_{PZL}		01 02,03 04 05	9, 10, 11		30 35 20 25	ns
Relative hold time 5/	t_{HCL}		All	9, 10, 11	0		ns

1/ Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V and output loading of the specified I_{OL}, I_{OH}, and 40 pF load capacitance. All test to be performed at worst case test conditions unless otherwise specified.
2/ For test purposes, not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. Guaranteed, if not tested, to the specified limits.
3/ Two quiescent figures are given for different input voltage ranges. To calculate I_{CC} at any given clock frequency, use 30 mA + I_{CC}(ac), where I_{CC}(ac) = (8 mA/MHz) x clock frequency.
4/ Transition is measured at steady state high level -500 mV or steady state low level +500 mV on the output from the 1.5 V level on the input and output load B on figure 7.
5/ Guaranteed to the limit specified herein, if not tested.

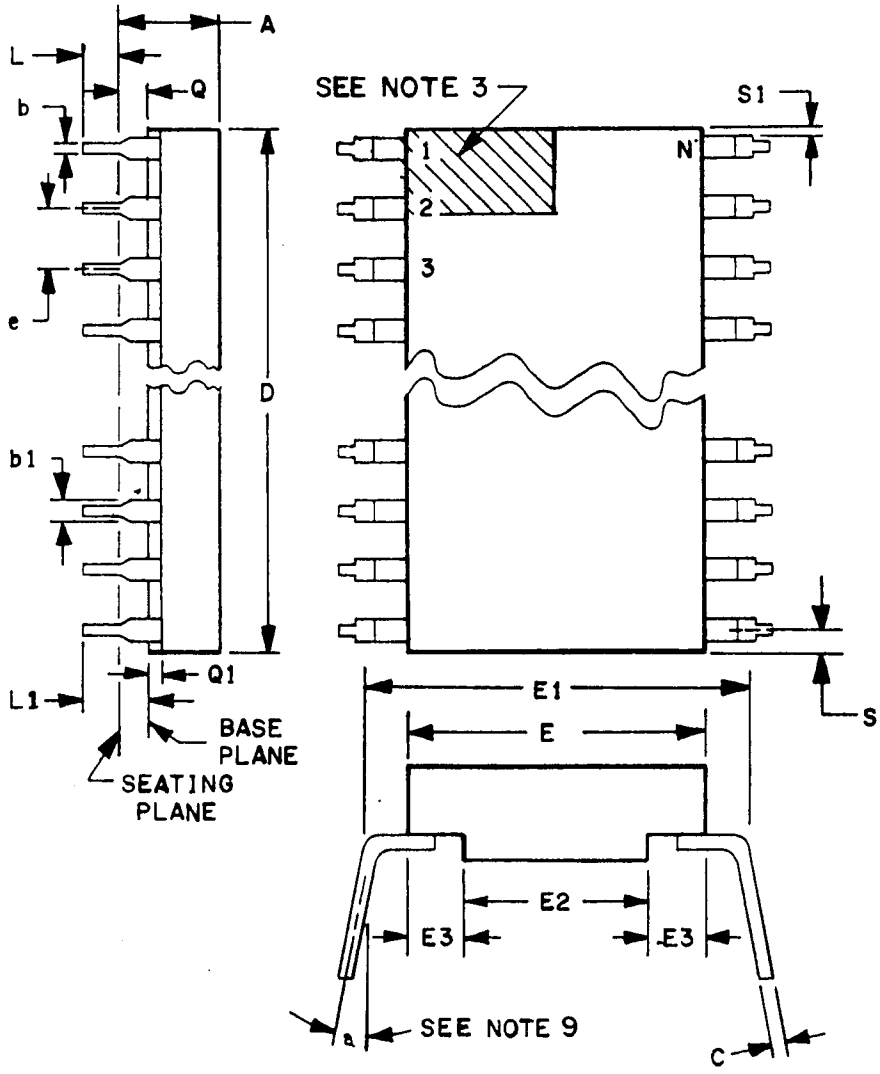


Ltr	Dimensions				Notes	Ltr	Dimensions				Notes
	Inches		Millimeters				Inches		Millimeters		
	Min	Max	Min	Max			Min	Max	Min	Max	
A	.070	.090	1.78	2.29		D3	.505	.535	12.83	13.59	
A1	.060	.078	1.52	1.98		e	.050 BSC		1.27		3
A2	.030	.045	0.76	1.14		E	.885	.915	22.48	23.24	
b	.016	.020	0.41	0.51		E1	.075 REF		1.90		
C	.009	.012	0.23	0.30		E2	.750 BSC		19.05		
D	.885	.915	22.48	23.24		E3	.505	.535	12.83	13.59	
D1	.075 REF		1.90			L	.350	.450	8.89	11.43	
D2	.750 BSC		19.05			ND	16				4

NOTES:
1. Dimensions are in inches.
2. BSC - Basic pin spacing between centers.
3. ND is the number of leads per package side.

FIGURE 1. Case outline T (64-lead, leaded chip carrier package).

Case X



Configuration 2

FIGURE 2. Case outline (64-pin, dual-in-line package)

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-88733
		REVISION LEVEL A	SHEET 7

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
A	---	.225	---	5.72	
b	.014	.023	0.36	0.58	8
b_1	.038	.065	0.97	1.65	2, 8
c	.008	.015	0.20	0.38	8
D	---	3.24	---	82.30	4
E	.780	.820	19.81	20.83	4
E_1	.870	.920	22.10	23.37	7
E_2	.600	---	15.24	---	
E_3	.050	---	1.27	---	

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
e	.100 BSC		2.54 BSC		5, 9
L	.125	.200	3.18	5.08	
L_1	.150	---	3.81	---	
Q	.080	.110	2.03	2.79	3
Q_1	.020	---	0.51	---	
S	---	.100	---	2.54	6
S_1	.005	---	0.13	---	6
a	0°	15°	0°	15°	

NOTES:
1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The minimum limit for dimension b_1 may be .023 (0.58 mm) for lead numbers 1, 32, 33, and 64 only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54 mm) between centerlines. Each lead centerline shall be located within ±.010 (0.25 mm) of its exact longitudinal position relative to leads 1 and 64.
6. Applies to all four corners. Lead numbers 1, 32, 33, and 64 shall apply.
7. Lead center when a is 0°. E_1 shall be measured at the centerline of the leads.
8. All leads: Increase maximum limit by .003 (0.08 mm) measured at the center of the flat, when lead finish A or B is applied.
9. Sixty-two places.
10. If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

FIGURE 2. Case outline (64-pin, dual-in-line package) - Continued.

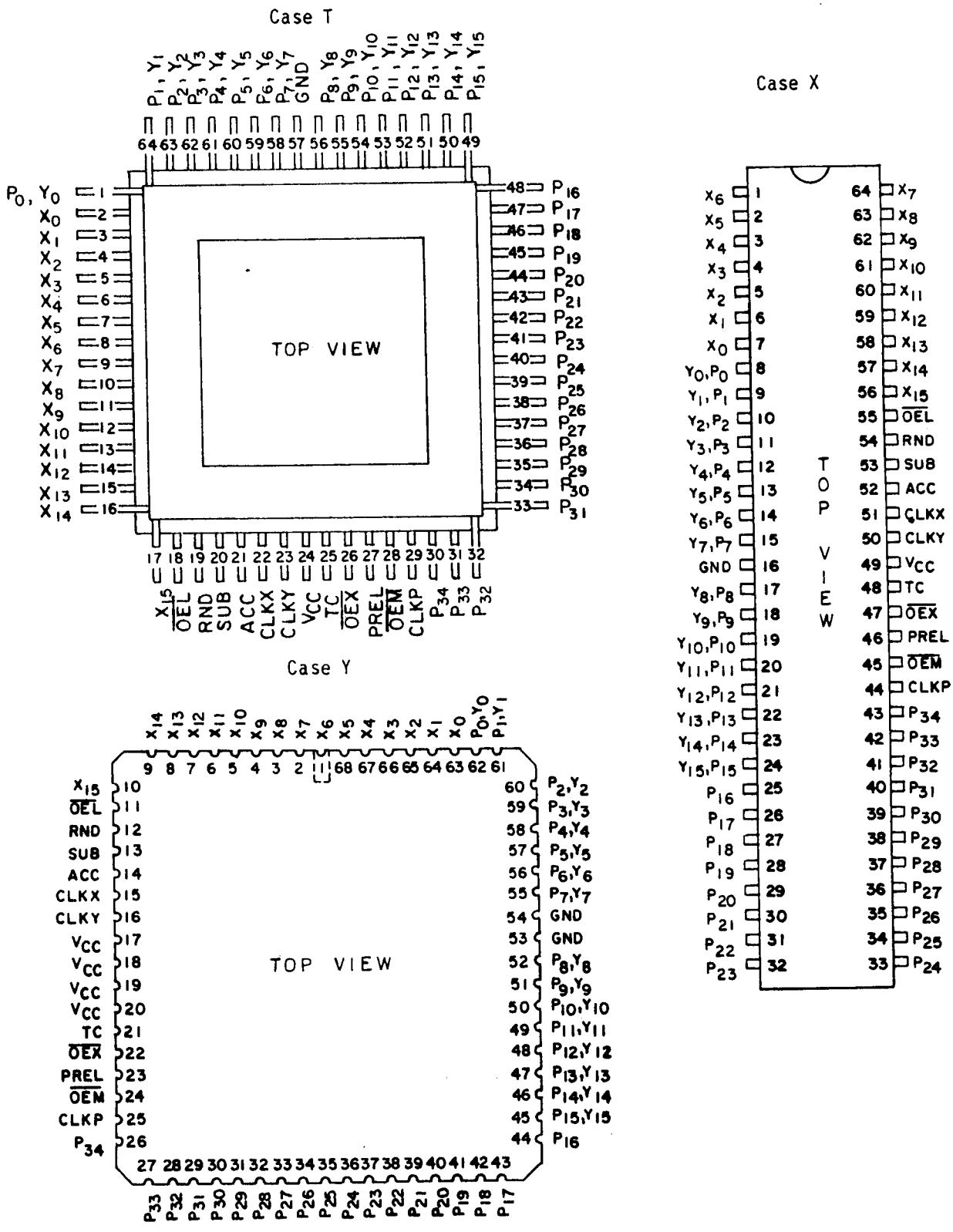
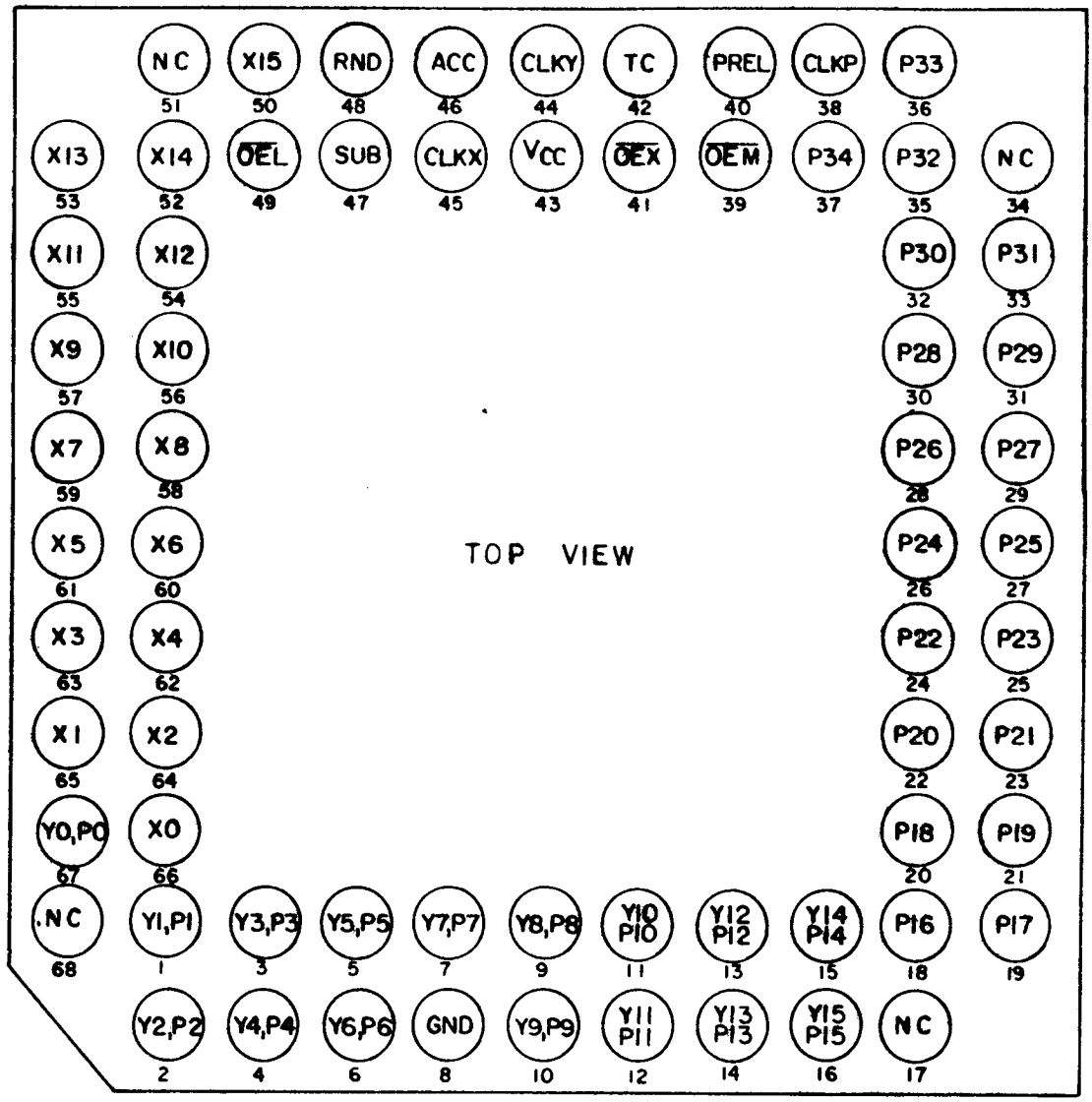


FIGURE 3. Terminal connections.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-88733
		REVISION LEVEL A	SHEET 9



Case Z

FIGURE 3. Terminal connections - Continued.

Preload function table

PREL	$\overline{OEX}$	$\overline{OEM}$	$\overline{OEL}$	Output register XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Z
0	0	1	0	Q	Z	Q
0	0	1	1	Q	Z	Z
0	1	0	0	Z	Q	Q
0	1	0	1	Z	Q	Z
0	1	1	0	Z	Z	Q
0	1	1	1	Z	Z	Z
1	0	0	0	Z	Z	Z
1	0	0	1	Z	Z	PL
1	0	1	0	Z	PL	Z
1	0	1	1	Z	PL	PL
1	1	0	0	PL	Z	Z
1	1	0	1	PL	Z	PL
1	1	1	0	PL	PL	Z
1	1	1	1	PL	PL	PL

Accumulator function table

PREL	ACC	SUB	P	Operation
L	L	X	Q	Load
L	H	L	Q	Add
L	H	H	Q	Subtract
H	X	X	PL	Preload

Z = Output buffers at high impedance (disabled).
Q = Output buffers at low impedance. Contents of output register available through output ports.
PL = Output disabled. Preload data supplied to the output pins will be loaded into the output register at the rising edge of CLKP.

FIGURE 4. Truth tables.

INPUT FORMATS

FRACTIONAL TWO'S COMPLEMENT INPUT

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}
(SIGN)															

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}
(SIGN)															

INTEGER TWO'S COMPLEMENT INPUT

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
(SIGN)															

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
(SIGN)															

UNSIGNED FRACTIONAL INPUT

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

UNSIGNED INTEGER INPUT

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

OUTPUT FORMATS

TWO'S COMPLEMENT FRACTIONAL OUTPUT

XTP			MSP														LSP														
34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}
(SIGN)																																	

TWO'S COMPLEMENT INTEGER OUTPUT

XTP			MSP														LSP														
34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{34}	2^{33}	2^{32}	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
(SIGN)																																	

UNSIGNED FRACTIONAL OUTPUT

XTP			MSP														LSP														
34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	2^{-31}	2^{-32}

UNSIGNED INTEGER OUTPUT

XTP			MSP														LSP														
34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{34}	2^{33}	2^{32}	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

FIGURE 5. Input/output data formats.

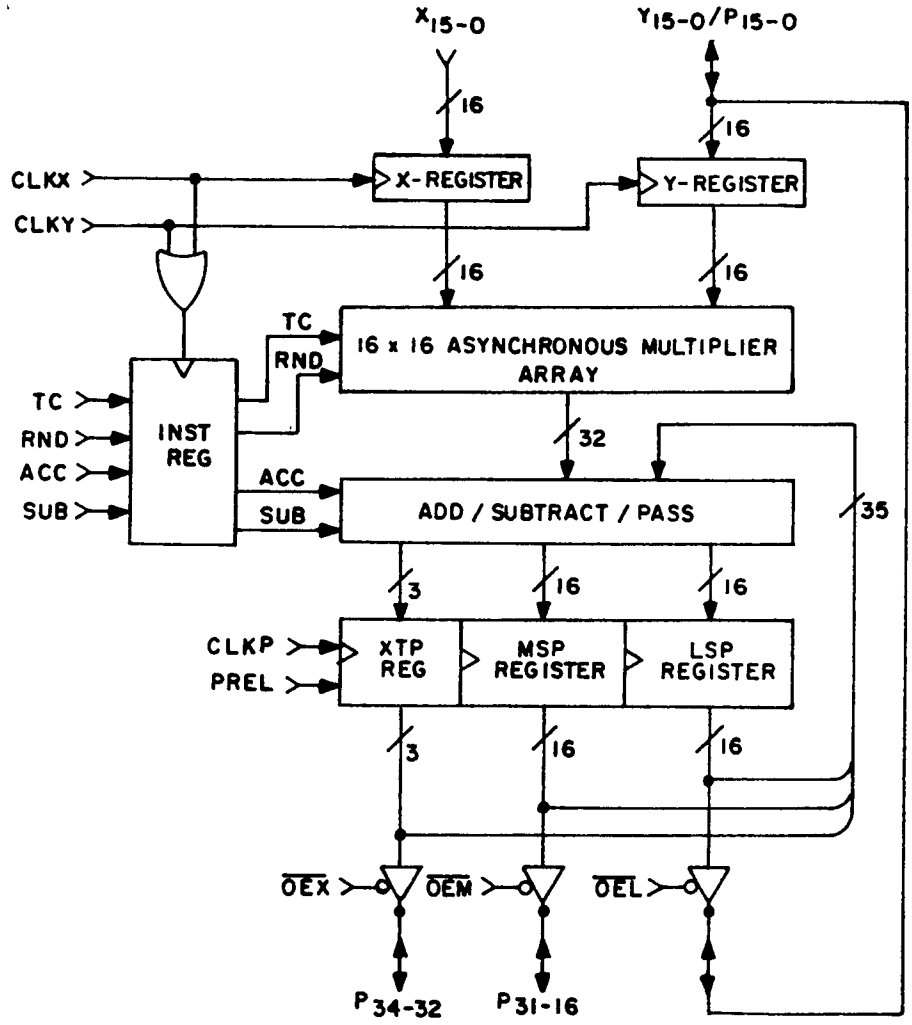
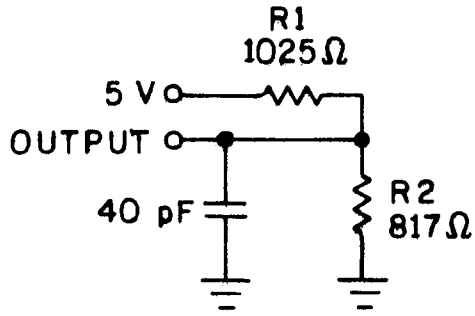
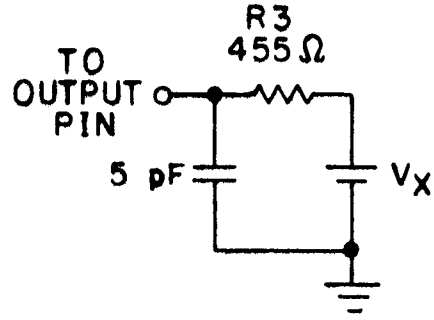


FIGURE 6. Logic diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-88733
		REVISION LEVEL A	SHEET 13

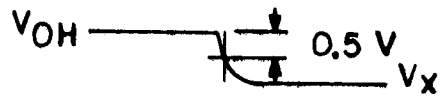
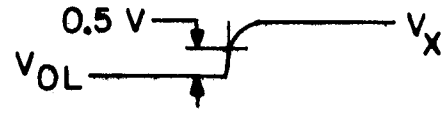
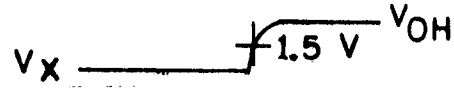
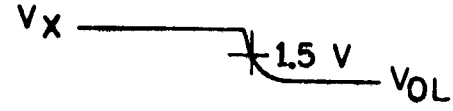


LOAD CIRCUIT A



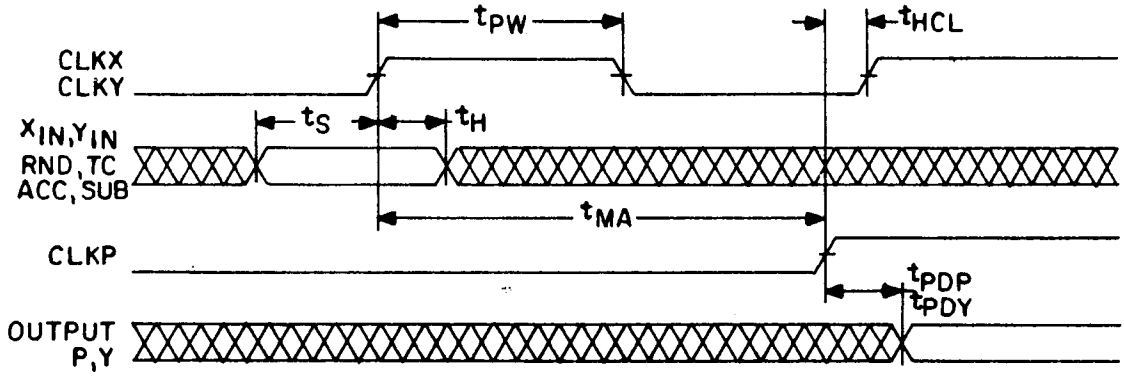
LOAD CIRCUIT B

Three-state

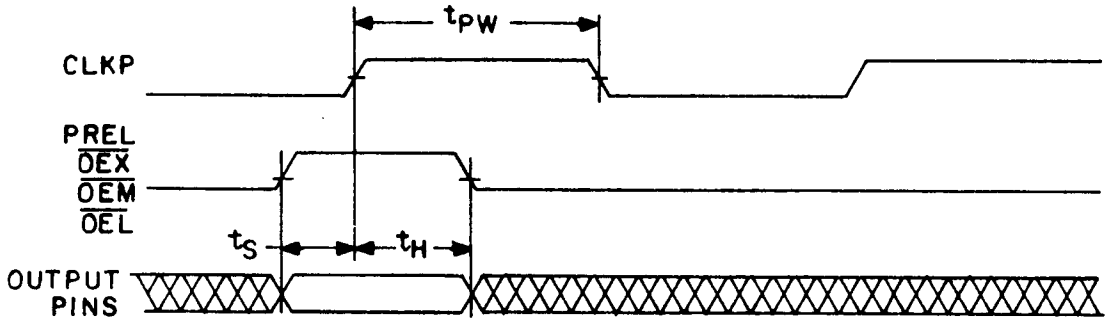
Test	V_X	Output waveform-measurement level
t_{PHZ}	0.0 V	
t_{PLZ}	2.6 V	
t_{PZH}	0.0 V	
t_{PZL}	2.6 V	

NOTE: Three-state tests utilize load circuit B all other tests utilize load circuit A.

FIGURE 7. Waveforms and test circuits.



PRELOAD TIMING DIAGRAM



THREE-STATE TIMING DIAGRAM

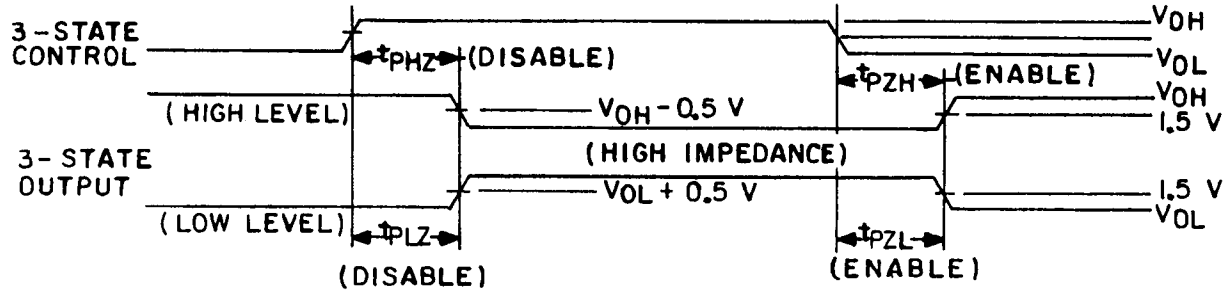


FIGURE 7. Waveforms and test circuits - Continued.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.7 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN}, C_{OUT}, and $C_{I/O}$ measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of 5 devices shall be required.

d. Subgroups 7 and 8 shall consist of verifying the functionality of the device. These tests form a part of the vendor's test tape and shall be maintained and available from the approved source of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition B or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*, 8,9
Group A test requirements (method 5005)	1,2,3,4,7, 8,9,10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3

* PDA applies to subgroups 1 and 7.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8526.

6.6 Pin descriptions.

Pin	I/O	Description
X_{15-0}	I	X input data. This 16-bit number may be interpreted as two's complement or unsigned magnitude.
Y_{15-0} (P_{15-0})	I/O	Y input data/LSP output data. This 16-bit number may be interpreted as two's complement or unsigned magnitude. The Y input port may be multiplexed with the LSP output (P_{15-0}), and can also be used to preload the LSP register.
P_{34-32}	I/O	Extended product (XTP) output data. This port is bidirectional. The extended product emerges through this port. The XTP register may also be preloaded through this port.
P_{31-16}	I/O	MSP output data. This port is bidirectional. The most significant product emerges through this port. The MSP register may also be preloaded through this port.
P_{15-0}	I/O	LSP output data. This port is bidirectional. The least significant product emerges through this port. The LSP register may also be preloaded through this port.
CLKX	I	X register clock. X input data are latched into the X-register at the rising edge of CLKX.
CLKY	I	Y register clock. Y input data are latched into the Y-register at the rising edge of CLKY.
CLKP	I	Product register clock. XTP, MSP, and LSP are latched into their respective registers at the rising edge of CLKP. If preload is selected, these registers are loaded with the preload data at the output pins via the bidirectional ports. If preload is not selected, these registers are loaded with the current accumulated product.
$\overline{OEX}$	I	Output enable extended. When low, the extended product bidirectional port is enabled for output. When high, the output drivers are disabled (high impedance) and the XTP port may be used for preloading. See preload function table.
$\overline{OEM}$	I	Output enable most. When low, the MSP bidirectional port is enabled for output. When high, the output drivers are disabled (high impedance) and the MSP port may be used for preloading. See preload function table.
$\overline{OEL}$	I	Output enable least. When low, the LSP bidirectional port is enabled for output. When high, the output drivers are disabled (high impedance) and the MSP port may be used for preloading. See preload function table.

6.6 Pin descriptions. - continued

Pin	I/O	Description
PREL	I	Preload. When high, the three bidirectional ports may be used to preload data into the accumulattor register at the rising edge of CLKP. The three-state controls (OEX,OEM, OEL) must be high to preload data. When low, the accumulated product is loaded into the accumulator/output register at the rising edge of CLKP. The output drivers must be enabled (OEX, OEM, OEL must be low) for the accumulated product to be output. Ordinarily, PREL, OEX, OEM, and OEL are tied together. See accumulator function table.
TC	I	Two's complement control. When high, the device is in two's complement mode, where the input and output data are interpreted as two's complement numbers. The device is in unsigned magnitude mode when TC is low. This control is loaded into the instruction register at the rising edge of CLKX + CLKY.
RND	I	Round control. When high, rounding is enabled and a "1" is added to the MSB of the LSP (P_{15}). When low, the product is unchanged. This control is loaded into the instruction register at the rising edge of CLKX + CLKY.
ACC	I	Accumulate control. When high, the accumulator/output register contents are added to or subtracted from the current product (XY) and this result is stored back into the accumulator/output register. When low, the product is loaded into the accumulator register, overwriting the current contents. This control is loaded into the instruction register at the rising edge of CLKX + CLKY. See accumulator function table.
SUB	I	Subtract control. When both ACC and SUB are high, the accumulator register contents are subtracted from the current product XY and this result is written back into the accumulator register. When ACC is high and SUB is low, the accumulator register contents and current product are summed, then written back to the accumulator register. This control is loaded into the instruction register at the rising edge of CLKX + CLKY. See accumulator function table.

6.7 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.